# AMD Xilinx - XC7VX690T-2FFG1157C Datasheet

**Welcome to** **E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 54150 |
| Number of Logic Elements/Cells | 693120 |
| Total RAM Bits | 54190080 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.03V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1157-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-2ffg1157c |

*Table 1:* **Absolute Maximum Ratings[1] *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{MGTAVTTRCAL}$ | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column | –0.5 | 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.26 | V |
| $I_{DCIN}$ | DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| $I_{DCOUT}$ | DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies(6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies(6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
5. See Table 10 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475).

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | Internal supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4). | 0.87 | 0.90 | 0.93 | V |
| $V_{CCBRAM}$(3) | Block RAM supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4). | 0.87 | 0.90 | 1.03 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCO}$(5)(6) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| | Supply voltage for 1.8V HP I/O banks | 1.14 | – | 1.89 | V |
| $V_{CCAUX\_IO}$ | Auxiliary supply voltage when set to 1.8V | 1.71 | 1.80 | 1.89 | V |
| | Auxiliary supply voltage when set to 2.0V | 1.94 | 2.00 | 2.06 | V |
| $V_{IN}$(7) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.2 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(8) | –0.20 | – | 2.625 | V |
| $I_{IN}$(9) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(10) | Battery voltage | 1.0 | – | 1.89 | V |

*Table 5:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks**(1)(2)

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 100 |
| $V_{CCO}$ + 0.60 | 50.0 | –0.60 | 50.0 |
| $V_{CCO}$ + 0.65 | 50.0 | –0.65 | 50.0 |
| $V_{CCO}$ + 0.70 | 47.0 | –0.70 | 50.0 |
| $V_{CCO}$ + 0.75 | 21.2 | –0.75 | 50.0 |
| $V_{CCO}$ + 0.80 | 9.71 | –0.80 | 50.0 |
| $V_{CCO}$ + 0.85 | 4.51 | –0.85 | 28.4 |
| $V_{CCO}$ + 0.90 | 2.12 | –0.90 | 12.7 |
| $V_{CCO}$ + 0.95 | 1.01 | –0.95 | 5.79 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

*Table 6:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2/-2L/-2G | -1 | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7V585T | 1483 | 1483 | 1483 | mA |
| | | XC7V2000T | N/A | 3756 | 3756 | mA |
| | | XC7VX330T | 1012 | 1012 | 1012 | mA |
| | | XC7VX415T | 1324 | 1324 | 1324 | mA |
| | | XC7VX485T | 1578 | 1578 | 1578 | mA |
| | | XC7VX550T | 2214 | 2214 | 2214 | mA |
| | | XC7VX690T | 2214 | 2214 | 2214 | mA |
| | | XC7VX980T | N/A | 2580 | 2580 | mA |
| | | XC7VX1140T | N/A | 3448 | 3448 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7V585T | 1 | 1 | 1 | mA |
| | | XC7V2000T | N/A | 1 | 1 | mA |
| | | XC7VX330T | 1 | 1 | 1 | mA |
| | | XC7VX415T | 1 | 1 | 1 | mA |
| | | XC7VX485T | 1 | 1 | 1 | mA |
| | | XC7VX550T | 1 | 1 | 1 | mA |
| | | XC7VX690T | 1 | 1 | 1 | mA |
| | | XC7VX980T | N/A | 1 | 1 | mA |
| | | XC7VX1140T | N/A | 1 | 1 | mA |

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, $V_{CCAUX\_IO}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$, $V_{CCAUX\_IO}$, and $V_{CCO}$ have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} – V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} – V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

## LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

*Table 12:* **LVDS_25 DC Specifications**(1)

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$ | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$ | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage ($Q - \overline{Q}$),<br>Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage ($Q - \overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage | | 0.300 | 1.200 | 1.425 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

*Table 13:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage | | 1.710 | 1.800 | 1.890 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$ | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$ | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage ($Q - \overline{Q}$),<br>Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage ($Q - \overline{Q}$),<br>Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage | Differential input voltage = ±350 mV | 0.300 | 1.200 | 1.425 | V |

**Notes:**

1. Differential inputs for LVDS can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

*Table 18:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator**(1)(2)

| Memory Standard | I/O Bank Type | $V_{CCAUX\_IO}$ | Speed Grade |  |  | Units |
|---|---|---|---|---|---|---|
|  |  |  | -3 | -2/-2L/-2G | -1 |  |
| **4:1 Memory Controllers** |  |  |  |  |  |  |
| DDR3 | HP | 2.0V | 1866 | 1866 | 1600 | Mb/s |
|  | HP | 1.8V | 1600 | 1333 | 1066 | Mb/s |
|  | HR | N/A | 1066 | 1066 | 800 | Mb/s |
| DDR3L | HP | 2.0V | 1600 | 1600 | 1333 | Mb/s |
|  | HP | 1.8V | 1333 | 1066 | 800 | Mb/s |
|  | HR | N/A | 800 | 800 | 667 | Mb/s |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | Mb/s |
|  | HP | 1.8V | 800 | 800 | 800 | Mb/s |
|  | HR | N/A | 800 | 800 | 800 | Mb/s |
| RLDRAM III | HP | 2.0V | 800 | 667 | 667 | MHz |
|  | HP | 1.8V | 550 | 500 | 450 | MHz |
|  | HR | N/A | N/A |  |  |  |
| **2:1 Memory Controllers** |  |  |  |  |  |  |
| DDR3 | HP | 2.0V | 1066 | 1066 | 800 | Mb/s |
|  | HP | 1.8V | 1066 | 1066 | 800 | Mb/s |
|  | HR | N/A | 1066 | 1066 | 800 | Mb/s |
| DDR3L | HP | 2.0V | 1066 | 1066 | 800 | Mb/s |
|  | HP | 1.8V | 1066 | 1066 | 800 | Mb/s |
|  | HR | N/A | 800 | 800 | 667 | Mb/s |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | Mb/s |
|  | HP | 1.8V |  |  |  |  |
|  | HR | N/A |  |  |  |  |
| QDR II+(3) | HP | 2.0V | 550 | 500 | 450 | MHz |
|  | HP | 1.8V |  |  |  |  |
|  | HR | N/A | 500 | 450 | 400 | MHz |
| RLDRAM II | HP | 2.0V | 533 | 500 | 450 | MHz |
|  | HP | 1.8V |  |  |  |  |
|  | HR | N/A |  |  |  |  |
| LPDDR2 | HP | 2.0V | 667 | 667 | 667 | Mb/s |
|  | HP | 1.8V | 667 | 667 | 667 | Mb/s |
|  | HR | N/A | 667 | 667 | 667 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

*Table 19:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | |
| LVCMOS15_F4 | 0.66 | 0.69 | 0.81 | 1.63 | 1.76 | 1.86 | 2.39 | 2.62 | 2.85 | ns |
| LVCMOS15_F8 | 0.66 | 0.69 | 0.81 | 1.79 | 1.99 | 2.18 | 2.55 | 2.85 | 3.17 | ns |
| LVCMOS15_F12 | 0.66 | 0.69 | 0.81 | 1.40 | 1.54 | 1.65 | 2.16 | 2.40 | 2.64 | ns |
| LVCMOS15_F16 | 0.66 | 0.69 | 0.81 | 1.37 | 1.51 | 1.61 | 2.13 | 2.37 | 2.60 | ns |
| LVCMOS12_S4 | 0.88 | 0.91 | 1.00 | 2.53 | 2.67 | 2.76 | 3.29 | 3.53 | 3.75 | ns |
| LVCMOS12_S8 | 0.88 | 0.91 | 1.00 | 2.05 | 2.18 | 2.28 | 2.81 | 3.04 | 3.27 | ns |
| LVCMOS12_S12(1) | 0.88 | 0.91 | 1.00 | 1.75 | 1.89 | 1.98 | 2.51 | 2.75 | 2.97 | ns |
| LVCMOS12_F4 | 0.88 | 0.91 | 1.00 | 1.94 | 2.07 | 2.17 | 2.70 | 2.93 | 3.16 | ns |
| LVCMOS12_F8 | 0.88 | 0.91 | 1.00 | 1.50 | 1.64 | 1.73 | 2.26 | 2.50 | 2.72 | ns |
| LVCMOS12_F12(1) | 0.88 | 0.91 | 1.00 | 1.54 | 1.71 | 1.87 | 2.30 | 2.57 | 2.86 | ns |
| SSTL135_S | 0.61 | 0.64 | 0.73 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| SSTL15_S | 0.61 | 0.64 | 0.73 | 1.24 | 1.37 | 1.47 | 2.00 | 2.23 | 2.46 | ns |
| SSTL18_I_S | 0.64 | 0.67 | 0.76 | 1.59 | 1.74 | 1.85 | 2.35 | 2.60 | 2.84 | ns |
| SSTL18_II_S | 0.64 | 0.67 | 0.76 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| DIFF_SSTL135_S | 0.59 | 0.61 | 0.73 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| DIFF_SSTL15_S | 0.63 | 0.67 | 0.77 | 1.24 | 1.37 | 1.47 | 2.00 | 2.23 | 2.46 | ns |
| DIFF_SSTL18_I_S | 0.65 | 0.69 | 0.78 | 1.50 | 1.63 | 1.72 | 2.26 | 2.49 | 2.71 | ns |
| DIFF_SSTL18_II_S | 0.65 | 0.69 | 0.78 | 1.13 | 1.22 | 1.25 | 1.89 | 2.08 | 2.24 | ns |
| SSTL135_F | 0.61 | 0.64 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| SSTL15_F | 0.61 | 0.64 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| SSTL18_I_F | 0.64 | 0.67 | 0.76 | 1.12 | 1.22 | 1.26 | 1.88 | 2.08 | 2.25 | ns |
| SSTL18_II_F | 0.64 | 0.67 | 0.76 | 1.05 | 1.18 | 1.28 | 1.81 | 2.04 | 2.27 | ns |
| DIFF_SSTL135_F | 0.59 | 0.61 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| DIFF_SSTL15_F | 0.63 | 0.67 | 0.77 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| DIFF_SSTL18_I_F | 0.65 | 0.69 | 0.78 | 1.10 | 1.19 | 1.23 | 1.86 | 2.05 | 2.22 | ns |
| DIFF_SSTL18_II_F | 0.65 | 0.69 | 0.78 | 1.02 | 1.10 | 1.14 | 1.78 | 1.96 | 2.13 | ns |

**Notes:**

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

## Input Serializer/Deserializer Switching Characteristics

*Table 24:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Setup/Hold for Control Lines** | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.12 | 0.02/0.13 | 0.02/0.15 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.39/–0.02 | 0.44/–0.02 | 0.63/–0.02 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.12/0.29 | –0.12/0.31 | –0.12/0.35 | ns |
| **Setup/Hold for Data Lines** | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_D\_DDR}$ / $T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.11/0.11 | 0.12/0.12 | 0.15/0.15 | ns |
| **Sequential Delays** | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.46 | 0.47 | 0.58 | ns |
| **Propagation Delays** | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.09 | 0.10 | 0.12 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in the timing report.

*Table 27:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade |  |  | Units |
|---|---|---|---|---|---|
|  |  | -3 | -2/-2L/-2G | -1 |  |
| **IO_FIFO Clock to Out Delays** |  |  |  |  |  |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs | 0.51 | 0.56 | 0.63 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags | 0.59 | 0.62 | 0.81 | ns |
| **Setup/Hold** |  |  |  |  |  |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK | 0.43/–0.01 | 0.47/–0.01 | 0.53/–0.01 | ns |
| $T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$ | WREN to WRCLK | 0.39/–0.01 | 0.43/–0.01 | 0.50/–0.01 | ns |
| $T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK | 0.49/0.01 | 0.53/0.02 | 0.61/0.02 | ns |
| **Minimum Pulse Width** |  |  |  |  |  |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | ns |
| **Maximum Frequency** |  |  |  |  |  |
| $F_{MAX}$ | RDCLK and WRCLK | 533.05 | 470.37 | 400.00 | MHz |

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Sequential Delays** | | | | | |
| $T_{SHCKO}$[1] | Clock to A – B outputs | 0.68 | 0.70 | 0.85 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 0.91 | 0.95 | 1.15 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK | 0.45/0.23 | 0.45/0.24 | 0.54/0.27 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock | 0.13/0.50 | 0.14/0.50 | 0.17/0.58 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.40/0.16 | 0.42/0.17 | 0.52/0.23 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock | 0.29/0.09 | 0.30/0.09 | 0.36/0.09 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK | 0.29/0.09 | 0.30/0.09 | 0.37/0.09 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW}$ | Minimum pulse width | 0.68 | 0.77 | 0.91 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 1.35 | 1.54 | 1.82 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 30:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Sequential Delays** | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 0.96 | 0.98 | 1.20 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.19 | 1.23 | 1.50 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 0.89 | 0.91 | 1.10 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{WS\_SHFREG}/T_{WH\_SHFREG}$ | WE input | 0.26/0.09 | 0.27/0.09 | 0.33/0.09 | ns, Min |
| $T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$ | CE input to CLK | 0.27/0.09 | 0.28/0.09 | 0.33/0.09 | ns, Min |
| $T_{DS\_SHFREG}/T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.28/0.26 | 0.28/0.26 | 0.33/0.30 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.55 | 0.65 | 0.78 | ns, Min |

*Table 31:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM<br>(Write first and No change modes)<br>When not in SDP RF mode | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM<br>(Read first, Performance mode)<br>When in SDP RF mode but no address overlap between port A and port B | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM<br>(Read first, Delayed_write mode)<br>When in SDP RF mode and there is possibility of overlap between port A and port B addresses | 528.26 | 477.33 | 400.80 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM Cascade<br>(Write first, No change mode)<br>When cascade but not in RF mode | 551.27 | 493.83 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM Cascade<br>(Read first, Performance mode)<br>When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27 | 493.83 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 478.24 | 427.35 | 350.88 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 484.26 | 430.85 | 351.12 | MHz |

**Notes:**

1. The timing report shows all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

*Table 38:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| MMCM_T$_{LOCKMAX}$ | MMCM maximum Lock Time | 100 | 100 | 100 | µs |
| MMCM_F$_{OUTMAX}$ | MMCM maximum output frequency | 1066.00 | 933.00 | 800.00 | MHz |
| MMCM_F$_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_T$_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | |
| MMCM_RST$_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | ns |
| MMCM_F$_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | MHz |
| MMCM_F$_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_T$_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | |
| $T_{MMCMDCK\_PSEN}$/<br>$T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/<br>$T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | |
| $T_{MMCMDCK\_DADDR}$/<br>$T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DI}$/$T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DEN}$/$T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/$T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
   See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F$_{OUTMIN}$ is 0.036 MHz.

## Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 40:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2/-2L/-2G | -1 | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region) | XC7V585T | 5.63 | 6.20 | 6.97 | ns |
| | | XC7V2000T | N/A | 5.66 | 6.35 | ns |
| | | XC7VX330T | 5.41 | 5.97 | 6.71 | ns |
| | | XC7VX415T | 5.46 | 5.96 | 6.70 | ns |
| | | XC7VX485T | 5.29 | 5.84 | 6.57 | ns |
| | | XC7VX550T | 5.45 | 6.02 | 6.76 | ns |
| | | XC7VX690T | 5.46 | 6.02 | 6.76 | ns |
| | | XC7VX980T | N/A | 6.12 | 6.87 | ns |
| | | XC7VX1140T | N/A | 5.59 | 6.28 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

*Table 41:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2/-2L/-2G | -1 | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region) | XC7V585T | 6.81 | 7.53 | 8.44 | ns |
| | | XC7V2000T | N/A | 6.00 | 6.73 | ns |
| | | XC7VX330T | 6.31 | 6.97 | 7.83 | ns |
| | | XC7VX415T | 6.36 | 6.90 | 7.69 | ns |
| | | XC7VX485T | 6.20 | 6.86 | 7.69 | ns |
| | | XC7VX550T | 6.66 | 7.37 | 8.27 | ns |
| | | XC7VX690T | 6.69 | 7.37 | 8.27 | ns |
| | | XC7VX980T | N/A | 7.47 | 8.37 | ns |
| | | XC7VX1140T | N/A | 5.93 | 6.65 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

### *Table 47:* Clock-Capable Clock Input Setup and Hold With PLL

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2/-2L/-2G | -1 | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2) | | | | | | |
| $T_{PSPLLCC}$/<br>$T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(3) with PLL | XC7V585T | 3.07/–0.21 | 3.40/–0.21 | 3.72/–0.21 | ns |
| | | XC7V2000T | N/A | 2.99/–0.35 | 3.27/–0.35 | ns |
| | | XC7VX330T | 2.94/–0.26 | 3.26/–0.26 | 3.57/–0.26 | ns |
| | | XC7VX415T | 3.09/–0.10 | 3.42/–0.10 | 3.75/–0.10 | ns |
| | | XC7VX485T | 2.95/–0.26 | 3.26/–0.26 | 3.58/–0.26 | ns |
| | | XC7VX550T | 3.08/–0.20 | 3.40/–0.20 | 3.74/–0.20 | ns |
| | | XC7VX690T | 3.08/–0.10 | 3.40/–0.10 | 3.74/–0.10 | ns |
| | | XC7VX980T | N/A | 3.39/–0.21 | 3.72/–0.21 | ns |
| | | XC7VX1140T | N/A | 3.00/–0.35 | 3.27/–0.35 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

### *Table 48:* Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup/hold of I/O clock for HR I/O banks | –0.36/1.36 | –0.36/1.50 | –0.36/1.70 | ns |
| | Setup/hold of I/O clock for HP I/O banks | –0.34/1.39 | –0.34/1.53 | –0.34/1.73 | ns |

### *Table 49:* Sample Window

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.51 | 0.56 | 0.61 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.30 | 0.35 | 0.40 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

*Table 52:* **GTX Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

*Table 53:* **GTX Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3/-2G | -2/-2L | -1[1] | |
| $F_{GTXMAX}$[2] | Maximum GTX transceiver data rate | | 12.5 | 10.3125 | 8.0 | Gb/s |
| $F_{GTXMIN}$[2] | Minimum GTX transceiver data rate | | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTXCRANGE}$ | CPLL line rate range | 1 | 3.2–6.6 | | | Gb/s |
| | | 2 | 1.6–3.3 | | | Gb/s |
| | | 4 | 0.8–1.65 | | | Gb/s |
| | | 8 | 0.5–0.825 | | | Gb/s |
| | | 16 | N/A | | | Gb/s |
| $F_{GTXQRANGE1}$ | QPLL line rate range 1 | 1 | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | Gb/s |
| | | 2 | 2.965–4.0 | 2.965–4.0 | 2.965–4.0 | Gb/s |
| | | 4 | 1.4825–2.0 | 1.4825–2.0 | 1.4825–2.0 | Gb/s |
| | | 8 | 0.74125–1.0 | 0.74125–1.0 | 0.74125–1.0 | Gb/s |
| | | 16 | N/A | N/A | N/A | Gb/s |
| $F_{GTXQRANGE2}$ | QPLL line rate range 2[3] | 1 | 9.8–12.5 | 9.8–10.3125 | N/A | Gb/s |
| | | 2 | 4.9–6.25 | 4.9–5.15625 | N/A | Gb/s |
| | | 4 | 2.45–3.125 | 2.45–2.578125 | N/A | Gb/s |
| | | 8 | 1.225–1.5625 | 1.225–1.2890625 | N/A | Gb/s |
| | | 16 | 0.6125–0.78125 | 0.6125–0.64453125 | N/A | Gb/s |
| $F_{GCPLLRANGE}$ | GTX transceiver CPLL frequency range | | 1.6–3.3 | 1.6–3.3 | 1.6–3.3 | GHz |
| $F_{GQPLLRANGE1}$ | GTX transceiver QPLL frequency range 1 | | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | GHz |
| $F_{GQPLLRANGE2}$ | GTX transceiver QPLL frequency range 2 | | 9.8–12.5 | 9.8–10.3125 | N/A | GHz |

**Notes:**

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with $V_{CCINT}$ = 0.9V, as described in tge *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

*Table 54:* **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3/-2G | -2/-2L | -1 | |
| $F_{GTXDRPCLK}$ | GTXDRPCLK maximum frequency | 175.01 | 175.01 | 156.25 | MHz |

*Table 55:* **GTX Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | -3 speed grade | 60 | – | 700 | MHz |
| | | All other speed grades | 60 | – | 670 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

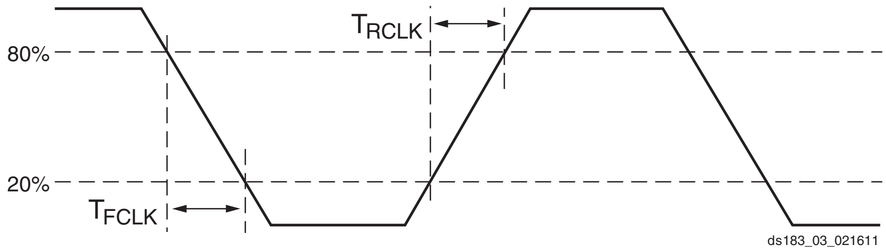

*Figure 3:* **Reference Clock Timing Parameters**

*Table 56:* **GTX Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 37 x$10^6$ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | 2.3 x$10^6$ | UI |

*Table 58:* **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $TJ_{6.6\_CPLL}$ | Total jitter(3)(4) | 6.6 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.6\_CPLL}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total jitter(3)(4) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total jitter(3)(4) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total jitter(3)(4) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $TJ_{3.20}$ | Total jitter(3)(4) | 3.20 Gb/s(5) | – | – | 0.20 | UI |
| $DJ_{3.20}$ | Deterministic jitter(3)(4) | | – | – | 0.10 | UI |
| $TJ_{3.20L}$ | Total jitter(3)(4) | 3.20 Gb/s(6) | – | – | 0.32 | UI |
| $DJ_{3.20L}$ | Deterministic jitter(3)(4) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total jitter(3)(4) | 2.5 Gb/s(7) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic jitter(3)(4) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total jitter(3)(4) | 1.25 Gb/s(8) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic jitter(3)(4) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total jitter(3)(4) | 500 Mb/s | – | – | 0.10 | UI |
| $DJ_{500}$ | Deterministic jitter(3)(4) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

# GTH Transceiver Specifications

## GTH Transceiver DC Input and Output Levels

Table 66 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

*Table 66:* **GTH Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled<br>$V_{MGTAVTT}$ = 1.2V | –400 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled<br>$V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to `1010` | – | – | 800 | mV |
| $V_{CMOUTDC}$ | Common mode output voltage: DC coupled | Equation based | $V_{MGTAVTT} – DV_{PPOUT}/4$ | | | mV |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | Equation based | $V_{MGTAVTT} – DV_{PPOUT}/2$ | | | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | – | 10 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

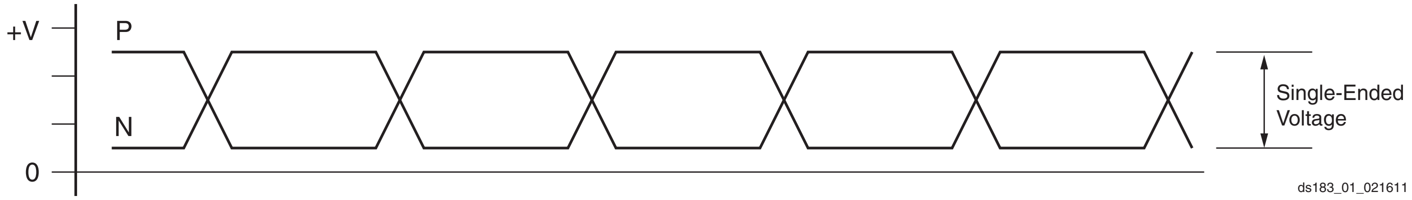

*Figure 4:* **Single-Ended Peak-to-Peak Voltage**

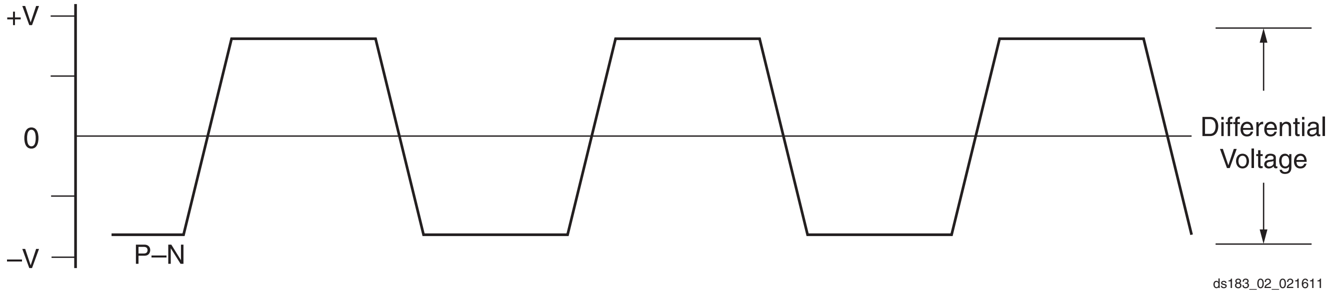

*Figure 5:* **Differential Peak-to-Peak Voltage**

*Table 70:* **GTH Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 820 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

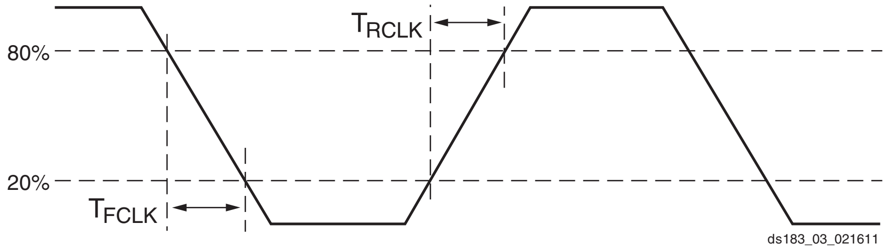

*Figure 6:* **Reference Clock Timing Parameters**

*Table 71:* **GTH Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 37 $\times10^6$ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | 2.3 $\times10^6$ | UI |

*Table 72:* **GTH Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Data Width Conditions | | Speed Grade | | | Units |
|---|---|---|---|---|---|---|---|
| | | Internal Logic | Interconnect Logic | -3E/-2GE(2) | -2(C&I)/-2LE(2) | -1(C&I)(3) | |
| $F_{TXOUT}$ | TXUSERCLKOUT maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| $F_{RXOUT}$ | RXUSERCLKOUT maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| $F_{TXIN}$ | TXUSERCLKIN maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| $F_{RXIN}$ | RXUSERCLKIN maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| $F_{TXIN2}$ | TXUSERCLKIN2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| | | 64-bit | 64-bit | 204.688 | 176.563 | 132.813 | MHz |
| $F_{RXIN2}$ | RXUSERCLKIN2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| | | 64-bit | 64-bit | 204.688 | 176.563 | 132.813 | MHz |

**Notes:**

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
3. For speed grade -1 (and when $V_{CCINT}$ = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

*Table 73:* **GTH Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTHTX}$ | Serial data rate range | | 0.500 | – | $F_{GTHMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 40 | – | ps |
| $T_{FTX}$ | TX fall time | 80%–20% | – | 40 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{13.1}$ | Total jitter(2)(4) | 13.1 Gb/s | – | – | 0.3 | UI |
| $DJ_{13.1}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{12.5}$ | Total jitter(2)(4) | 12.5 Gb/s | – | – | 0.28 | UI |
| $DJ_{12.5}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{11.3}$ | Total jitter(2)(4) | 11.3 Gb/s | – | – | 0.28 | UI |
| $DJ_{11.3}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{10.3125\_QPLL}$ | Total jitter(2)(4) | 10.3125 Gb/s | – | – | 0.28 | UI |
| $DJ_{10.3125\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{10.3125\_CPLL}$ | Total jitter(3)(4) | 10.3125 Gb/s | – | – | 0.33 | UI |
| $DJ_{10.3125\_CPLL}$ | Deterministic jitter(3)(4) | | – | – | 0.17 | UI |
| $TJ_{9.953}$ | Total jitter(2)(4) | 9.953 Gb/s | – | – | 0.28 | UI |
| $DJ_{9.953}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{9.8}$ | Total jitter(2)(4) | 9.8 Gb/s | – | – | 0.28 | UI |
| $DJ_{9.8}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{8.0\_QPLL}$ | Total jitter(2)(4) | 8.0 Gb/s | – | – | 0.28 | UI |
| $DJ_{8.0\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |

## XADC Specifications

*Table 82:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±3 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Offset calibration enabled | – | – | ±6 | LSBs |
| Gain Error | | Gain calibration disabled | – | – | ±0.5 | % |
| Offset Matching | | Offset calibration enabled | – | – | 4 | LSBs |
| Gain Matching | | Gain calibration disabled | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | – | 70 | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C. | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5%<br>$T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5%<br>$T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | cycle |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | cycle |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |
| DCLK Duty Cycle | | | 40 | – | 60 | % |