# AMD Xilinx - XC7VX690T-2FFG1157I Datasheet

**Welcome to** **E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 54150 |
| Number of Logic Elements/Cells | 693120 |
| Total RAM Bits | 54190080 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.03V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1157-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-2ffg1157i |

*Table 1:* **Absolute Maximum Ratings(1)** ***(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{MGTAVTTRCAL}$ | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column | –0.5 | 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.26 | V |
| $I_{DCIN}$ | DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| $I_{DCOUT}$ | DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies(6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies(6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
5. See Table 10 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475).

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | Internal supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4). | 0.87 | 0.90 | 0.93 | V |
| $V_{CCBRAM}$(3) | Block RAM supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4). | 0.87 | 0.90 | 1.03 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCO}$(5)(6) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| | Supply voltage for 1.8V HP I/O banks | 1.14 | – | 1.89 | V |
| $V_{CCAUX\_IO}$ | Auxiliary supply voltage when set to 1.8V | 1.71 | 1.80 | 1.89 | V |
| | Auxiliary supply voltage when set to 2.0V | 1.94 | 2.00 | 2.06 | V |
| $V_{IN}$(7) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.2 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(8) | –0.20 | – | 2.625 | V |
| $I_{IN}$(9) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(10) | Battery voltage | 1.0 | – | 1.89 | V |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions** ***(Cont'd)***

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$[3] | Battery supply current | – | – | 150 | nA |
| $R_{IN\_TERM}$[4] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}$/2 level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 5:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 100 |
| $V_{CCO}$ + 0.60 | 50.0 | –0.60 | 50.0 |
| $V_{CCO}$ + 0.65 | 50.0 | –0.65 | 50.0 |
| $V_{CCO}$ + 0.70 | 47.0 | –0.70 | 50.0 |
| $V_{CCO}$ + 0.75 | 21.2 | –0.75 | 50.0 |
| $V_{CCO}$ + 0.80 | 9.71 | –0.80 | 50.0 |
| $V_{CCO}$ + 0.85 | 4.51 | –0.85 | 28.4 |
| $V_{CCO}$ + 0.90 | 2.12 | –0.90 | 12.7 |
| $V_{CCO}$ + 0.95 | 1.01 | –0.95 | 5.79 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

*Table 6:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade |  |  | Units |
|---|---|---|---|---|---|---|
|  |  |  | -3 | -2/-2L/-2G | -1 |  |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7V585T | 1483 | 1483 | 1483 | mA |
|  |  | XC7V2000T | N/A | 3756 | 3756 | mA |
|  |  | XC7VX330T | 1012 | 1012 | 1012 | mA |
|  |  | XC7VX415T | 1324 | 1324 | 1324 | mA |
|  |  | XC7VX485T | 1578 | 1578 | 1578 | mA |
|  |  | XC7VX550T | 2214 | 2214 | 2214 | mA |
|  |  | XC7VX690T | 2214 | 2214 | 2214 | mA |
|  |  | XC7VX980T | N/A | 2580 | 2580 | mA |
|  |  | XC7VX1140T | N/A | 3448 | 3448 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7V585T | 1 | 1 | 1 | mA |
|  |  | XC7V2000T | N/A | 1 | 1 | mA |
|  |  | XC7VX330T | 1 | 1 | 1 | mA |
|  |  | XC7VX415T | 1 | 1 | 1 | mA |
|  |  | XC7VX485T | 1 | 1 | 1 | mA |
|  |  | XC7VX550T | 1 | 1 | 1 | mA |
|  |  | XC7VX690T | 1 | 1 | 1 | mA |
|  |  | XC7VX980T | N/A | 1 | 1 | mA |
|  |  | XC7VX1140T | N/A | 1 | 1 | mA |

*Table 6:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2/-2L/-2G | -1 | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7V585T | 114 | 114 | 114 | mA |
| | | XC7V2000T | N/A | 315 | 315 | mA |
| | | XC7VX330T | 73 | 73 | 73 | mA |
| | | XC7VX415T | 88 | 88 | 88 | mA |
| | | XC7VX485T | 104 | 104 | 104 | mA |
| | | XC7VX550T | 147 | 147 | 147 | mA |
| | | XC7VX690T | 147 | 147 | 147 | mA |
| | | XC7VX980T | N/A | 183 | 183 | mA |
| | | XC7VX1140T | N/A | 250 | 250 | mA |
| $I_{CCAUX\_IOQ}$ | Quiescent $V_{CCAUX\_IO}$ supply current | XC7V585T | 2 | 2 | 2 | mA |
| | | XC7V2000T | N/A | 2 | 2 | mA |
| | | XC7VX330T | 2 | 2 | 2 | mA |
| | | XC7VX415T | 2 | 2 | 2 | mA |
| | | XC7VX485T | 2 | 2 | 2 | mA |
| | | XC7VX550T | 2 | 2 | 2 | mA |
| | | XC7VX690T | 2 | 2 | 2 | mA |
| | | XC7VX980T | N/A | 2 | 2 | mA |
| | | XC7VX1140T | N/A | 2 | 2 | mA |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7V585T | 34 | 34 | 34 | mA |
| | | XC7V2000T | N/A | 56 | 56 | mA |
| | | XC7VX330T | 32 | 32 | 32 | mA |
| | | XC7VX415T | 38 | 38 | 38 | mA |
| | | XC7VX485T | 44 | 44 | 44 | mA |
| | | XC7VX550T | 63 | 63 | 63 | mA |
| | | XC7VX690T | 63 | 63 | 63 | mA |
| | | XC7VX980T | N/A | 65 | 65 | mA |
| | | XC7VX1140T | N/A | 81 | 81 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Table 7 shows the minimum current, in addition to $I_{CCQ}$, that is required by Virtex-7 T and XT devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after $V_{CCINT}$ is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

*Table 7:* **Power-On Current for Virtex-7 T and XT Devices**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCAUX\_IO}$ | $I_{CCBRAM}$ | Units |
|---|---|---|---|---|---|---|
| | Typ(1) | Typ(1) | Typ(1) | Typ(1) | Typ(1) | |
| XC7V585T | $I_{CCINTQ}$ + 2700 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 60 mA per bank | $I_{CCOAUXIOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 108 | mA |
| XC7V2000T | $I_{CCINTQ}$ + 4000 | $I_{CCAUXQ}$ + 80 | $I_{CCOQ}$ + 60 mA per bank | $I_{CCOAUXIOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 176 | mA |
| XC7VX330T | $I_{CCINTQ}$ + 1000 | $I_{CCAUXQ}$ + 65 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 95 | mA |
| XC7VX415T | $I_{CCINTQ}$ + 1200 | $I_{CCAUXQ}$ + 75 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 115 | mA |
| XC7VX485T | $I_{CCINTQ}$ + 1200 | $I_{CCAUXQ}$ + 80 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 140 | mA |
| XC7VX550T | $I_{CCINTQ}$ + 3300 | $I_{CCAUXQ}$ + 143 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 57 mA per bank | $I_{CCBRAMQ}$ + 200 | mA |
| XC7VX690T | $I_{CCINTQ}$ + 3300 | $I_{CCAUXQ}$ + 143 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 57 mA per bank | $I_{CCBRAMQ}$ + 200 | mA |
| XC7VX980T | $I_{CCINTQ}$ + 6500 | $I_{CCAUXQ}$ + 202 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 60 mA per bank | $I_{CCBRAMQ}$ + 204 | mA |
| XC7VX1140T | $I_{CCINTQ}$ + 8000 | $I_{CCAUXQ}$ + 235 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCOAUXIOQ}$ + 63 mA per bank | $I_{CCBRAMQ}$ + 256 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

*Table 8:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$ | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX\_IO}$ | Ramp time from GND to 90% of $V_{CCAUX\_IO}$ | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$ | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ | $T_J = 100°C$(1) | – | 500 | ms |
| | | $T_J = 85°C$(1) | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |
| $T_{MGTVCCAUX}$ | Ramp time from GND to 90% of $V_{MGTVCCAUX}$ | | 0.2 | 50 | ms |

**Notes:**

1. Based on 240,000 power cycles with nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with a worst case $V_{CCO}$ of 3.465V.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 as outlined in Table 14.

*Table 14:* **Virtex-7 T and XT FPGA Speed Specification Version By Device/Speed Grade**

| Version In: | | Typical $V_{CCINT}$ | Device |
|---|---|---|---|
| **ISE 14.5** | **Vivado 2013.1** | **(Table 2)** | |
| 1.09 | 1.09 | 1.0V | XC7V585T, XC7VX485T |
| N/A | 1.08 | 1.0V | XC7V2000T |
| 1.08 | 1.08 | 1.0V | XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T |
| N/A | 1.08 | 1.0V | XC7VX1140T |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### *Advance Product Specification*

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### *Preliminary Product Specification*

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### *Production Product Specification*

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

*Table 19:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | |
| HSTL_II_F | 0.61 | 0.64 | 0.73 | 1.05 | 1.18 | 1.28 | 1.81 | 2.04 | 2.27 | ns |
| HSTL_I_18_F | 0.64 | 0.67 | 0.76 | 1.05 | 1.18 | 1.28 | 1.81 | 2.04 | 2.27 | ns |
| HSTL_II_18_F | 0.64 | 0.67 | 0.76 | 1.03 | 1.14 | 1.23 | 1.79 | 2.00 | 2.22 | ns |
| DIFF_HSTL_I_F | 0.63 | 0.67 | 0.77 | 1.09 | 1.18 | 1.22 | 1.85 | 2.04 | 2.21 | ns |
| DIFF_HSTL_II_F | 0.63 | 0.67 | 0.77 | 1.02 | 1.11 | 1.14 | 1.78 | 1.97 | 2.13 | ns |
| DIFF_HSTL_I_18_F | 0.65 | 0.69 | 0.78 | 1.08 | 1.17 | 1.21 | 1.84 | 2.03 | 2.20 | ns |
| DIFF_HSTL_II_18_F | 0.65 | 0.69 | 0.78 | 1.01 | 1.10 | 1.13 | 1.77 | 1.96 | 2.12 | ns |
| LVCMOS33_S4 | 1.31 | 1.40 | 1.60 | 3.77 | 3.90 | 4.00 | 4.53 | 4.76 | 4.99 | ns |
| LVCMOS33_S8 | 1.31 | 1.40 | 1.60 | 3.49 | 3.62 | 3.72 | 4.25 | 4.48 | 4.71 | ns |
| LVCMOS33_S12 | 1.31 | 1.40 | 1.60 | 3.05 | 3.18 | 3.28 | 3.81 | 4.04 | 4.27 | ns |
| LVCMOS33_S16 | 1.31 | 1.40 | 1.60 | 3.06 | 3.43 | 3.88 | 3.82 | 4.29 | 4.87 | ns |
| LVCMOS33_F4 | 1.31 | 1.40 | 1.60 | 3.22 | 3.36 | 3.45 | 3.98 | 4.22 | 4.44 | ns |
| LVCMOS33_F8 | 1.31 | 1.40 | 1.60 | 2.71 | 2.84 | 2.93 | 3.47 | 3.70 | 3.92 | ns |
| LVCMOS33_F12 | 1.31 | 1.40 | 1.60 | 2.57 | 2.85 | 3.15 | 3.33 | 3.71 | 4.14 | ns |
| LVCMOS33_F16 | 1.31 | 1.40 | 1.60 | 2.44 | 2.69 | 2.96 | 3.20 | 3.55 | 3.95 | ns |
| LVCMOS25_S4 | 1.08 | 1.16 | 1.32 | 3.08 | 3.22 | 3.31 | 3.84 | 4.08 | 4.30 | ns |
| LVCMOS25_S8 | 1.08 | 1.16 | 1.32 | 2.85 | 2.98 | 3.07 | 3.61 | 3.84 | 4.06 | ns |
| LVCMOS25_S12 | 1.08 | 1.16 | 1.32 | 2.44 | 2.57 | 2.67 | 3.20 | 3.43 | 3.66 | ns |
| LVCMOS25_S16 | 1.08 | 1.16 | 1.32 | 2.79 | 2.92 | 3.01 | 3.55 | 3.78 | 4.00 | ns |
| LVCMOS25_F4 | 1.08 | 1.16 | 1.32 | 2.71 | 2.84 | 2.93 | 3.47 | 3.70 | 3.92 | ns |
| LVCMOS25_F8 | 1.08 | 1.16 | 1.32 | 2.14 | 2.28 | 2.37 | 2.90 | 3.14 | 3.36 | ns |
| LVCMOS25_F12 | 1.08 | 1.16 | 1.32 | 2.15 | 2.29 | 2.52 | 2.91 | 3.15 | 3.51 | ns |
| LVCMOS25_F16 | 1.08 | 1.16 | 1.32 | 1.92 | 2.17 | 2.45 | 2.68 | 3.03 | 3.44 | ns |
| LVCMOS18_S4 | 0.64 | 0.66 | 0.74 | 1.55 | 1.68 | 1.78 | 2.31 | 2.54 | 2.77 | ns |
| LVCMOS18_S8 | 0.64 | 0.66 | 0.74 | 2.14 | 2.28 | 2.37 | 2.90 | 3.14 | 3.36 | ns |
| LVCMOS18_S12 | 0.64 | 0.66 | 0.74 | 2.14 | 2.28 | 2.37 | 2.90 | 3.14 | 3.36 | ns |
| LVCMOS18_S16 | 0.64 | 0.66 | 0.74 | 1.49 | 1.62 | 1.72 | 2.25 | 2.48 | 2.71 | ns |
| LVCMOS18_S24(1) | 0.64 | 0.66 | 0.74 | 1.74 | 1.92 | 2.08 | 2.50 | 2.78 | 3.07 | ns |
| LVCMOS18_F4 | 0.64 | 0.66 | 0.74 | 1.38 | 1.51 | 1.61 | 2.14 | 2.37 | 2.60 | ns |
| LVCMOS18_F8 | 0.64 | 0.66 | 0.74 | 1.64 | 1.78 | 1.87 | 2.40 | 2.64 | 2.86 | ns |
| LVCMOS18_F12 | 0.64 | 0.66 | 0.74 | 1.64 | 1.78 | 1.87 | 2.40 | 2.64 | 2.86 | ns |
| LVCMOS18_F16 | 0.64 | 0.66 | 0.74 | 1.52 | 1.68 | 1.81 | 2.28 | 2.54 | 2.80 | ns |
| LVCMOS18_F24(1) | 0.64 | 0.66 | 0.74 | 1.34 | 1.46 | 1.55 | 2.10 | 2.32 | 2.54 | ns |
| LVCMOS15_S4 | 0.66 | 0.69 | 0.81 | 1.86 | 2.00 | 2.09 | 2.62 | 2.86 | 3.08 | ns |
| LVCMOS15_S8 | 0.66 | 0.69 | 0.81 | 2.05 | 2.18 | 2.28 | 2.81 | 3.04 | 3.27 | ns |
| LVCMOS15_S12 | 0.66 | 0.69 | 0.81 | 1.83 | 2.03 | 2.23 | 2.59 | 2.89 | 3.22 | ns |
| LVCMOS15_S16 | 0.66 | 0.69 | 0.81 | 1.76 | 1.95 | 2.13 | 2.52 | 2.81 | 3.12 | ns |

*Table 20:* **1.8V IOB High Performance (HP) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | |
| LVDS | 0.75 | 0.79 | 0.92 | 1.05 | 1.17 | 1.24 | 1.68 | 1.92 | 2.06 | ns |
| HSUL_12 | 0.69 | 0.72 | 0.82 | 1.65 | 1.84 | 2.05 | 2.29 | 2.59 | 2.87 | ns |
| DIFF_HSUL_12 | 0.69 | 0.72 | 0.82 | 1.65 | 1.84 | 2.05 | 2.29 | 2.59 | 2.87 | ns |
| HSTL_I_S | 0.68 | 0.72 | 0.82 | 1.15 | 1.28 | 1.38 | 1.79 | 2.03 | 2.20 | ns |
| HSTL_II_S | 0.68 | 0.72 | 0.82 | 1.05 | 1.17 | 1.26 | 1.69 | 1.93 | 2.08 | ns |
| HSTL_I_18_S | 0.70 | 0.72 | 0.82 | 1.12 | 1.24 | 1.34 | 1.75 | 2.00 | 2.16 | ns |
| HSTL_II_18_S | 0.70 | 0.72 | 0.82 | 1.06 | 1.18 | 1.26 | 1.70 | 1.94 | 2.08 | ns |
| HSTL_I_12_S | 0.68 | 0.72 | 0.82 | 1.14 | 1.27 | 1.37 | 1.78 | 2.02 | 2.20 | ns |
| HSTL_I_DCI_S | 0.68 | 0.72 | 0.82 | 1.11 | 1.23 | 1.33 | 1.74 | 1.99 | 2.15 | ns |
| HSTL_II_DCI_S | 0.68 | 0.72 | 0.82 | 1.05 | 1.17 | 1.26 | 1.69 | 1.93 | 2.08 | ns |
| HSTL_II_T_DCI_S | 0.70 | 0.72 | 0.82 | 1.15 | 1.28 | 1.38 | 1.78 | 2.03 | 2.20 | ns |
| HSTL_I_DCI_18_S | 0.70 | 0.72 | 0.82 | 1.11 | 1.23 | 1.33 | 1.74 | 1.99 | 2.15 | ns |
| HSTL_II_DCI_18_S | 0.70 | 0.72 | 0.82 | 1.05 | 1.16 | 1.24 | 1.69 | 1.92 | 2.06 | ns |
| HSTL_II _T_DCI_18_S | 0.70 | 0.72 | 0.82 | 1.11 | 1.23 | 1.33 | 1.74 | 1.99 | 2.15 | ns |
| DIFF_HSTL_I_S | 0.75 | 0.79 | 0.92 | 1.15 | 1.28 | 1.38 | 1.79 | 2.03 | 2.20 | ns |
| DIFF_HSTL_II_S | 0.75 | 0.79 | 0.92 | 1.05 | 1.17 | 1.26 | 1.69 | 1.93 | 2.08 | ns |
| DIFF_HSTL_I_DCI_S | 0.75 | 0.79 | 0.92 | 1.15 | 1.28 | 1.38 | 1.78 | 2.03 | 2.20 | ns |
| DIFF_HSTL_II_DCI_S | 0.75 | 0.79 | 0.92 | 1.05 | 1.17 | 1.26 | 1.69 | 1.93 | 2.08 | ns |
| DIFF_HSTL_I_18_S | 0.75 | 0.79 | 0.92 | 1.12 | 1.24 | 1.34 | 1.75 | 2.00 | 2.16 | ns |
| DIFF_HSTL_II_18_S | 0.75 | 0.79 | 0.92 | 1.06 | 1.18 | 1.26 | 1.70 | 1.94 | 2.08 | ns |
| DIFF_HSTL_I_DCI_18_S | 0.75 | 0.79 | 0.92 | 1.11 | 1.23 | 1.33 | 1.74 | 1.99 | 2.15 | ns |
| DIFF_HSTL_II_DCI_18_S | 0.75 | 0.79 | 0.92 | 1.05 | 1.16 | 1.24 | 1.69 | 1.92 | 2.06 | ns |
| DIFF_HSTL_II _T_DCI_18_S | 0.75 | 0.79 | 0.92 | 1.11 | 1.23 | 1.33 | 1.74 | 1.99 | 2.15 | ns |
| HSTL_I_F | 0.68 | 0.72 | 0.82 | 1.02 | 1.14 | 1.22 | 1.66 | 1.90 | 2.04 | ns |
| HSTL_II_F | 0.68 | 0.72 | 0.82 | 0.97 | 1.08 | 1.15 | 1.61 | 1.84 | 1.97 | ns |
| HSTL_I_18_F | 0.70 | 0.72 | 0.82 | 1.04 | 1.16 | 1.24 | 1.68 | 1.91 | 2.06 | ns |
| HSTL_II_18_F | 0.70 | 0.72 | 0.82 | 0.98 | 1.09 | 1.16 | 1.62 | 1.85 | 1.98 | ns |
| HSTL_I_12_F | 0.68 | 0.72 | 0.82 | 1.02 | 1.13 | 1.21 | 1.65 | 1.88 | 2.03 | ns |
| HSTL_I_DCI_F | 0.68 | 0.72 | 0.82 | 1.04 | 1.16 | 1.24 | 1.67 | 1.91 | 2.06 | ns |
| HSTL_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.97 | 1.08 | 1.15 | 1.61 | 1.84 | 1.97 | ns |
| HSTL_II_T_DCI_F | 0.70 | 0.72 | 0.82 | 1.02 | 1.14 | 1.22 | 1.66 | 1.90 | 2.04 | ns |
| HSTL_I_DCI_18_F | 0.70 | 0.72 | 0.82 | 1.04 | 1.16 | 1.24 | 1.67 | 1.91 | 2.06 | ns |
| HSTL_II_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.98 | 1.09 | 1.16 | 1.61 | 1.85 | 1.98 | ns |
| HSTL_II _T_DCI_18_F | 0.70 | 0.72 | 0.82 | 1.04 | 1.16 | 1.24 | 1.67 | 1.91 | 2.06 | ns |
| DIFF_HSTL_I_F | 0.75 | 0.79 | 0.92 | 1.02 | 1.14 | 1.22 | 1.66 | 1.90 | 2.04 | ns |
| DIFF_HSTL_II_F | 0.75 | 0.79 | 0.92 | 0.97 | 1.08 | 1.15 | 1.61 | 1.84 | 1.97 | ns |
| DIFF_HSTL_I_DCI_F | 0.75 | 0.79 | 0.92 | 1.02 | 1.14 | 1.22 | 1.66 | 1.90 | 2.04 | ns |
| DIFF_HSTL_II_DCI_F | 0.75 | 0.79 | 0.92 | 0.97 | 1.08 | 1.15 | 1.61 | 1.84 | 1.97 | ns |

*Table 20:* **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | |
| LVDCI_15 | 0.59 | 0.62 | 0.73 | 1.98 | 2.23 | 2.58 | 2.62 | 2.99 | 3.40 | ns |
| LVDCI_DV2_18 | 0.47 | 0.50 | 0.60 | 1.99 | 2.15 | 2.34 | 2.62 | 2.90 | 3.17 | ns |
| LVDCI_DV2_15 | 0.59 | 0.62 | 0.73 | 1.98 | 2.23 | 2.58 | 2.62 | 2.99 | 3.40 | ns |
| HSLVDCI_18 | 0.68 | 0.72 | 0.82 | 1.99 | 2.15 | 2.35 | 2.62 | 2.91 | 3.17 | ns |
| HSLVDCI_15 | 0.68 | 0.72 | 0.82 | 1.98 | 2.23 | 2.58 | 2.62 | 2.99 | 3.40 | ns |
| SSTL18_I_S | 0.68 | 0.72 | 0.82 | 1.02 | 1.15 | 1.24 | 1.66 | 1.90 | 2.07 | ns |
| SSTL18_II_S | 0.68 | 0.72 | 0.82 | 1.17 | 1.29 | 1.37 | 1.81 | 2.05 | 2.19 | ns |
| SSTL18_I_DCI_S | 0.68 | 0.72 | 0.82 | 0.92 | 1.06 | 1.17 | 1.56 | 1.82 | 1.99 | ns |
| SSTL18_II_DCI_S | 0.68 | 0.72 | 0.82 | 0.88 | 0.98 | 1.08 | 1.51 | 1.74 | 1.90 | ns |
| SSTL18_II_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.92 | 1.06 | 1.17 | 1.56 | 1.82 | 1.99 | ns |
| SSTL15_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.58 | 1.82 | 1.97 | ns |
| SSTL15_DCI_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.57 | 1.82 | 1.97 | ns |
| SSTL15_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.57 | 1.82 | 1.97 | ns |
| SSTL135_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.10 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| SSTL135_DCI_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.09 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| SSTL135_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.09 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| SSTL12_S | 0.69 | 0.72 | 0.82 | 0.96 | 1.09 | 1.18 | 1.60 | 1.84 | 2.00 | ns |
| SSTL12_DCI_S | 0.69 | 0.72 | 0.82 | 1.03 | 1.17 | 1.27 | 1.66 | 1.92 | 2.09 | ns |
| SSTL12_T_DCI_S | 0.69 | 0.72 | 0.82 | 1.03 | 1.17 | 1.27 | 1.66 | 1.92 | 2.09 | ns |
| DIFF_SSTL18_I_S | 0.75 | 0.79 | 0.92 | 1.02 | 1.15 | 1.24 | 1.66 | 1.90 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.75 | 0.79 | 0.92 | 1.17 | 1.29 | 1.37 | 1.81 | 2.05 | 2.19 | ns |
| DIFF_SSTL18_I_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.06 | 1.17 | 1.56 | 1.82 | 1.99 | ns |
| DIFF_SSTL18_II_DCI_S | 0.75 | 0.79 | 0.92 | 0.88 | 0.98 | 1.08 | 1.51 | 1.74 | 1.90 | ns |
| DIFF_SSTL18_II_T_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.06 | 1.17 | 1.56 | 1.82 | 1.99 | ns |
| DIFF_SSTL15_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.58 | 1.82 | 1.97 | ns |
| DIFF_SSTL15_DCI_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.57 | 1.82 | 1.97 | ns |
| DIFF_SSTL15_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.57 | 1.82 | 1.97 | ns |
| DIFF_SSTL135_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.10 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| DIFF_SSTL135_DCI_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.09 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| DIFF_SSTL135_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.97 | 1.09 | 1.19 | 1.60 | 1.85 | 2.01 | ns |
| DIFF_SSTL12_S | 0.69 | 0.72 | 0.82 | 0.96 | 1.09 | 1.18 | 1.60 | 1.84 | 2.00 | ns |
| DIFF_SSTL12_DCI_S | 0.69 | 0.72 | 0.82 | 1.03 | 1.17 | 1.27 | 1.66 | 1.92 | 2.09 | ns |
| DIFF_SSTL12_T_DCI_S | 0.69 | 0.72 | 0.82 | 1.03 | 1.17 | 1.27 | 1.66 | 1.92 | 2.09 | ns |
| SSTL18_I_F | 0.68 | 0.72 | 0.82 | 0.94 | 1.06 | 1.15 | 1.58 | 1.82 | 1.97 | ns |
| SSTL18_II_F | 0.68 | 0.72 | 0.82 | 0.97 | 1.09 | 1.16 | 1.61 | 1.84 | 1.99 | ns |
| SSTL18_I_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |
| SSTL18_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |
| SSTL18_II_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |

*Table 20:* **1.8V IOB High Performance (HP) Switching Characteristics** ***(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | -3 | -2/-2L/-2G | -1 | |
| SSTL15_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| SSTL135_F | 0.69 | 0.72 | 0.82 | 0.88 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.89 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.89 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| SSTL12_F | 0.69 | 0.72 | 0.82 | 0.88 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 1.03 | 1.11 | 1.54 | 1.79 | 1.93 | ns |
| SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 1.03 | 1.11 | 1.54 | 1.79 | 1.93 | ns |
| DIFF_SSTL18_I_F | 0.75 | 0.79 | 0.92 | 0.94 | 1.06 | 1.15 | 1.58 | 1.82 | 1.97 | ns |
| DIFF_SSTL18_II_F | 0.75 | 0.79 | 0.92 | 0.97 | 1.09 | 1.16 | 1.61 | 1.84 | 1.99 | ns |
| DIFF_SSTL18_I_DCI_F | 0.75 | 0.79 | 0.92 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |
| DIFF_SSTL18_II_DCI_F | 0.75 | 0.79 | 0.92 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |
| DIFF_SSTL18_II_T_DCI_F | 0.75 | 0.79 | 0.92 | 0.89 | 1.02 | 1.10 | 1.53 | 1.77 | 1.92 | ns |
| DIFF_SSTL15_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| DIFF_SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| DIFF_SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.89 | 1.01 | 1.09 | 1.53 | 1.77 | 1.91 | ns |
| DIFF_SSTL135_F | 0.69 | 0.72 | 0.82 | 0.88 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| DIFF_SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.89 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| DIFF_SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.89 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| DIFF_SSTL12_F | 0.69 | 0.72 | 0.82 | 0.88 | 1.00 | 1.08 | 1.52 | 1.76 | 1.90 | ns |
| DIFF_SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 1.03 | 1.11 | 1.54 | 1.79 | 1.93 | ns |
| DIFF_SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 1.03 | 1.11 | 1.54 | 1.79 | 1.93 | ns |

**Notes:**

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{IOTPHZ}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 21:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 0.76 | 0.86 | 0.99 | ns |
| $T_{IOIBUFDISABLE\_HR}$ | IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks | 1.72 | 1.89 | 2.14 | ns |
| $T_{IOIBUFDISABLE\_HP}$ | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 1.31 | 1.46 | 1.76 | ns |

## Input/Output Delay Switching Characteristics

*Table 26:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **IDELAYCTRL** | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to ready for IDELAYCTRL | 3.22 | 3.22 | 3.22 | µs |
| $F_{IDELAYCTRL\_REF}$ | Attribute REFCLK frequency = 200.0(1) | 200 | 200 | 200 | MHz |
| | Attribute REFCLK frequency = 300.0(1) | 300 | 300 | N/A | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum reset pulse width | 52.00 | 52.00 | 52.00 | ns |
| **IDELAY/ODELAY** | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY/ODELAY chain delay resolution | $1/(32 \times 2 \times F_{REF})$ | | | ps |
| $T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3) | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4) | ±9 | ±9 | ±9 | ps per tap |
| $T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IDELAY/ODELAY | 800 | 800 | 710 | MHz |
| $T_{IDCCK\_CE}$ / $T_{IDCKC\_CE}$ | CE pin setup/hold with respect to C for IDELAY | 0.11/0.10 | 0.14/0.12 | 0.18/0.14 | ns |
| $T_{ODCCK\_CE}$ / $T_{ODCKC\_CE}$ | CE pin setup/hold with respect to C for ODELAY | 0.14/0.03 | 0.16/0.04 | 0.19/0.05 | ns |
| $T_{IDCCK\_INC}$/ $T_{IDCKC\_INC}$ | INC pin setup/hold with respect to C for IDELAY | 0.10/0.14 | 0.12/0.16 | 0.14/0.20 | ns |
| $T_{ODCCK\_INC}$/ $T_{ODCKC\_INC}$ | INC pin setup/hold with respect to C for ODELAY | 0.10/0.07 | 0.12/0.08 | 0.13/0.09 | ns |
| $T_{IDCCK\_RST}$/ $T_{IDCKC\_RST}$ | RST pin setup/hold with respect to C for IDELAY | 0.13/0.08 | 0.14/0.10 | 0.16/0.12 | ns |
| $T_{ODCCK\_RST}$/ $T_{ODCKC\_RST}$ | RST pin setup/hold with respect to C for ODELAY | 0.16/0.04 | 0.19/0.06 | 0.24/0.08 | ns |
| $T_{IDDO\_IDATAIN}$ | Propagation delay through IDELAY | Note 5 | Note 5 | Note 5 | ps |
| $T_{ODDO\_ODATAIN}$ | Propagation delay through ODELAY | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Sequential Delays** | | | | | |
| $T_{SHCKO}$[1] | Clock to A – B outputs | 0.68 | 0.70 | 0.85 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 0.91 | 0.95 | 1.15 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK | 0.45/0.23 | 0.45/0.24 | 0.54/0.27 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock | 0.13/0.50 | 0.14/0.50 | 0.17/0.58 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.40/0.16 | 0.42/0.17 | 0.52/0.23 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock | 0.29/0.09 | 0.30/0.09 | 0.36/0.09 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK | 0.29/0.09 | 0.30/0.09 | 0.37/0.09 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW}$ | Minimum pulse width | 0.68 | 0.77 | 0.91 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 1.35 | 1.54 | 1.82 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 30:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Sequential Delays** | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 0.96 | 0.98 | 1.20 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.19 | 1.23 | 1.50 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 0.89 | 0.91 | 1.10 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{WS\_SHFREG}/T_{WH\_SHFREG}$ | WE input | 0.26/0.09 | 0.27/0.09 | 0.33/0.09 | ns, Min |
| $T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$ | CE input to CLK | 0.27/0.09 | 0.28/0.09 | 0.33/0.09 | ns, Min |
| $T_{DS\_SHFREG}/T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.28/0.26 | 0.28/0.26 | 0.33/0.30 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.55 | 0.65 | 0.78 | ns, Min |

## Block RAM and FIFO Switching Characteristics

*Table 31:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | |
| $T_{RCKO\_DO}$ and<br>$T_{RCKO\_DO\_REG}$(1) | Clock CLK to DOUT output (without output register)(2)(3) | 1.57 | 1.80 | 2.08 | ns, Max |
| | Clock CLK to DOUT output (with output register)(4)(5) | 0.54 | 0.63 | 0.75 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and<br>$T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)(2)(3) | 2.35 | 2.58 | 3.26 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)(4)(5) | 0.62 | 0.69 | 0.80 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and<br>$T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with Cascade (without output register)(2) | 2.21 | 2.45 | 2.80 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register)(4) | 0.98 | 1.08 | 1.24 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs(6) | 0.65 | 0.74 | 0.89 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs(7) | 0.79 | 0.87 | 0.98 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.66 | 0.72 | 0.80 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and<br>$T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register) | 2.17 | 2.38 | 3.01 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.57 | 0.65 | 0.76 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and<br>$T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.64 | 0.74 | 0.90 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.71 | 0.79 | 0.92 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{RCCK\_ADDRA}$/$T_{RCKC\_ADDRA}$ | ADDR inputs(8) | 0.38/0.27 | 0.42/0.28 | 0.48/0.31 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}$/<br>$T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode(9) | 0.49/0.51 | 0.55/0.53 | 0.63/0.57 | ns, Min |
| $T_{RDCK\_DI\_RF}$/$T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode(9) | 0.17/0.25 | 0.19/0.29 | 0.21/0.35 | ns, Min |
| $T_{RDCK\_DI\_ECC}$/$T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode(9) | 0.42/0.37 | 0.47/0.39 | 0.53/0.43 | ns, Min |
| $T_{RDCK\_DI\_ECCW}$/$T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only(9) | 0.79/0.37 | 0.87/0.39 | 0.99/0.43 | ns, Min |
| $T_{RDCK\_DI\_ECC\_FIFO}$/<br>$T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode(9) | 0.89/0.47 | 0.98/0.50 | 1.12/0.54 | ns, Min |
| $T_{RCCK\_INJECTBITERR}$/<br>$T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.49/0.30 | 0.55/0.31 | 0.63/0.34 | ns, Min |
| $T_{RCCK\_EN}$/$T_{RCKC\_EN}$ | Block RAM Enable (EN) input | 0.30/0.17 | 0.33/0.18 | 0.38/0.20 | ns, Min |
| $T_{RCCK\_REGCE}$/$T_{RCKC\_REGCE}$ | CE input of output register | 0.21/0.13 | 0.25/0.13 | 0.31/0.14 | ns, Min |
| $T_{RCCK\_RSTREG}$/$T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.25/0.06 | 0.27/0.06 | 0.29/0.06 | ns, Min |
| $T_{RCCK\_RSTRAM}$/$T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.27/0.35 | 0.29/0.37 | 0.31/0.39 | ns, Min |
| $T_{RCCK\_WEA}$/$T_{RCKC\_WEA}$ | Write Enable (WE) input (Block RAM only) | 0.38/0.15 | 0.41/0.16 | 0.46/0.17 | ns, Min |
| $T_{RCCK\_WREN}$/$T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.39/0.25 | 0.39/0.30 | 0.40/0.37 | ns, Min |
| $T_{RCCK\_RDEN}$/$T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.36/0.26 | 0.36/0.30 | 0.37/0.37 | ns, Min |
| **Reset Delays** | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.76 | 0.83 | 0.93 | ns, Max |
| $T_{RREC\_RST}$/$T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.59/–0.68 | 1.76/–0.68 | 2.01/–0.68 | ns, Max |

*Table 31:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2/-2L/-2G | -1 | |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM<br>(Write first and No change modes)<br>When not in SDP RF mode | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM<br>(Read first, Performance mode)<br>When in SDP RF mode but no address overlap between port A and port B | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM<br>(Read first, Delayed_write mode)<br>When in SDP RF mode and there is possibility of overlap between port A and port B addresses | 528.26 | 477.33 | 400.80 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM Cascade<br>(Write first, No change mode)<br>When cascade but not in RF mode | 551.27 | 493.83 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM Cascade<br>(Read first, Performance mode)<br>When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27 | 493.83 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 478.24 | 427.35 | 350.88 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 484.26 | 430.85 | 351.12 | MHz |

**Notes:**

1. The timing report shows all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 32:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade |  |  | Units |
|---|---|---|---|---|---|
|  |  | -3 | -2/-2L/-2G | -1 |  |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** |  |  |  |  |  |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.24/0.12 | 0.27/0.14 | 0.31/0.16 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.28/0.13 | 0.32/0.14 | 0.39/0.15 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.15/0.15 | 0.17/0.17 | 0.20/0.20 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.21/0.19 | 0.27/0.22 | 0.35/0.26 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.21/0.12 | 0.24/0.14 | 0.27/0.16 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.22/0.13 | 0.25/0.14 | 0.30/0.15 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** |  |  |  |  |  |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$ | {A, B,} input to M register CLK using multiplier | 2.04/–0.01 | 2.34/–0.01 | 2.79/–0.01 | ns |
| $T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$ | {A, D} input to AD register CLK | 1.09/–0.02 | 1.25/–0.02 | 1.49/–0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** |  |  |  |  |  |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$ | {A, B,} input to P register CLK using multiplier | 3.41/–0.24 | 3.90/–0.24 | 4.64/–0.24 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.33/–0.62 | 3.81/–0.62 | 4.53/–0.62 | ns |
| $T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$ | A or B input to P register CLK not using multiplier | 1.47/–0.24 | 1.68/–0.24 | 2.00/–0.24 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.30/–0.22 | 1.49/–0.22 | 1.78/–0.22 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.12/–0.13 | 1.28/–0.13 | 1.52/–0.13 | ns |
| **Setup and Hold Times of the CE Pins** |  |  |  |  |  |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.30/0.05 | 0.36/0.06 | 0.44/0.09 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/$T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.24/0.08 | 0.29/0.09 | 0.36/0.11 | ns |
| $T_{DSPDCK\_CED\_DREG}$/$T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.31/–0.02 | 0.36/–0.02 | 0.44/–0.02 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/$T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.26/0.15 | 0.29/0.17 | 0.33/0.20 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.31/0.01 | 0.36/0.01 | 0.45/0.01 | ns |
| **Setup and Hold Times of the RST Pins** |  |  |  |  |  |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.34/0.10 | 0.39/0.11 | 0.47/0.13 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/$T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.06/0.22 | 0.07/0.24 | 0.08/0.26 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/$T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.37/0.06 | 0.42/0.06 | 0.50/0.07 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/$T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.18/0.18 | 0.20/0.21 | 0.23/0.24 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/$T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.24/0.01 | 0.26/0.01 | 0.30/0.01 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** |  |  |  |  |  |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier | 3.21 | 3.69 | 4.39 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier | 3.15 | 3.61 | 4.30 | ns |

*Table 38:* **MMCM Specification *(Cont'd)***

| **Symbol** | **Description** | **Speed Grade** | | | **Units** |
|---|---|---|---|---|---|
| | | **-3** | **-2/-2L/-2G** | **-1** | |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum Lock Time | 100 | 100 | 100 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency | 1066.00 | 933.00 | 800.00 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DI}$/$T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DEN}$/$T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/$T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

*Table 52:* **GTX Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

*Table 53:* **GTX Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3/-2G | -2/-2L | -1(1) | |
| $F_{GTXMAX}$(2) | Maximum GTX transceiver data rate | | 12.5 | 10.3125 | 8.0 | Gb/s |
| $F_{GTXMIN}$(2) | Minimum GTX transceiver data rate | | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTXCRANGE}$ | CPLL line rate range | 1 | 3.2–6.6 | | | Gb/s |
| | | 2 | 1.6–3.3 | | | Gb/s |
| | | 4 | 0.8–1.65 | | | Gb/s |
| | | 8 | 0.5–0.825 | | | Gb/s |
| | | 16 | N/A | | | Gb/s |
| $F_{GTXQRANGE1}$ | QPLL line rate range 1 | 1 | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | Gb/s |
| | | 2 | 2.965–4.0 | 2.965–4.0 | 2.965–4.0 | Gb/s |
| | | 4 | 1.4825–2.0 | 1.4825–2.0 | 1.4825–2.0 | Gb/s |
| | | 8 | 0.74125–1.0 | 0.74125–1.0 | 0.74125–1.0 | Gb/s |
| | | 16 | N/A | N/A | N/A | Gb/s |
| $F_{GTXQRANGE2}$ | QPLL line rate range 2(3) | 1 | 9.8–12.5 | 9.8–10.3125 | N/A | Gb/s |
| | | 2 | 4.9–6.25 | 4.9–5.15625 | N/A | Gb/s |
| | | 4 | 2.45–3.125 | 2.45–2.578125 | N/A | Gb/s |
| | | 8 | 1.225–1.5625 | 1.225–1.2890625 | N/A | Gb/s |
| | | 16 | 0.6125–0.78125 | 0.6125–0.64453125 | N/A | Gb/s |
| $F_{GCPLLRANGE}$ | GTX transceiver CPLL frequency range | | 1.6–3.3 | 1.6–3.3 | 1.6–3.3 | GHz |
| $F_{GQPLLRANGE1}$ | GTX transceiver QPLL frequency range 1 | | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | GHz |
| $F_{GQPLLRANGE2}$ | GTX transceiver QPLL frequency range 2 | | 9.8–12.5 | 9.8–10.3125 | N/A | GHz |

**Notes:**

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with $V_{CCINT}$ = 0.9V, as described in tge *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

*Table 54:* **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3/-2G | -2/-2L | -1 | |
| $F_{GTXDRPCLK}$ | GTXDRPCLK maximum frequency | 175.01 | 175.01 | 156.25 | MHz |

*Table 59:* **GTX Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| JT_SJ$_{12.5}$ | Sinusoidal jitter (QPLL)(3) | 12.5 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{11.18}$ | Sinusoidal jitter (QPLL)(3) | 11.18 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{10.32}$ | Sinusoidal jitter (QPLL)(3) | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{9.95}$ | Sinusoidal jitter (QPLL)(3) | 9.95 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{9.8}$ | Sinusoidal jitter (QPLL)(3) | 9.8 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{8.0}$ | Sinusoidal jitter (QPLL)(3) | 8.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{6.6\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 6.6 Gb/s | 0.48 | – | – | UI |
| JT_SJ$_{6.6\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{5.0}$ | Sinusoidal jitter (CPLL)(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{4.25}$ | Sinusoidal jitter (CPLL)(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{3.75}$ | Sinusoidal jitter (CPLL)(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{3.2}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| JT_SJ$_{3.2L}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| JT_SJ$_{2.5}$ | Sinusoidal jitter (CPLL)(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| JT_SJ$_{1.25}$ | Sinusoidal jitter (CPLL)(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| JT_SJ$_{500}$ | Sinusoidal jitter (CPLL)(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| JT_TJSE$_{3.2}$ | Total jitter with stressed eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| JT_TJSE$_{6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| JT_SJSE$_{3.2}$ | Sinusoidal jitter with stressed eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| JT_SJSE$_{6.6}$ | | 6.6 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 67 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

*Table 67:* **GTH Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTH Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

*Table 68:* **GTH Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3E/-2GE | -2(C&I)/-2LE | -1(C&I)[1] | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | | 13.1 | 11.3 | 8.5 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate | | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTHCRANGE}$ | CPLL line rate range | 1 | 3.2–10.3125 | | 3.2–8.0 | Gb/s |
| | | 2 | 1.6–5.16 | | 1.6–4.0 | Gb/s |
| | | 4 | 0.8–2.58 | | 0.8–2.0 | Gb/s |
| | | 8 | 0.5–1.29 | | 0.5–1.0 | Gb/s |
| | | 16 | N/A | | | Gb/s |
| $F_{GTHQRANGE1}$ | QPLL line rate range 1 | 1 | 8.0–11.85 | 8.0–11.3 | 8.0–8.5 | Gb/s |
| | | 2 | 4.0–5.925 | 4.0–5.65 | 4.0–4.25 | Gb/s |
| | | 4 | 2.0–2.9625 | 2.0–2.825 | 2.0–2.125 | Gb/s |
| | | 8 | 1.0–1.48125 | 1.0–1.4125 | 1.0–1.0625 | Gb/s |
| | | 16 | N/A | | | Gb/s |
| $F_{GTHQRANGE2}$ | QPLL line rate range 2 | 1 | 11.85–13.1 | N/A | | Gb/s |
| | | 2 | 5.925–6.55 | N/A | | Gb/s |
| | | 4 | 2.96–3.275 | N/A | | Gb/s |
| | | 8 | 1.48–1.63 | N/A | | Gb/s |
| | | 16 | 0.74–0.81 | N/A | | Gb/s |
| $F_{GCPLLRANGE}$ | GTH transceiver CPLL frequency range | | 1.6–5.16 | | 1.6–4.0 | GHz |
| $F_{GQPLLRANGE1}$ | GTH transceiver QPLL frequency range 1 | | 8.0–11.85 | 8.0–11.3 | 8.0–8.5 | GHz |
| $F_{GQPLLRANGE2}$ | GTH transceiver QPLL frequency range 2 | | 11.85–13.1 | N/A | | GHz |

**Notes:**

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with $V_{CCINT}$ = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.

*Table 69:* **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3/-2G | -2L | -2 | -1 | |
| $F_{GTHDRPCLK}$ | GTHDRPCLK maximum frequency | 175 | 175 | 175 | 156 | MHz |

*Table 74:* **GTH Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTHRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTHMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| JT_SJ$_{13.1}$ | Sinusoidal jitter (QPLL)(3) | 13.1 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{12.5}$ | Sinusoidal jitter (QPLL)(3) | 12.5 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{11.3}$ | Sinusoidal jitter (QPLL)(3) | 11.3 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{10.32\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{10.32\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{9.8}$ | Sinusoidal jitter (QPLL)(3) | 9.8 Gb/s | 0.3 | – | – | UI |
| JT_SJ$_{8.0\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 8.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{8.0\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 8.0 Gb/s | 0.42 | – | – | UI |
| JT_SJ$_{6.6\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 6.6 Gb/s | 0.48 | – | – | UI |
| JT_SJ$_{6.6\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{5.0}$ | Sinusoidal jitter (CPLL)(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{4.25}$ | Sinusoidal jitter (CPLL)(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{3.75}$ | Sinusoidal jitter (CPLL)(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| JT_SJ$_{3.2}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| JT_SJ$_{3.2L}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| JT_SJ$_{2.5}$ | Sinusoidal jitter (CPLL)(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| JT_SJ$_{1.25}$ | Sinusoidal jitter (CPLL)(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| JT_SJ$_{500}$ | Sinusoidal jitter (CPLL)(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| JT_TJSE$_{3.2}$ | Total jitter with stressed eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| JT_TJSE$_{6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| JT_SJSE$_{3.2}$ | Sinusoidal jitter with stressed eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| JT_SJSE$_{6.6}$ | | 6.6 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 1e$^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.