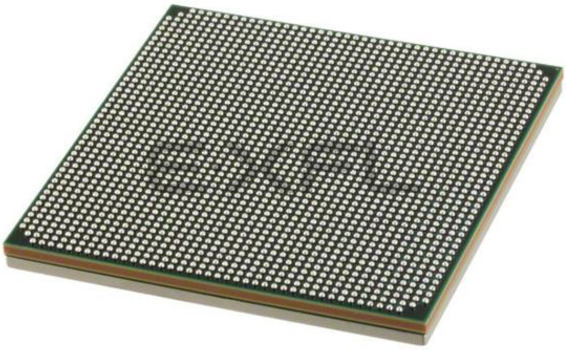

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	54150
Number of Logic Elements/Cells	693120
Total RAM Bits	54190080
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1926-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-2ffg1926i

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} – V_{MGTAVCC}$ > 150 mV and $V_{MGTAVCC}$ < 0.7V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} – V_{CCINT}$ > 150 mV and V_{CCINT} < 0.7V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **SelectIO DC Input and Output Levels[1][2]**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	13.0	–13.0
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	13.0	–13.0
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.600	$V_{CCO}/2$ + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} [(1)]			V_{ID} [(2)]			V_{OCM} [(3)]			V_{OD} [(4)]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} [(1)]			V_{ID} [(2)]		V_{OL} [(3)]	V_{OH} [(4)]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 as outlined in Table 14.

Table 14: **Virtex-7 T and XT FPGA Speed Specification Version By Device/Speed Grade**

Version In:		Typical V_{CCINT}	Device
ISE 14.5	Vivado 2013.1	(Table 2)	
1.09	1.09	1.0V	XC7V585T, XC7VX485T
N/A	1.08	1.0V	XC7V2000T
1.08	1.08	1.0V	XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T
N/A	1.08	1.0V	XC7VX1140T

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 12. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator[(1)(2)]**

<table>
<tr><th rowspan="2">Memory Standard</th><th rowspan="2">I/O Bank Type</th><th rowspan="2">V_{CCAUX_IO}</th><th colspan="3">Speed Grade</th><th rowspan="2">Units</th></tr>
<tr><th>-3</th><th>-2/-2L/-2G</th><th>-1</th></tr>
<tr><td colspan="7">4:1 Memory Controllers</td></tr>
<tr><td rowspan="3">DDR3</td><td>HP</td><td>2.0V</td><td>1866</td><td>1866</td><td>1600</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>1600</td><td>1333</td><td>1066</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td rowspan="3">DDR3L</td><td>HP</td><td>2.0V</td><td>1600</td><td>1600</td><td>1333</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>1333</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>800</td><td>800</td><td>667</td><td>Mb/s</td></tr>
<tr><td rowspan="3">DDR2</td><td>HP</td><td>2.0V</td><td>800</td><td>800</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>800</td><td>800</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>800</td><td>800</td><td>800</td><td>Mb/s</td></tr>
<tr><td rowspan="3">RLDRAM III</td><td>HP</td><td>2.0V</td><td>800</td><td>667</td><td>667</td><td>MHz</td></tr>
<tr><td>HP</td><td>1.8V</td><td>550</td><td>500</td><td>450</td><td>MHz</td></tr>
<tr><td>HR</td><td>N/A</td><td colspan="4">N/A</td></tr>
<tr><td colspan="7">2:1 Memory Controllers</td></tr>
<tr><td rowspan="3">DDR3</td><td>HP</td><td>2.0V</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td rowspan="3">DDR3L</td><td>HP</td><td>2.0V</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>1066</td><td>1066</td><td>800</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>800</td><td>800</td><td>667</td><td>Mb/s</td></tr>
<tr><td rowspan="3">DDR2</td><td>HP</td><td>2.0V</td><td rowspan="3">800</td><td rowspan="3">800</td><td rowspan="3">800</td><td rowspan="3">Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td></tr>
<tr><td>HR</td><td>N/A</td></tr>
<tr><td rowspan="3">QDR II+[(3)]</td><td>HP</td><td>2.0V</td><td rowspan="2">550</td><td rowspan="2">500</td><td rowspan="2">450</td><td rowspan="2">MHz</td></tr>
<tr><td>HP</td><td>1.8V</td></tr>
<tr><td>HR</td><td>N/A</td><td>500</td><td>450</td><td>400</td><td>MHz</td></tr>
<tr><td rowspan="3">RLDRAM II</td><td>HP</td><td>2.0V</td><td rowspan="3">533</td><td rowspan="3">500</td><td rowspan="3">450</td><td rowspan="3">MHz</td></tr>
<tr><td>HP</td><td>1.8V</td></tr>
<tr><td>HR</td><td>N/A</td></tr>
<tr><td rowspan="3">LPDDR2</td><td>HP</td><td>2.0V</td><td>667</td><td>667</td><td>667</td><td>Mb/s</td></tr>
<tr><td>HP</td><td>1.8V</td><td>667</td><td>667</td><td>667</td><td>Mb/s</td></tr>
<tr><td>HR</td><td>N/A</td><td>667</td><td>667</td><td>667</td><td>Mb/s</td></tr>
</table>

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25(1)	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25(1)	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25(1)	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33(1)	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3(1)	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVCMOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVCMOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVCMOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVCMOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVCMOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVCMOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVCMOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVCMOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVCMOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVCMOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVCMOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVCMOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVCMOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVCMOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVCMOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVCMOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVCMOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVCMOS18_S24[(1)]	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVCMOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVCMOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVCMOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVCMOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVCMOS18_F24[(1)]	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVCMOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVCMOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVCMOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVCMOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVCMOS15_F4	0.66	0.69	0.81	1.63	1.76	1.86	2.39	2.62	2.85	ns
LVCMOS15_F8	0.66	0.69	0.81	1.79	1.99	2.18	2.55	2.85	3.17	ns
LVCMOS15_F12	0.66	0.69	0.81	1.40	1.54	1.65	2.16	2.40	2.64	ns
LVCMOS15_F16	0.66	0.69	0.81	1.37	1.51	1.61	2.13	2.37	2.60	ns
LVCMOS12_S4	0.88	0.91	1.00	2.53	2.67	2.76	3.29	3.53	3.75	ns
LVCMOS12_S8	0.88	0.91	1.00	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVCMOS12_S12(1)	0.88	0.91	1.00	1.75	1.89	1.98	2.51	2.75	2.97	ns
LVCMOS12_F4	0.88	0.91	1.00	1.94	2.07	2.17	2.70	2.93	3.16	ns
LVCMOS12_F8	0.88	0.91	1.00	1.50	1.64	1.73	2.26	2.50	2.72	ns
LVCMOS12_F12(1)	0.88	0.91	1.00	1.54	1.71	1.87	2.30	2.57	2.86	ns
SSTL135_S	0.61	0.64	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
SSTL15_S	0.61	0.64	0.73	1.24	1.37	1.47	2.00	2.23	2.46	ns
SSTL18_I_S	0.64	0.67	0.76	1.59	1.74	1.85	2.35	2.60	2.84	ns
SSTL18_II_S	0.64	0.67	0.76	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL135_S	0.59	0.61	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL15_S	0.63	0.67	0.77	1.24	1.37	1.47	2.00	2.23	2.46	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	1.50	1.63	1.72	2.26	2.49	2.71	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	1.13	1.22	1.25	1.89	2.08	2.24	ns
SSTL135_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL15_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL18_I_F	0.64	0.67	0.76	1.12	1.22	1.26	1.88	2.08	2.25	ns
SSTL18_II_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
DIFF_SSTL135_F	0.59	0.61	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL15_F	0.63	0.67	0.77	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	1.10	1.19	1.23	1.86	2.05	2.22	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	1.02	1.10	1.14	1.78	1.96	2.13	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{SHCKO}[(1)]	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/T_{WH\_SHFREG}$	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
$T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
$T_{DS\_SHFREG}/T_{DH\_SHFREG}$	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

Table 32: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK (DREG) to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK (CREG) to CARRYCASCOUT output	1.64	1.88	2.23	ns
Maximum Frequency					
F_{MAX}	With all registers used	741.84	650.20	547.95	MHz
F_{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	412.20	360.75	303.77	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	468.82	408.66	342.70	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	468.82	408.66	342.58	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	MHz

PLL Switching Characteristics

Table 39: **PLL Specification**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
PLL_F_{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	MHz
$PLL\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	MHz
$PLL\_F_{BANDWIDTH}$	Low PLL bandwidth at typical[(1)]	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical[(1)]	4.00	4.00	4.00	MHz
$PLL\_T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs[(2)]	0.12	0.12	0.12	ns
$PLL\_T_{OUTJITTER}$	PLL output jitter	Note 3			
$PLL\_T_{OUTDUTY}$	PLL output clock duty cycle precision[(4)]	0.20	0.20	0.20	ns
$PLL\_T_{LOCKMAX}$	PLL maximum lock time	100	100	100	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	1066.00	933.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency[(5)]	6.25	6.25	6.25	MHz
$PLL\_T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
$PLL\_RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	MHz
$PLL\_T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
$T_{PLLDCK\_DADDR}/T_{PLLCKD\_DADDR}$	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{PLLDCK\_DI}/T_{PLLCKD\_DI}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{PLLDCK\_DEN}/T_{PLLCKD\_DEN}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
$T_{PLLDCK\_DWE}/T_{PLLCKD\_DWE}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
   See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Table 47: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL	XC7V585T	3.07/–0.21	3.40/–0.21	3.72/–0.21	ns
		XC7V2000T	N/A	2.99/–0.35	3.27/–0.35	ns
		XC7VX330T	2.94/–0.26	3.26/–0.26	3.57/–0.26	ns
		XC7VX415T	3.09/–0.10	3.42/–0.10	3.75/–0.10	ns
		XC7VX485T	2.95/–0.26	3.26/–0.26	3.58/–0.26	ns
		XC7VX550T	3.08/–0.20	3.40/–0.20	3.74/–0.20	ns
		XC7VX690T	3.08/–0.10	3.40/–0.10	3.74/–0.10	ns
		XC7VX980T	N/A	3.39/–0.21	3.72/–0.21	ns
		XC7VX1140T	N/A	3.00/–0.35	3.27/–0.35	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: **Sample Window**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{SAMP}	Sampling error at receiver pins(1)	0.51	0.56	0.61	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.30	0.35	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC specifications of the GTX transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 51: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} – DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor[2]		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

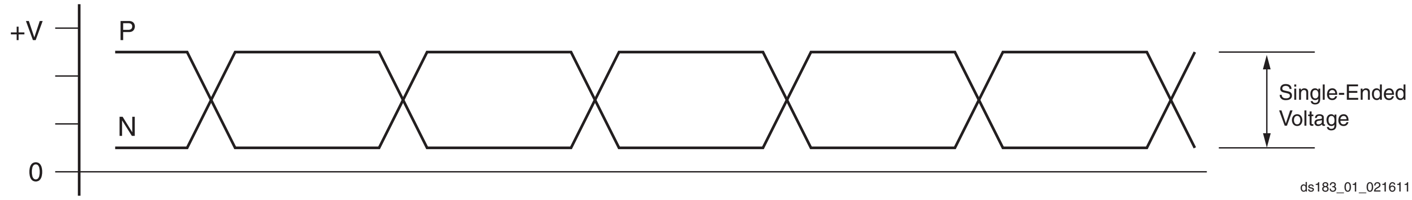

Figure 1: **Single-Ended Peak-to-Peak Voltage**

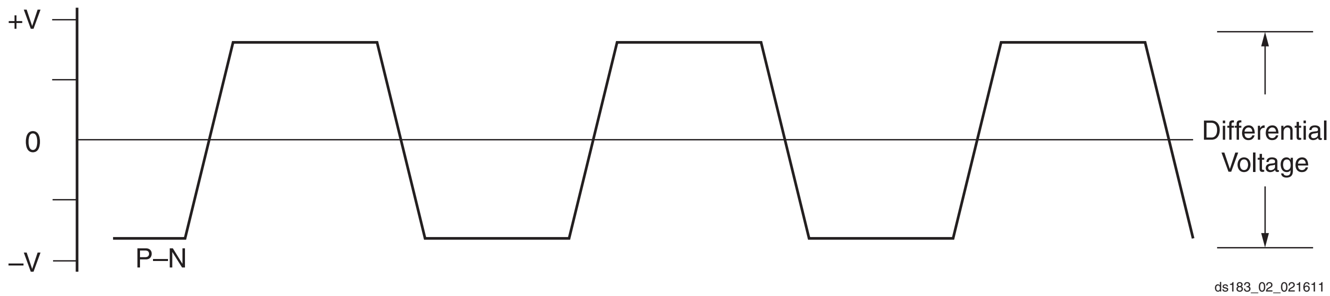

Figure 2: **Differential Peak-to-Peak Voltage**

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 52: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

Table 53: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1[1]	
F_{GTXMAX}[2]	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F_{GTXMIN}[2]	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[3]	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in tge *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 57: **GTX Transceiver User Clock Switching Characteristics[1][2]**

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G[3]	-2/-2L[3]	-1[4]	
F_{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F_{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total jitter[2][4]	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic jitter[2][4]		–	–	0.17	UI
$TJ_{11.18}$	Total jitter[2][4]	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic jitter[2][4]		–	–	0.17	UI
$TJ_{10.3125}$	Total jitter[2][4]	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125}$	Deterministic jitter[2][4]		–	–	0.17	UI
$TJ_{9.953}$	Total jitter[2][4]	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic jitter[2][4]		–	–	0.17	UI
$TJ_{9.8}$	Total jitter[2][4]	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic jitter[2][4]		–	–	0.17	UI
$TJ_{8.0}$	Total jitter[2][4]	8.0 Gb/s	–	–	0.30	UI
$DJ_{8.0}$	Deterministic jitter[2][4]		–	–	0.15	UI
$TJ_{6.6\_QPLL}$	Total jitter[2][4]	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI

Table 70: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

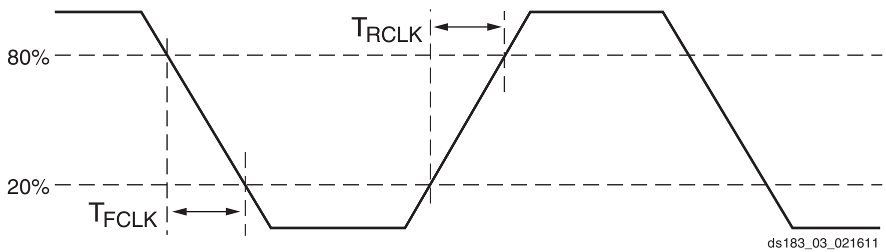

Figure 6: **Reference Clock Timing Parameters**

Table 71: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10^6	UI

XADC Specifications

Table 82: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSB (at 10 bits)
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%