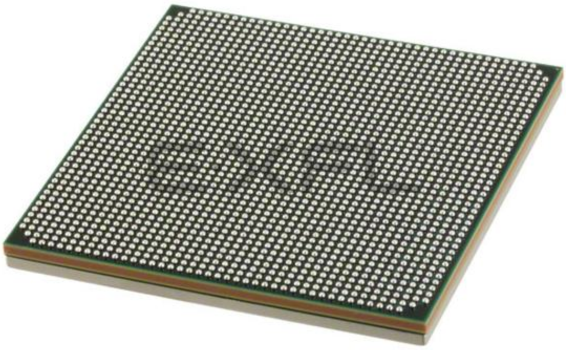
AMD Xilinx - XC7VX690T-3FFG1926E Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	54150
Number of Logic Elements/Cells	693120
Total RAM Bits	54190080
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1926-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-3ffg1926e

Table 1: **Absolute Maximum Ratings(1)** ***(Cont'd)***

Symbol	Description	Min	Max	Units
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
I_{DCOUT}	DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(6)	–	+260	°C
T_j	Maximum junction temperature(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
5. See Table 10 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}(3)	Internal supply voltage	0.97	1.00	1.03	V
	Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4).	0.87	0.90	0.93	V
V_{CCBRAM}(3)	Block RAM supply voltage	0.97	1.00	1.03	V
	Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical(4).	0.87	0.90	1.03	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCO}(5)(6)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN}(7)	I/O input voltage	–0.20	–	V_{CCO} + 0.2	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.20	–	2.625	V
I_{IN}(9)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(10)	Battery voltage	1.0	–	1.89	V

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 12. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
4:1 Memory Controllers						
DDR3	HP	2.0V	1866	1866	1600	Mb/s
	HP	1.8V	1600	1333	1066	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	Mb/s
	HP	1.8V	1333	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V	800	800	800	Mb/s
	HR	N/A	800	800	800	Mb/s
RLDRAM III	HP	2.0V	800	667	667	MHz
	HP	1.8V	550	500	450	MHz
	HR	N/A	N/A			
2:1 Memory Controllers						
DDR3	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V				
	HR	N/A				
QDR II+(3)	HP	2.0V	550	500	450	MHz
	HP	1.8V				
	HR	N/A	500	450	400	MHz
RLDRAM II	HP	2.0V	533	500	450	MHz
	HP	1.8V				
	HR	N/A				
LPDDR2	HP	2.0V	667	667	667	Mb/s
	HP	1.8V	667	667	667	Mb/s
	HR	N/A	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
DIFF_HSTL_I_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.68	1.91	2.06	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.62	1.85	1.98	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.61	1.85	1.98	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
LVCMOS18_S2	0.47	0.50	0.60	3.95	4.28	4.85	4.59	5.04	5.67	ns
LVCMOS18_S4	0.47	0.50	0.60	2.67	2.98	3.43	3.31	3.73	4.26	ns
LVCMOS18_S6	0.47	0.50	0.60	2.14	2.38	2.72	2.77	3.14	3.54	ns
LVCMOS18_S8	0.47	0.50	0.60	1.98	2.21	2.52	2.61	2.97	3.35	ns
LVCMOS18_S12	0.47	0.50	0.60	1.70	1.91	2.17	2.34	2.67	2.99	ns
LVCMOS18_S16	0.47	0.50	0.60	1.57	1.75	1.97	2.20	2.51	2.79	ns
LVCMOS18_F2	0.47	0.50	0.60	3.50	3.87	4.48	4.14	4.63	5.30	ns
LVCMOS18_F4	0.47	0.50	0.60	2.23	2.50	2.87	2.87	3.25	3.69	ns
LVCMOS18_F6	0.47	0.50	0.60	1.80	2.00	2.26	2.43	2.76	3.08	ns
LVCMOS18_F8	0.47	0.50	0.60	1.46	1.72	2.04	2.10	2.47	2.86	ns
LVCMOS18_F12	0.47	0.50	0.60	1.26	1.40	1.53	1.89	2.16	2.35	ns
LVCMOS18_F16	0.47	0.50	0.60	1.19	1.33	1.44	1.83	2.08	2.26	ns
LVCMOS15_S2	0.59	0.62	0.73	3.55	3.89	4.45	4.19	4.65	5.27	ns
LVCMOS15_S4	0.59	0.62	0.73	2.45	2.70	3.06	3.08	3.45	3.89	ns
LVCMOS15_S6	0.59	0.62	0.73	2.24	2.51	2.88	2.88	3.26	3.71	ns
LVCMOS15_S8	0.59	0.62	0.73	1.91	2.16	2.49	2.55	2.91	3.31	ns
LVCMOS15_S12	0.59	0.62	0.73	1.77	1.98	2.23	2.41	2.73	3.05	ns
LVCMOS15_S16	0.59	0.62	0.73	1.62	1.81	2.02	2.26	2.56	2.84	ns
LVCMOS15_F2	0.59	0.62	0.73	3.38	3.69	4.18	4.02	4.44	5.00	ns
LVCMOS15_F4	0.59	0.62	0.73	2.04	2.21	2.44	2.68	2.97	3.26	ns
LVCMOS15_F6	0.59	0.62	0.73	1.47	1.74	2.09	2.10	2.50	2.91	ns
LVCMOS15_F8	0.59	0.62	0.73	1.31	1.46	1.61	1.95	2.22	2.43	ns
LVCMOS15_F12	0.59	0.62	0.73	1.21	1.34	1.45	1.84	2.10	2.27	ns
LVCMOS15_F16	0.59	0.62	0.73	1.18	1.31	1.41	1.82	2.07	2.23	ns
LVCMOS12_S2	0.64	0.67	0.78	3.38	3.80	4.48	4.02	4.55	5.30	ns
LVCMOS12_S4	0.64	0.67	0.78	2.62	2.94	3.43	3.26	3.70	4.25	ns
LVCMOS12_S6	0.64	0.67	0.78	2.05	2.33	2.72	2.69	3.08	3.54	ns
LVCMOS12_S8	0.64	0.67	0.78	1.94	2.18	2.51	2.58	2.94	3.33	ns
LVCMOS12_F2	0.64	0.67	0.78	2.84	3.15	3.62	3.48	3.90	4.44	ns
LVCMOS12_F4	0.64	0.67	0.78	1.97	2.18	2.44	2.61	2.93	3.26	ns
LVCMOS12_F6	0.64	0.67	0.78	1.33	1.51	1.70	1.96	2.26	2.52	ns
LVCMOS12_F8	0.64	0.67	0.78	1.27	1.42	1.55	1.91	2.18	2.37	ns
LVDCI_18	0.47	0.50	0.60	1.99	2.15	2.35	2.62	2.91	3.17	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	**T_{IOPI}**			**T_{IOOP}**			**T_{IOTP}**			**Units**
	Speed Grade			**Speed Grade**			**Speed Grade**			
	-3	**-2/-2L/-2G**	**-1**	**-3**	**-2/-2L/-2G**	**-1**	**-3**	**-2/-2L/-2G**	**-1**	
LVDCI_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
LVDCI_DV2_18	0.47	0.50	0.60	1.99	2.15	2.34	2.62	2.90	3.17	ns
LVDCI_DV2_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
HSLVDCI_18	0.68	0.72	0.82	1.99	2.15	2.35	2.62	2.91	3.17	ns
HSLVDCI_15	0.68	0.72	0.82	1.98	2.23	2.58	2.62	2.99	3.40	ns
SSTL18_I_S	0.68	0.72	0.82	1.02	1.15	1.24	1.66	1.90	2.07	ns
SSTL18_II_S	0.68	0.72	0.82	1.17	1.29	1.37	1.81	2.05	2.19	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.88	0.98	1.08	1.51	1.74	1.90	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	1.02	1.15	1.24	1.66	1.90	2.07	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	1.17	1.29	1.37	1.81	2.05	2.19	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.88	0.98	1.08	1.51	1.74	1.90	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL18_I_F	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL18_II_F	0.68	0.72	0.82	0.97	1.09	1.16	1.61	1.84	1.99	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns

Input/Output Logic Switching Characteristics

Table 22: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	ns
$T_{IDOCKE2}$/$T_{IOCKDE2}$	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
$T_{IDOCKDE2}$/$T_{IOCKDDE2}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
$T_{IDOCKE3}$/$T_{IOCKDE3}$	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
$T_{IDOCKDE3}$/$T_{IOCKDDE3}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
Combinatorial					
T_{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	ns
T_{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	ns
Sequential Delays					
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	ns
$T_{GSRQ\_ILOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	ns
$T_{GSRQ\_ILOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
$T_{RPW\_ILOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	ns, Min

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	**-2/-2L/-2G**	**-1**	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})			ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{SHCKO}[1]	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/T_{WH\_SHFREG}$	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
$T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
$T_{DS\_SHFREG}/T_{DH\_SHFREG}$	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

DSP48E1 Switching Characteristics

Table 32: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.24/0.12	0.27/0.14	0.31/0.16	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.28/0.13	0.32/0.14	0.39/0.15	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.15/0.15	0.17/0.17	0.20/0.20	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.21/0.19	0.27/0.22	0.35/0.26	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.21/0.12	0.24/0.14	0.27/0.16	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.22/0.13	0.25/0.14	0.30/0.15	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B,} input to M register CLK using multiplier	2.04/–0.01	2.34/–0.01	2.79/–0.01	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_\ D\_ADREG}$	{A, D} input to AD register CLK	1.09/–0.02	1.25/–0.02	1.49/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$	{A, B,} input to P register CLK using multiplier	3.41/–0.24	3.90/–0.24	4.64/–0.24	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.33/–0.62	3.81/–0.62	4.53/–0.62	ns
$T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$	A or B input to P register CLK not using multiplier	1.47/–0.24	1.68/–0.24	2.00/–0.24	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.30/–0.22	1.49/–0.22	1.78/–0.22	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.12/–0.13	1.28/–0.13	1.52/–0.13	ns
Setup and Hold Times of the CE Pins					
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.30/0.05	0.36/0.06	0.44/0.09	ns
$T_{DSPDCK\_CEC\_CREG}$/$T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/0.08	0.29/0.09	0.36/0.11	ns
$T_{DSPDCK\_CED\_DREG}$/$T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/–0.02	0.36/–0.02	0.44/–0.02	ns
$T_{DSPDCK\_CEM\_MREG}$/$T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/0.15	0.29/0.17	0.33/0.20	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.31/0.01	0.36/0.01	0.45/0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$/ $T_{DSPCKD\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/0.10	0.39/0.11	0.47/0.13	ns
$T_{DSPDCK\_RSTC\_CREG}$/$T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.06/0.22	0.07/0.24	0.08/0.26	ns
$T_{DSPDCK\_RSTD\_DREG}$/$T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.37/0.06	0.42/0.06	0.50/0.07	ns
$T_{DSPDCK\_RSTM\_MREG}$/$T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.18/0.18	0.20/0.21	0.23/0.24	ns
$T_{DSPDCK\_RSTP\_PREG}$/$T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.24/0.01	0.26/0.01	0.30/0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.15	3.61	4.30	ns

Table 37: **Duty Cycle Distortion and Clock Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T_{DCD_CLK}	Global clock tree duty cycle distortion(1)	All	0.20	0.20	0.20	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: **MMCM Specification**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F_{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision(4)	0.20	0.20	0.20	ns

Table 38: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_$\mathrm{T_{LOCKMAX}}$	MMCM maximum Lock Time	100	100	100	µs
MMCM_$\mathrm{F_{OUTMAX}}$	MMCM maximum output frequency	1066.00	933.00	800.00	MHz
MMCM_$\mathrm{F_{OUTMIN}}$	MMCM minimum output frequency(5)(6)	4.69	4.69	4.69	MHz
MMCM_$\mathrm{T_{EXTFDVAR}}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_$\mathrm{RST_{MINPULSE}}$	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_$\mathrm{F_{PFDMAX}}$	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
MMCM_$\mathrm{F_{PFDMIN}}$	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	MHz
MMCM_$\mathrm{T_{FBDELAY}}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$\mathrm{T_{MMCMDCK\_PSEN}}$/ $\mathrm{T_{MMCMCKD\_PSEN}}$	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	ns
$\mathrm{T_{MMCMDCK\_PSINCDEC}}$/ $\mathrm{T_{MMCMCKD\_PSINCDEC}}$	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	ns
$\mathrm{T_{MMCMCKO\_PSDONE}}$	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$\mathrm{T_{MMCMDCK\_DADDR}}$/ $\mathrm{T_{MMCMCKD\_DADDR}}$	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$\mathrm{T_{MMCMDCK\_DI}}$/$\mathrm{T_{MMCMCKD\_DI}}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$\mathrm{T_{MMCMDCK\_DEN}}$/$\mathrm{T_{MMCMCKD\_DEN}}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
$\mathrm{T_{MMCMDCK\_DWE}}$/$\mathrm{T_{MMCMCKD\_DWE}}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$\mathrm{T_{MMCMCKO\_DRDY}}$	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
$\mathrm{F_{DCK}}$	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
   See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $\mathrm{F_{VCO}}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$\mathrm{F_{OUTMIN}}$ is 0.036 MHz.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 52: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

Table 53: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1[1]	
F_{GTXMAX}[2]	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F_{GTXMIN}[2]	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[3]	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in tge *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 59: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTXMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
JT_SJ$_{12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
JT_SJ$_{11.18}$	Sinusoidal jitter (QPLL)(3)	11.18 Gb/s	0.3	–	–	UI
JT_SJ$_{10.32}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
JT_SJ$_{9.95}$	Sinusoidal jitter (QPLL)(3)	9.95 Gb/s	0.3	–	–	UI
JT_SJ$_{9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
JT_SJ$_{8.0}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
JT_SJ$_{6.6\_QPLL}$	Sinusoidal jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
JT_SJ$_{6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
JT_SJ$_{5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
JT_SJ$_{4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
JT_SJ$_{3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
JT_SJ$_{3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
JT_SJ$_{3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
JT_SJ$_{2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
JT_SJ$_{1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ$_{500}$	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
JT_TJSE$_{3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
JT_TJSE$_{6.6}$		6.6 Gb/s	0.70	–	–	UI
JT_SJSE$_{3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.1	–	–	UI
JT_SJSE$_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: **Gigabit Ethernet Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: **XAUI Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: **PCI Express Protocol Characteristics (GTX Transceivers)(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 65: **CPRI Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 64.

Table 67 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 67: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTH Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further information.

Table 68: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade			Units
			-3E/-2GE	-2(C&I)/-2LE	-1(C&I)[1]	
F_{GTHMAX}	Maximum GTH transceiver data rate		13.1	11.3	8.5	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate		0.500	0.500	0.500	Gb/s
$F_{GTHCRANGE}$	CPLL line rate range	1	3.2–10.3125		3.2–8.0	Gb/s
		2	1.6–5.16		1.6–4.0	Gb/s
		4	0.8–2.58		0.8–2.0	Gb/s
		8	0.5–1.29		0.5–1.0	Gb/s
		16	N/A			Gb/s
$F_{GTHQRANGE1}$	QPLL line rate range 1	1	8.0–11.85	8.0–11.3	8.0–8.5	Gb/s
		2	4.0–5.925	4.0–5.65	4.0–4.25	Gb/s
		4	2.0–2.9625	2.0–2.825	2.0–2.125	Gb/s
		8	1.0–1.48125	1.0–1.4125	1.0–1.0625	Gb/s
		16	N/A			Gb/s
$F_{GTHQRANGE2}$	QPLL line rate range 2	1	11.85–13.1	N/A		Gb/s
		2	5.925–6.55	N/A		Gb/s
		4	2.96–3.275	N/A		Gb/s
		8	1.48–1.63	N/A		Gb/s
		16	0.74–0.81	N/A		Gb/s
$F_{GCPLLRANGE}$	GTH transceiver CPLL frequency range		1.6–5.16		1.6–4.0	GHz
$F_{GQPLLRANGE1}$	GTH transceiver QPLL frequency range 1		8.0–11.85	8.0–11.3	8.0–8.5	GHz
$F_{GQPLLRANGE2}$	GTH transceiver QPLL frequency range 2		11.85–13.1	N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.

Table 69: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3/-2G	-2L	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	175	175	175	156	MHz

Table 74: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTHRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTHMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.3	–	–	UI
$JT\_SJ_{12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0\_QPLL}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
10/05/2011	1.1	Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to Table 12. Updated Table 84 including adding Note 1. Added Table 13. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20. Removed the *I/O Standard Adjustment Measurement Methodology* section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT\_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK\_DI\_WF\_NC}$/$T_{RCKD\_DI\_WF\_NC}$ and $T_{RDCK\_DI\_RF}$/$T_{RCKD\_DI\_RF}$ to Table 31. Completely updated the specifications in Table 83. Updated MMCM_F_{INDUTY} and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFDVAR}$ and Note 3 to Table 38. Updated the AC Switching Characteristics section. Updated the Table 50 package list. Updated the Notice of Disclaimer.
11/07/2011	1.2	Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 49.
02/13/2012	1.3	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical numbers to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 82. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 83. Updated Note 1 in Table 37. In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Updated and added notes to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/2012	1.4	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 82 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 83 to Table 38 and Table 39.

Date	Version	Description
03/27/2013	1.13	In Table 7, added values for the XC7VX330T and XC7VX415T devices. Revised Table 15 and Table 16 to include production release of the XC7VX330T and XC7VX415T. In Table 18, updated the table title, LPDDR2 values, and removed Note 3. Removed Note 2: *For QPLL line rate, the maximum line rate with the divider N set to 66 is 10.3125 Gb/s* from Table 68.
04/17/2013	1.14	Updated the AC Switching Characteristics section with production release changes to Table 15 and Table 16 for XC7VX550T for all speed specifications. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5, and combined Note 4 with old Note 5 and then added new Note 5. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4 and Table 5. Updated values and added new values to Table 7. Also revised PCI33_3 voltage minimum in Table 10 to match values in Table 1, Table 4, and Table 5. Added Note 1 to Table 12 and Table 13. Throughout the data sheet (Table 29, Table 30, and Table 45) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time." Updated and clarified USRCLK data in Table 57 and Table 72.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at http://www.xilinx.com/warranty.htm; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: http://www.xilinx.com/warranty.htm#critapps.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.