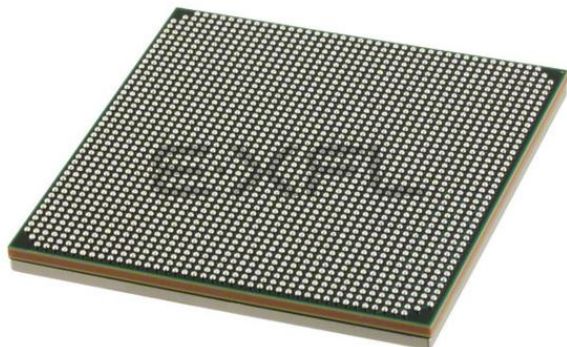




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	54150
Number of Logic Elements/Cells	693120
Total RAM Bits	54190080
Number of I/O	1000
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1930-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-3ffg1930e

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA
R_{IN_TERM} ⁽⁴⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.55$	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

- A total of 200 mA per bank should not be exceeded.

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVC MOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVC MOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVC MOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVC MOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVC MOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVC MOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVC MOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVC MOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVC MOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVC MOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVC MOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVC MOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVC MOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVC MOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVC MOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVC MOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVC MOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVC MOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVC MOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVC MOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVC MOS15_F4	0.66	0.69	0.81	1.63	1.76	1.86	2.39	2.62	2.85	ns
LVC MOS15_F8	0.66	0.69	0.81	1.79	1.99	2.18	2.55	2.85	3.17	ns
LVC MOS15_F12	0.66	0.69	0.81	1.40	1.54	1.65	2.16	2.40	2.64	ns
LVC MOS15_F16	0.66	0.69	0.81	1.37	1.51	1.61	2.13	2.37	2.60	ns
LVC MOS12_S4	0.88	0.91	1.00	2.53	2.67	2.76	3.29	3.53	3.75	ns
LVC MOS12_S8	0.88	0.91	1.00	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS12_S12 ⁽¹⁾	0.88	0.91	1.00	1.75	1.89	1.98	2.51	2.75	2.97	ns
LVC MOS12_F4	0.88	0.91	1.00	1.94	2.07	2.17	2.70	2.93	3.16	ns
LVC MOS12_F8	0.88	0.91	1.00	1.50	1.64	1.73	2.26	2.50	2.72	ns
LVC MOS12_F12 ⁽¹⁾	0.88	0.91	1.00	1.54	1.71	1.87	2.30	2.57	2.86	ns
SSTL135_S	0.61	0.64	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
SSTL15_S	0.61	0.64	0.73	1.24	1.37	1.47	2.00	2.23	2.46	ns
SSTL18_I_S	0.64	0.67	0.76	1.59	1.74	1.85	2.35	2.60	2.84	ns
SSTL18_II_S	0.64	0.67	0.76	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL135_S	0.59	0.61	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL15_S	0.63	0.67	0.77	1.24	1.37	1.47	2.00	2.23	2.46	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	1.50	1.63	1.72	2.26	2.49	2.71	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	1.13	1.22	1.25	1.89	2.08	2.24	ns
SSTL135_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL15_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL18_I_F	0.64	0.67	0.76	1.12	1.22	1.26	1.88	2.08	2.25	ns
SSTL18_II_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
DIFF_SSTL135_F	0.59	0.61	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL15_F	0.63	0.67	0.77	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	1.10	1.19	1.23	1.86	2.05	2.22	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	1.02	1.10	1.14	1.78	1.96	2.13	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_OLOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
T _{RPW_OLOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCK_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCK_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{SHCKO} ⁽¹⁾	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
T _{CECK_LRAM} /T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{WS_SHFREG} /T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
T _{CECK_SHFREG} /T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
T _{DS_SHFREG} /T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Block RAM and FIFO Clock-to-Out Delays					
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{RCKC_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	ns, Min
T _{RDCK_DI_ECCW} /T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	ns, Min
T _{RCKC_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	ns, Min
T _{RCKC_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	ns, Min
T _{RCKC_WEA} /T _{RCKC_WEA}	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	ns, Min
T _{RCKC_WREN} /T _{RCKC_WREN}	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	ns, Min
Reset Delays					
T _{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.76	0.83	0.93	ns, Max
T _{RREC_RST} /T _{RREM_RST}	FIFO reset recovery and removal timing ⁽¹¹⁾	1.59/–0.68	1.76/–0.68	2.01/–0.68	ns, Max

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{\text{DSPDO_}\{A; B\}_ \{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output	1.42	1.64	1.96	ns
$T_{\text{DSPCKO_CARRYCASCOUT_MREG}}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	ns
$T_{\text{DSPCKO_CARRYCASCOUT_ADREG_MULT}}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{\text{DSPCKO_P_AREG_MULT}}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	ns
$T_{\text{DSPCKO_P_BREG}}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	ns
$T_{\text{DSPCKO_P_CREG}}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	ns
$T_{\text{DSPCKO_P_DREG_MULT}}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	ns

Table 37: Duty Cycle Distortion and Clock Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T _{DCD_CLK}	Global clock tree duty cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T _{DCD_BUFIN}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns

PLL Switching Characteristics

Table 39: PLL Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
PLL_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3			
PLL_T _{OUTDUTY}	PLL output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100	100	100	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	1066.00	933.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max			
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_DADDR} /T _{PLLCKD_DADDR}	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DEN} /T _{PLLCKD_DEN}	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
T _{PLLDCK_DWE} /T _{PLLCKD_DWE}	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

- The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
- The static offset is measured between any PLL outputs with identical phase.
- Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
- Includes global clock buffer.
- Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks (only)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) Global clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7V585T	3.12/−0.37	3.19/−0.37	3.42/−0.37	ns
		XC7V2000T	N/A	N/A	N/A	ns
		XC7VX330T	2.90/−0.31	2.96/−0.31	3.16/−0.31	ns
		XC7VX415T	N/A	N/A	N/A	ns
		XC7VX485T	N/A	N/A	N/A	ns
		XC7VX550T	N/A	N/A	N/A	ns
		XC7VX690T	N/A	N/A	N/A	ns
		XC7VX980T	N/A	N/A	N/A	ns
		XC7VX1140T	N/A	N/A	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽³⁾ with MMCM	XC7V585T	2.71/−0.10	3.00/−0.10	3.33/−0.10	ns
		XC7V2000T	N/A	2.60/−0.24	2.87/−0.24	ns
		XC7VX330T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX415T	2.73/0.01	3.03/0.01	3.36/0.01	ns
		XC7VX485T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX550T	2.72/−0.09	3.01/−0.09	3.34/−0.09	ns
		XC7VX690T	2.72/0.01	3.01/0.01	3.34/0.01	ns
		XC7VX980T	N/A	3.01/−0.10	3.36/−0.10	ns
		XC7VX1140T	N/A	2.61/−0.24	2.88/−0.24	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

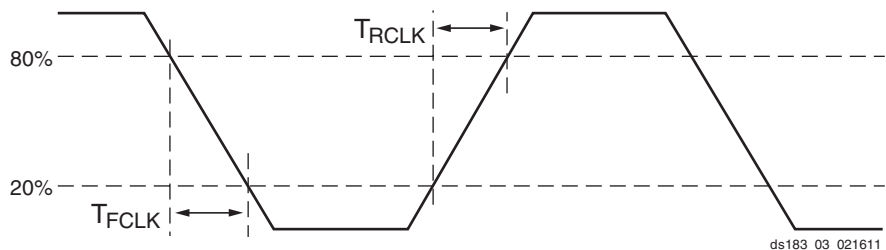


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 70: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

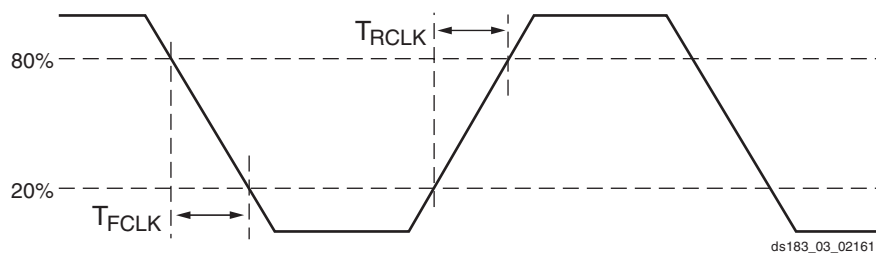


Figure 6: Reference Clock Timing Parameters

Table 71: GTH Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 78: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 79: SFP+ Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	—	0.35	UI
	1228.8	—	0.35	UI
	2457.6	—	0.35	UI
	3072.0	—	0.35	UI
	4915.2	—	0.3	UI
	6144.0	—	0.3	UI
	9830.4	—	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	—	UI
	1228.8	0.65	—	UI
	2457.6	0.65	—	UI
	3072.0	0.65	—	UI
	4915.2	0.95	—	UI
	6144.0	0.95	—	UI
	9830.4	Note 1	—	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

Table 83: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMWCCK} /T _{SMCKKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T _{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F _{RBCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F _{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T _{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
T _{SPICFC}	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* ([UG470](#)).

Table 84: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
10/05/2011	1.1	Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to Table 12. Updated Table 84 including adding Note 1. Added Table 13. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20. Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK_DI_WF_NC}/T_{RDCK_DI_WF_NC}$ and $T_{RDCK_DI_RF}/T_{RDCK_DI_RF}$ to Table 31. Completely updated the specifications in Table 83. Updated $MMCM_F_{INDUTY}$ and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFVAR}$ and Note 3 to Table 38. Updated the AC Switching Characteristics section. Updated the Table 50 package list. Updated the Notice of Disclaimer.
11/07/2011	1.2	Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 49.
02/13/2012	1.3	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical numbers to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 82. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 83. Updated Note 1 in Table 37. In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Updated and added notes to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/2012	1.4	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 82 and added Note 2. Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 83 to Table 38 and Table 39.