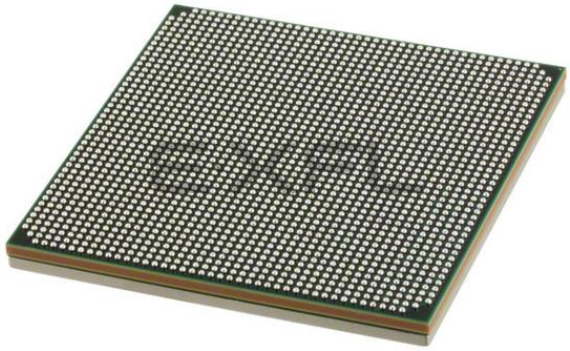
AMD Xilinx - XC7VX690T-L2FFG1930E Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	54150
Number of Logic Elements/Cells	693120
Total RAM Bits	54190080
Number of I/O	1000
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1930-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx690t-l2ffg1930e

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Table 7 shows the minimum current, in addition to I_{CCQ}, that is required by Virtex-7 T and XT devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: **Power-On Current for Virtex-7 T and XT Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCAUX_IO}	I_{CCBRAM}	Units
	Typ(1)	Typ(1)	Typ(1)	Typ(1)	Typ(1)	
XC7V585T	I_{CCINTQ} + 2700	I_{CCAUXQ} + 40	I_{CCOQ} + 60 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 108	mA
XC7V2000T	I_{CCINTQ} + 4000	I_{CCAUXQ} + 80	I_{CCOQ} + 60 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 176	mA
XC7VX330T	I_{CCINTQ} + 1000	I_{CCAUXQ} + 65	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 95	mA
XC7VX415T	I_{CCINTQ} + 1200	I_{CCAUXQ} + 75	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 115	mA
XC7VX485T	I_{CCINTQ} + 1200	I_{CCAUXQ} + 80	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 140	mA
XC7VX550T	I_{CCINTQ} + 3300	I_{CCAUXQ} + 143	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 57 mA per bank	$I_{CCBRAMQ}$ + 200	mA
XC7VX690T	I_{CCINTQ} + 3300	I_{CCAUXQ} + 143	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 57 mA per bank	$I_{CCBRAMQ}$ + 200	mA
XC7VX980T	I_{CCINTQ} + 6500	I_{CCAUXQ} + 202	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 60 mA per bank	$I_{CCBRAMQ}$ + 204	mA
XC7VX1140T	I_{CCINTQ} + 8000	I_{CCAUXQ} + 235	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 63 mA per bank	$I_{CCBRAMQ}$ + 256	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 8: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100°C$(1)	–	500	ms
		$T_J = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 as outlined in Table 14.

Table 14: **Virtex-7 T and XT FPGA Speed Specification Version By Device/Speed Grade**

Version In:		Typical V_{CCINT}	Device
ISE 14.5	Vivado 2013.1	(Table 2)	
1.09	1.09	1.0V	XC7V585T, XC7VX485T
N/A	1.08	1.0V	XC7V2000T
1.08	1.08	1.0V	XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T
N/A	1.08	1.0V	XC7VX1140T

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: **Virtex-7 T and XT Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V585T			-3, -2, -2L, -1
XC7V2000T	-2L, -2G		-2, -1
XC7VX330T			-3, -2, -2L, -1
XC7VX415T			-3, -2, -2L, -1
XC7VX485T			-3, -2, -2L, -1
XC7VX550T			-3, -2, -2L, -1
XC7VX690T			-3, -2, -2L, -1
XC7VX980T	-2, -2L, -1		
XC7VX1140T	-2, -2L, -2G, -1		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: **Virtex-7 T and XT Device Production Software and Speed Specification Release**

Device	Speed Grade Designations				
	-3	-2G	-2	-2L	-1
XC7V585T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7V2000T	N/A		Vivado 2012.4 v1.07		Vivado 2012.4 v1.07
XC7VX330T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX415T		N/A			
XC7VX485T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7VX550T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX690T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX980T	N/A	N/A			
XC7VX1140T	N/A				

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 12. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25(1)	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25(1)	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25(1)	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33(1)	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3(1)	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
DIFF_HSTL_I_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.68	1.91	2.06	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.62	1.85	1.98	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.61	1.85	1.98	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
LVCMOS18_S2	0.47	0.50	0.60	3.95	4.28	4.85	4.59	5.04	5.67	ns
LVCMOS18_S4	0.47	0.50	0.60	2.67	2.98	3.43	3.31	3.73	4.26	ns
LVCMOS18_S6	0.47	0.50	0.60	2.14	2.38	2.72	2.77	3.14	3.54	ns
LVCMOS18_S8	0.47	0.50	0.60	1.98	2.21	2.52	2.61	2.97	3.35	ns
LVCMOS18_S12	0.47	0.50	0.60	1.70	1.91	2.17	2.34	2.67	2.99	ns
LVCMOS18_S16	0.47	0.50	0.60	1.57	1.75	1.97	2.20	2.51	2.79	ns
LVCMOS18_F2	0.47	0.50	0.60	3.50	3.87	4.48	4.14	4.63	5.30	ns
LVCMOS18_F4	0.47	0.50	0.60	2.23	2.50	2.87	2.87	3.25	3.69	ns
LVCMOS18_F6	0.47	0.50	0.60	1.80	2.00	2.26	2.43	2.76	3.08	ns
LVCMOS18_F8	0.47	0.50	0.60	1.46	1.72	2.04	2.10	2.47	2.86	ns
LVCMOS18_F12	0.47	0.50	0.60	1.26	1.40	1.53	1.89	2.16	2.35	ns
LVCMOS18_F16	0.47	0.50	0.60	1.19	1.33	1.44	1.83	2.08	2.26	ns
LVCMOS15_S2	0.59	0.62	0.73	3.55	3.89	4.45	4.19	4.65	5.27	ns
LVCMOS15_S4	0.59	0.62	0.73	2.45	2.70	3.06	3.08	3.45	3.89	ns
LVCMOS15_S6	0.59	0.62	0.73	2.24	2.51	2.88	2.88	3.26	3.71	ns
LVCMOS15_S8	0.59	0.62	0.73	1.91	2.16	2.49	2.55	2.91	3.31	ns
LVCMOS15_S12	0.59	0.62	0.73	1.77	1.98	2.23	2.41	2.73	3.05	ns
LVCMOS15_S16	0.59	0.62	0.73	1.62	1.81	2.02	2.26	2.56	2.84	ns
LVCMOS15_F2	0.59	0.62	0.73	3.38	3.69	4.18	4.02	4.44	5.00	ns
LVCMOS15_F4	0.59	0.62	0.73	2.04	2.21	2.44	2.68	2.97	3.26	ns
LVCMOS15_F6	0.59	0.62	0.73	1.47	1.74	2.09	2.10	2.50	2.91	ns
LVCMOS15_F8	0.59	0.62	0.73	1.31	1.46	1.61	1.95	2.22	2.43	ns
LVCMOS15_F12	0.59	0.62	0.73	1.21	1.34	1.45	1.84	2.10	2.27	ns
LVCMOS15_F16	0.59	0.62	0.73	1.18	1.31	1.41	1.82	2.07	2.23	ns
LVCMOS12_S2	0.64	0.67	0.78	3.38	3.80	4.48	4.02	4.55	5.30	ns
LVCMOS12_S4	0.64	0.67	0.78	2.62	2.94	3.43	3.26	3.70	4.25	ns
LVCMOS12_S6	0.64	0.67	0.78	2.05	2.33	2.72	2.69	3.08	3.54	ns
LVCMOS12_S8	0.64	0.67	0.78	1.94	2.18	2.51	2.58	2.94	3.33	ns
LVCMOS12_F2	0.64	0.67	0.78	2.84	3.15	3.62	3.48	3.90	4.44	ns
LVCMOS12_F4	0.64	0.67	0.78	1.97	2.18	2.44	2.61	2.93	3.26	ns
LVCMOS12_F6	0.64	0.67	0.78	1.33	1.51	1.70	1.96	2.26	2.52	ns
LVCMOS12_F8	0.64	0.67	0.78	1.27	1.42	1.55	1.91	2.18	2.37	ns
LVDCI_18	0.47	0.50	0.60	1.99	2.15	2.35	2.62	2.91	3.17	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.97	1.09	1.16	1.61	1.84	1.99	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	ns

Table 23: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/–0.13	0.50/–0.13	0.58/–0.13	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/–0.16	0.56/–0.16	0.68/–0.16	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
$T_{GSRQ\_OLOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
$T_{GSRQ\_OLOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
$T_{RPW\_OLOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 24: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.39/–0.02	0.44/–0.02	0.63/–0.02	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.12/0.29	–0.12/0.31	–0.12/0.35	ns
Setup/Hold for Data Lines					
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.11	–0.02/0.12	–0.02/0.15	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.11	–0.02/0.12	–0.02/0.15	ns
$T_{ISDCK\_D\_DDR}$ / $T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.11	–0.02/0.12	–0.02/0.15	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.11/0.11	0.12/0.12	0.15/0.15	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 25: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input setup/hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T_{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})			ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 32: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK (DREG) to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK (CREG) to CARRYCASCOUT output	1.64	1.88	2.23	ns
Maximum Frequency					
F_{MAX}	With all registers used	741.84	650.20	547.95	MHz
F_{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	412.20	360.75	303.77	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	468.82	408.66	342.70	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	468.82	408.66	342.58	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	MHz

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7V585T	FFG1157	232	ps
			FFG1761	255	ps
		XC7V2000T	FHG1761	308	ps
			FLG1925	266	ps
		XC7VX330T	FFG1157	170	ps
			FFG1761	270	ps
		XC7VX415T	FFG1157	203	ps
			FFG1158	237	ps
			FFG1927	183	ps
		XC7VX485T	FFG1157	191	ps
			FFG1158	209	ps
			FFG1761	274	ps
			FFG1927	209	ps
			FFG1930	304	ps
		XC7VX550T	FFG1158	217	ps
			FFG1927	254	ps
		XC7VX690T	FFG1157	239	ps
			FFG1158	217	ps
			FFG1761	284	ps
			FFG1926	238	ps
			FFG1927	254	ps
			FFG1930	287	ps
		XC7VX980T	FFG1926	242	ps
			FFG1928	199	ps
			FFG1930	243	ps
		XC7VX1140T	FLG1926	271	ps
			FLG1928	216	ps
			FLG1930	279	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 57: **GTX Transceiver User Clock Switching Characteristics(1)(2)**

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G(3)	-2/-2L(3)	-1(4)	
F_{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F_{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{11.18}$	Total jitter(2)(4)	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{10.3125}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{9.8}$	Total jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{8.0}$	Total jitter(2)(4)	8.0 Gb/s	–	–	0.30	UI
$DJ_{8.0}$	Deterministic jitter(2)(4)		–	–	0.15	UI
$TJ_{6.6\_QPLL}$	Total jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI

Table 65: **CPRI Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 64.

Table 70: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

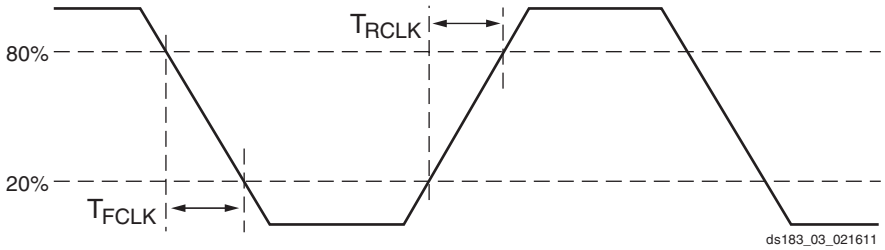

Figure 6: **Reference Clock Timing Parameters**

Table 71: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 82: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 83: **Configuration Switching Characteristics**

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency		5	5	5	ms, Max
T_{POR}(1)	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

Date	Version	Description
03/27/2013	1.13	In Table 7, added values for the XC7VX330T and XC7VX415T devices. Revised Table 15 and Table 16 to include production release of the XC7VX330T and XC7VX415T. In Table 18, updated the table title, LPDDR2 values, and removed Note 3. Removed Note 2: *For QPLL line rate, the maximum line rate with the divider N set to 66 is 10.3125 Gb/s* from Table 68.
04/17/2013	1.14	Updated the AC Switching Characteristics section with production release changes to Table 15 and Table 16 for XC7VX550T for all speed specifications. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5, and combined Note 4 with old Note 5 and then added new Note 5. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4 and Table 5. Updated values and added new values to Table 7. Also revised PCI33_3 voltage minimum in Table 10 to match values in Table 1, Table 4, and Table 5. Added Note 1 to Table 12 and Table 13. Throughout the data sheet (Table 29, Table 30, and Table 45) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.” Updated and clarified USRCLK data in Table 57 and Table 72.

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