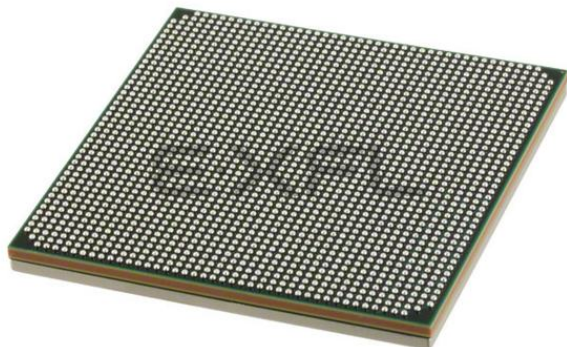




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	76500
Number of Logic Elements/Cells	979200
Total RAM Bits	55296000
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1926-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx980t-2ffg1926c

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 15](#) correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: Virtex-7 T and XT Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V585T			-3, -2, -2L, -1
XC7V2000T	-2L, -2G		-2, -1
XC7VX330T			-3, -2, -2L, -1
XC7VX415T			-3, -2, -2L, -1
XC7VX485T			-3, -2, -2L, -1
XC7VX550T			-3, -2, -2L, -1
XC7VX690T			-3, -2, -2L, -1
XC7VX980T	-2, -2L, -1		
XC7VX1140T	-2, -2L, -2G, -1		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 16](#) lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: Virtex-7 T and XT Device Production Software and Speed Specification Release

Device	Speed Grade Designations				
	-3	-2G	-2	-2L	-1
XC7V585T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7V2000T	N/A		Vivado 2012.4 v1.07		Vivado 2012.4 v1.07
XC7VX330T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX415T		N/A			
XC7VX485T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7VX550T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX690T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX980T	N/A	N/A			
XC7VX1140T	N/A				

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVDS	0.75	0.79	0.92	1.05	1.17	1.24	1.68	1.92	2.06	ns
HSUL_12	0.69	0.72	0.82	1.65	1.84	2.05	2.29	2.59	2.87	ns
DIFF_HSUL_12	0.69	0.72	0.82	1.65	1.84	2.05	2.29	2.59	2.87	ns
HSTL_I_S	0.68	0.72	0.82	1.15	1.28	1.38	1.79	2.03	2.20	ns
HSTL_II_S	0.68	0.72	0.82	1.05	1.17	1.26	1.69	1.93	2.08	ns
HSTL_I_18_S	0.70	0.72	0.82	1.12	1.24	1.34	1.75	2.00	2.16	ns
HSTL_II_18_S	0.70	0.72	0.82	1.06	1.18	1.26	1.70	1.94	2.08	ns
HSTL_I_12_S	0.68	0.72	0.82	1.14	1.27	1.37	1.78	2.02	2.20	ns
HSTL_I_DCI_S	0.68	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_II_DCI_S	0.68	0.72	0.82	1.05	1.17	1.26	1.69	1.93	2.08	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	1.15	1.28	1.38	1.78	2.03	2.20	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	1.05	1.16	1.24	1.69	1.92	2.06	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	1.15	1.28	1.38	1.79	2.03	2.20	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	1.05	1.17	1.26	1.69	1.93	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	1.15	1.28	1.38	1.78	2.03	2.20	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	1.05	1.17	1.26	1.69	1.93	2.08	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	1.12	1.24	1.34	1.75	2.00	2.16	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	1.06	1.18	1.26	1.70	1.94	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	1.11	1.23	1.33	1.74	1.99	2.15	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	1.05	1.16	1.24	1.69	1.92	2.06	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_I_F	0.68	0.72	0.82	1.02	1.14	1.22	1.66	1.90	2.04	ns
HSTL_II_F	0.68	0.72	0.82	0.97	1.08	1.15	1.61	1.84	1.97	ns
HSTL_I_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.68	1.91	2.06	ns
HSTL_II_18_F	0.70	0.72	0.82	0.98	1.09	1.16	1.62	1.85	1.98	ns
HSTL_I_12_F	0.68	0.72	0.82	1.02	1.13	1.21	1.65	1.88	2.03	ns
HSTL_I_DCI_F	0.68	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.97	1.08	1.15	1.61	1.84	1.97	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	1.02	1.14	1.22	1.66	1.90	2.04	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.98	1.09	1.16	1.61	1.85	1.98	ns
HSTL_II_T_DCI_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	1.02	1.14	1.22	1.66	1.90	2.04	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.97	1.08	1.15	1.61	1.84	1.97	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	1.02	1.14	1.22	1.66	1.90	2.04	ns
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.97	1.08	1.15	1.61	1.84	1.97	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
DIFF_HSTL_I_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.68	1.91	2.06	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.62	1.85	1.98	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.61	1.85	1.98	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
LVC MOS18_S2	0.47	0.50	0.60	3.95	4.28	4.85	4.59	5.04	5.67	ns
LVC MOS18_S4	0.47	0.50	0.60	2.67	2.98	3.43	3.31	3.73	4.26	ns
LVC MOS18_S6	0.47	0.50	0.60	2.14	2.38	2.72	2.77	3.14	3.54	ns
LVC MOS18_S8	0.47	0.50	0.60	1.98	2.21	2.52	2.61	2.97	3.35	ns
LVC MOS18_S12	0.47	0.50	0.60	1.70	1.91	2.17	2.34	2.67	2.99	ns
LVC MOS18_S16	0.47	0.50	0.60	1.57	1.75	1.97	2.20	2.51	2.79	ns
LVC MOS18_F2	0.47	0.50	0.60	3.50	3.87	4.48	4.14	4.63	5.30	ns
LVC MOS18_F4	0.47	0.50	0.60	2.23	2.50	2.87	2.87	3.25	3.69	ns
LVC MOS18_F6	0.47	0.50	0.60	1.80	2.00	2.26	2.43	2.76	3.08	ns
LVC MOS18_F8	0.47	0.50	0.60	1.46	1.72	2.04	2.10	2.47	2.86	ns
LVC MOS18_F12	0.47	0.50	0.60	1.26	1.40	1.53	1.89	2.16	2.35	ns
LVC MOS18_F16	0.47	0.50	0.60	1.19	1.33	1.44	1.83	2.08	2.26	ns
LVC MOS15_S2	0.59	0.62	0.73	3.55	3.89	4.45	4.19	4.65	5.27	ns
LVC MOS15_S4	0.59	0.62	0.73	2.45	2.70	3.06	3.08	3.45	3.89	ns
LVC MOS15_S6	0.59	0.62	0.73	2.24	2.51	2.88	2.88	3.26	3.71	ns
LVC MOS15_S8	0.59	0.62	0.73	1.91	2.16	2.49	2.55	2.91	3.31	ns
LVC MOS15_S12	0.59	0.62	0.73	1.77	1.98	2.23	2.41	2.73	3.05	ns
LVC MOS15_S16	0.59	0.62	0.73	1.62	1.81	2.02	2.26	2.56	2.84	ns
LVC MOS15_F2	0.59	0.62	0.73	3.38	3.69	4.18	4.02	4.44	5.00	ns
LVC MOS15_F4	0.59	0.62	0.73	2.04	2.21	2.44	2.68	2.97	3.26	ns
LVC MOS15_F6	0.59	0.62	0.73	1.47	1.74	2.09	2.10	2.50	2.91	ns
LVC MOS15_F8	0.59	0.62	0.73	1.31	1.46	1.61	1.95	2.22	2.43	ns
LVC MOS15_F12	0.59	0.62	0.73	1.21	1.34	1.45	1.84	2.10	2.27	ns
LVC MOS15_F16	0.59	0.62	0.73	1.18	1.31	1.41	1.82	2.07	2.23	ns
LVC MOS12_S2	0.64	0.67	0.78	3.38	3.80	4.48	4.02	4.55	5.30	ns
LVC MOS12_S4	0.64	0.67	0.78	2.62	2.94	3.43	3.26	3.70	4.25	ns
LVC MOS12_S6	0.64	0.67	0.78	2.05	2.33	2.72	2.69	3.08	3.54	ns
LVC MOS12_S8	0.64	0.67	0.78	1.94	2.18	2.51	2.58	2.94	3.33	ns
LVC MOS12_F2	0.64	0.67	0.78	2.84	3.15	3.62	3.48	3.90	4.44	ns
LVC MOS12_F4	0.64	0.67	0.78	1.97	2.18	2.44	2.61	2.93	3.26	ns
LVC MOS12_F6	0.64	0.67	0.78	1.33	1.51	1.70	1.96	2.26	2.52	ns
LVC MOS12_F8	0.64	0.67	0.78	1.27	1.42	1.55	1.91	2.18	2.37	ns
LVDCI_18	0.47	0.50	0.60	1.99	2.15	2.35	2.62	2.91	3.17	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.97	1.09	1.16	1.61	1.84	1.99	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and T_{IOIBUFDISABLE}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{IOIBUFDISABLE} is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T _{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	ns
T _{IOIBUFDISABLE_HR}	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	ns
T _{IOIBUFDISABLE_HP}	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	ns

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold for Control Lines					
$T_{ISCK_BITSIP}/T_{ISCKC_BITSIP}$	BITSIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	ns
$T_{ISCK_CE} / T_{ISCKC_CE}^{(2)}$	CE pin setup/hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	ns
$T_{ISCK_CE2} / T_{ISCKC_CE2}^{(2)}$	CE pin setup/hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/T_{ISCKD_D}	D pin setup/hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDLY}/T_{ISCKD_DDLY}$	DDLY pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin setup/hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDLY_DDR}/T_{ISCKD_DDLY_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{OSDCK_D} /T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})			ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCKO_O}^{(2)}$	BUFGCTRL delay from I/O to O	0.08	0.10	0.12	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I/O to O) values are the same as T_{BCKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	ns
Maximum Frequency					
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	ns
$T_{BHCKCK_CE}/T_{BHCKCK_CE}$	CE pin setup and hold	0.20/0.16	0.23/0.20	0.38/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	MHz

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks (only)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) Global clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7V585T	3.12/−0.37	3.19/−0.37	3.42/−0.37	ns
		XC7V2000T	N/A	N/A	N/A	ns
		XC7VX330T	2.90/−0.31	2.96/−0.31	3.16/−0.31	ns
		XC7VX415T	N/A	N/A	N/A	ns
		XC7VX485T	N/A	N/A	N/A	ns
		XC7VX550T	N/A	N/A	N/A	ns
		XC7VX690T	N/A	N/A	N/A	ns
		XC7VX980T	N/A	N/A	N/A	ns
		XC7VX1140T	N/A	N/A	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽³⁾ with MMCM	XC7V585T	2.71/−0.10	3.00/−0.10	3.33/−0.10	ns
		XC7V2000T	N/A	2.60/−0.24	2.87/−0.24	ns
		XC7VX330T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX415T	2.73/0.01	3.03/0.01	3.36/0.01	ns
		XC7VX485T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX550T	2.72/−0.09	3.01/−0.09	3.34/−0.09	ns
		XC7VX690T	2.72/0.01	3.01/0.01	3.34/0.01	ns
		XC7VX980T	N/A	3.01/−0.10	3.36/−0.10	ns
		XC7VX1140T	N/A	2.61/−0.24	2.88/−0.24	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7V585T	FFG1157	232	ps
			FFG1761	255	ps
		XC7V2000T	FHG1761	308	ps
			FLG1925	266	ps
		XC7VX330T	FFG1157	170	ps
			FFG1761	270	ps
		XC7VX415T	FFG1157	203	ps
			FFG1158	237	ps
			FFG1927	183	ps
		XC7VX485T	FFG1157	191	ps
			FFG1158	209	ps
			FFG1761	274	ps
			FFG1927	209	ps
			FFG1930	304	ps
		XC7VX550T	FFG1158	217	ps
			FFG1927	254	ps
		XC7VX690T	FFG1157	239	ps
			FFG1158	217	ps
			FFG1761	284	ps
			FFG1926	238	ps
			FFG1927	254	ps
			FFG1930	287	ps
		XC7VX980T	FFG1926	242	ps
			FFG1928	199	ps
			FFG1930	243	ps
		XC7VX1140T	FLG1926	271	ps
			FLG1928	216	ps
			FLG1930	279	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 53: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1 ⁽¹⁾	
F _{GTXMAX} ⁽²⁾	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F _{GTXMIN} ⁽²⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽³⁾	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
F _{GCPLLRANGE}	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
F _{GQPLLRange1}	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
F _{GQPLLRange2}	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	
F _{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	40	–	ps
T _{FTX}	TX fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOVBVDP}	Electrical idle amplitude		–	–	15	mV
T _{TXOVBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{10.3125}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
DJ _{10.3125}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{8.0}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.30	UI
DJ _{8.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.15	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.10	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 65: CPRI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 64.

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 66 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 66: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010	–	–	800	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /4			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /2			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

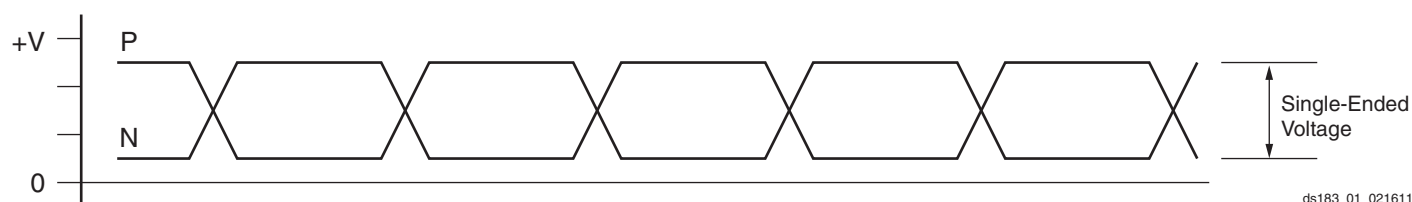


Figure 4: Single-Ended Peak-to-Peak Voltage

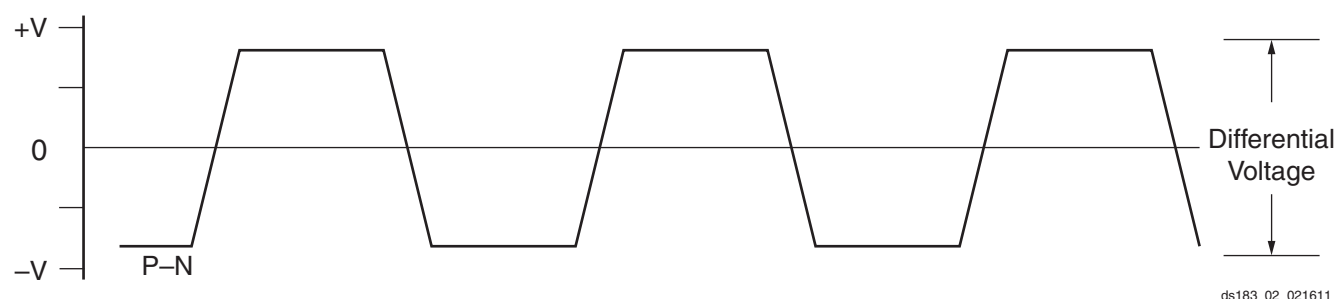


Figure 5: Differential Peak-to-Peak Voltage

Table 78: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 79: SFP+ Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	—	0.35	UI
	1228.8	—	0.35	UI
	2457.6	—	0.35	UI
	3072.0	—	0.35	UI
	4915.2	—	0.3	UI
	6144.0	—	0.3	UI
	9830.4	—	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	—	UI
	1228.8	0.65	—	UI
	2457.6	0.65	—	UI
	3072.0	0.65	—	UI
	4915.2	0.95	—	UI
	6144.0	0.95	—	UI
	9830.4	Note 1	—	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

XADC Specifications

Table 82: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 82: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference⁽⁵⁾						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for new BitGen option XADCEnhancedLinearity = ON.
- For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
- For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted. On-chip reference variation is $\pm 1\%$.

Configuration Switching Characteristics

Table 83: Configuration Switching Characteristics

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency		5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F _{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T _{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F _{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

Date	Version	Description
08/03/2012	1.5	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 12 and Note 13. Updated parameters in Table 3. Added Table 4 and Table 5. Updated the values for in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.2 speed specifications throughout the document with appropriate changes to Table 15 and Table 16 including production release of the XC7VX485T in the -2 and -1 speed designations. Added notes and specifications to Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 48 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 82 updated Note 1 and added Note 4. In Table 83, updated T_{POR} and F_{EMCK}.
09/20/2012	1.6	Removed the XC7V1500T device from data sheet. In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated some of the values in Table 7. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -2 and -1 speed designations. Added values for the XC7V585T in Table 50. Updated Note 2 in Table 58.
09/26/2012	1.7	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -3 speed designation.
10/19/2012	1.8	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -2L (1.0V) speed designation. Removed -2L (0.9V) speed specifications from data sheet, this change includes edits to V_{CCINT} and V_{CCBRAM} in Table 2, editing Note 1 and removing Note 2 in Table 53. Also in Table 53, updated the F_{GTXMAX}, $F_{GTXQRANGE1}$, and $F_{GQPLLRange1}$ specification for -1 speed grade from 6.6 Gb/s to 8.0 Gb/s. Edited Note 4 in Table 57 and Note 3 in Table 72.
12/12/2012	1.9	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.3 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -3 and -2L(1.0V) speed designations. Updated the notes in Table 50. Updated GTH Transceiver Specifications including removal of GTH Transceiver DC Characteristics section (use the XPE (download at http://www.xilinx.com/power). Updated Table 68 and added Table 71, Table 73, and Table 74. Removed Note 4 from Table 82.
12/24/2012	1.10	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.4 and Vivado 2012.4 speed specifications throughout the document. Revised the XC7V2000T in the -1 and -2 speed designations Table 15 to preliminary. Added the GTH Transceiver Protocol Jitter Characteristics section. Updated T_{TCKTDO} and added Internal Configuration Access Port section to Table 83.
01/31/2013	1.11	Added Note 2 to Table 2. Revised Table 15 and Table 16 to include production release of the XC7V2000T in the -1 and -2 speed specifications. Updated Note 1 in Table 35. Updated the notes in Table 37, Table 40 through Table 43, Table 46, and Table 47. In Table 66, updated D_{VPPIN}. In Table 67, updated V_{IDIFF}. Removed T_{LOCK} and T_{PHASE} from Table 70. Updated T_{DLOCK} in Table 71.
03/07/2013	1.12	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.5 and Vivado 2013.1 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7VX690T. Revised D_{VPPOUT} in Table 66. Updated values in Table 67 and Table 74. Removed Note 1 from Table 68. Updated $MMCM_F_{PFDMAX}$ in Table 38 and PLL_F_{PFDMAX} in Table 39. Added skew values to Table 50.