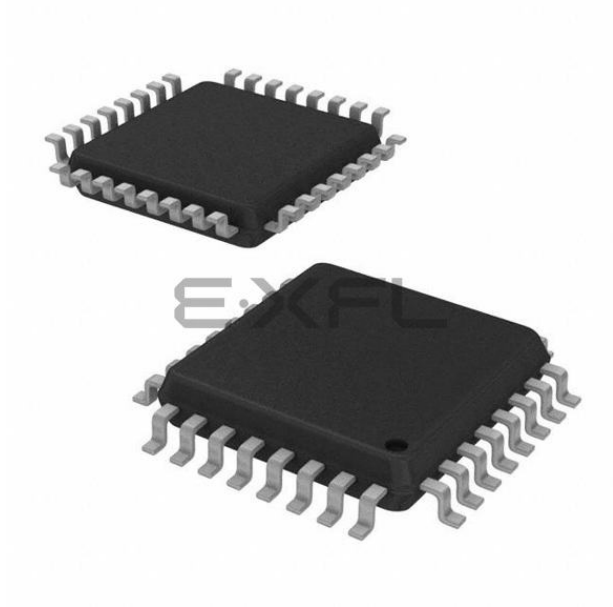

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

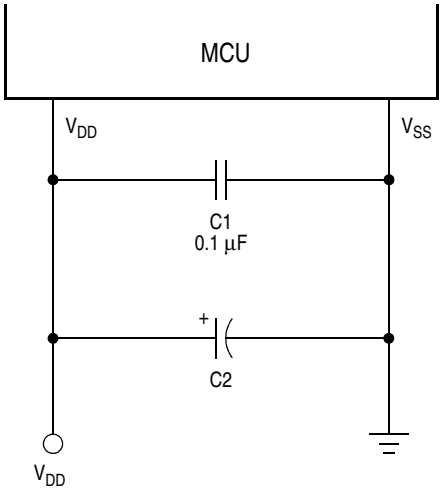
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbus, SCI, SPI
Peripherals	POR, PWM
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908ey8mfae

- Timebase Module (TBM)
- 5-bit keyboard interrupt (KBI) with wakeup feature
- 24 general-purpose input/output (I/O) pins
- External asynchronous interrupt pin with internal pullup ($\overline{IRQ}$)
- System protection features:
  - Optional computer operating properly (COP) reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- 32-pin quad flat pack (QFP) package
- Low-power design; fully static with stop and wait modes
- Internal pullups on $\overline{IRQ}$ and $\overline{RST}$ to reduce customer system cost
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin ($\overline{RST}$) and power-on reset (POR)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Higher current source capability on nine port lines for LED drive (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KBD4}$, PTA3/$\overline{KBD3}$, PTA2/$\overline{KBD2}$, PTA1/$\overline{KBD1}$, PTA0/$\overline{KBD0}$, PTC1/MOSI, and PTC0/MISO)

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16 ÷ 8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.5.2 Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator.

When selecting PTC4 and PTC3 as I/O, OSC1 and OSC2 functions are not available.

1.5.3 External Reset Pin ($\overline{RST}$)

A logic 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor that is always activated, even when the reset pin is pulled low. See Chapter 14 System Integration Module (SIM).

1.5.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled low. See Chapter 9 External Interrupt (IRQ).

1.5.5 Analog Power Supply/Reference Pins (V_{DDA}, V_{REFH}, V_{SSA} and V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Decoupling of these pins should be as per the digital supply.

NOTE

V_{REFH} is the high reference supply for the ADC. V_{DDA} should be tied to the same potential as V_{DD} via separate traces.

V_{REFL} is the low reference supply for the ADC. V_{SSA} should be tied to the same potential as V_{SS} via separate traces.

See Chapter 3 Analog-to-Digital Converter (ADC) Module.

Chapter 2
Memory

2.1 Introduction

The M68HC08 central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- 16 Kbytes of FLASH memory, 15, 872 bytes of user space
- 512 bytes of random-access memory (RAM)
- 36 bytes of user-defined vectors
- 310 bytes of monitor routines in read-only memory (ROM)
- 1024 bytes of integrated FLASH burn-in routines in ROM

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can cause an illegal address reset. In the memory map (Figure 2-1) and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on microcontroller unit (MCU) operation. In the Figure 2-1 and in register figures in this document, reserved locations are marked with the word reserved or with the letter R.

2.4 Input/Output (I/O) Section

Most of the control, status, and data registers are in the zero page area of $0000–$003F. Additional I/O registers have these addresses:

- $FE00; SIM break status register, SBSR
- $FE01; SIM reset status register, SRSR
- $FE03; SIM break flag control register, SBFCR
- $FE08; FLASH control register, FLCR
- $FE09; break address register high, BRKH
- $FE0A; break address register low, BRKL
- $FE0B; break status and control register, BRKSCR
- $FE0C; LVI status register, LVISR
- $FF7E; FLASH block protect register, FLBPR
- $FF80; ICG trim value (optional), ICGT

Data registers are shown in Figure 2-2. and Table 2-1 is a list of vector locations.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0023	Timer A Counter Modulo Register High (TAMODH) See page 203.	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Reset:	1	1	1	1	1	1	1	1
$0024	Timer A Counter Modulo Register Low (TAMODL) See page 203.	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Reset:	1	1	1	1	1	1	1	1
$0025	Timer A Channel 0 Status and Control Register (TASC0) See page 204.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	Timer A Channel 0 Register High (TACH0H) See page 207.	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Reset:	Indeterminate after reset							
$0027	Timer A Channel 0 Register Low (TACH0L) See page 207.	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Reset:	Indeterminate after reset							
$0028	Timer A Channel 1 Status and Control Register (TASC1) See page 207.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0		R					
		Reset:	0	0	0	0	0	0	0	0
$0029	Timer A Channel 1 Register High (TACH1H) See page 207.	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Reset:	Indeterminate after reset							
$002A	Timer A Channel 1 Register Low (TACH1L) See page 207.	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Reset:	Indeterminate after reset							
$002B	Timer B Status and Control Register (TBSC) See page 217.	Read:	TOF	TOIE	TSTOP	0	R	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$002C	Timer B Counter Register High (TBCNTH) See page 219.	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$002D	Timer B Counter Register Low (TBCNTL) See page 219.	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$002E	Timer B Counter Modulo Register High (TBMODH) See page 219.	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Reset:	1	1	1	1	1	1	1	1

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 7)

EXTSLOW — Slow External Crystal Enable Bit

The EXTSLOW bit has two functions. It configures the ICG module for a fast (1 MHz to 8 MHz) or slow (30 kHz to 100 kHz) speed crystal. The option also configures the clock monitor operation in the ICG module to expect an external frequency higher (307.2 kHz to 32 MHz) or lower (60 Hz to 307.2 kHz) than the base frequency of the internal oscillator. See Chapter 8 Internal Clock Generator (ICG) Module.

1 = ICG set for slow external crystal operation
0 = ICG set for fast external crystal operation

EXTCLKEN — External Clock Enable Bit

EXTCLKEN enables an external clock source or crystal/ceramic resonator to be used as a clock input. Setting this bit enables PTC4/OSC1 pin to be a clock input pin. Clearing this bit (default setting) allows the PTC4/OSC1 and PTC3/OSC2 pins to function as general-purpose input/output (I/O) pins. Refer to Table 5-1 for configuration options for the external source. See Chapter 8 Internal Clock Generator (ICG) Module for a more detailed description of the external clock operation.

1 = Allows PTC4/OSC1 to be an external clock connection
0 = PTC4/OSC1 and PTC3/OSC2 function as I/O port pins (default).

TMBCLKSEL — Timebase Clock Select Bit

TMBCLKSEL enables an enable the extra divide by 128 prescaler in the timebase module. Setting this bit enables the extra prescaler and clearing this bit disables it. Refer to Table 16-1 for timebase divider selection details.

1 = Enables extra divide by 128 prescaler in timebase module.
0 = Disables extra divide by 128 prescaler in timebase module.

OSCENINSTOP — Oscillator Enable In Stop Mode Bit

OSCENINSTOP, when set, will enable the internal clock generator module to continue to generate clocks (either internal, ICLK, or external, ECLK) in stop mode. See Chapter 8 Internal Clock Generator (ICG) Module. This function is used to keep the timebase running while the rest of the microcontroller stops. When clear, all clock generation will cease and both ICLK and ECLK will be forced low during stop mode. The default state for this option is clear, disabling the ICG in stop mode.

1 = Oscillator enabled to operate during stop mode
0 = Oscillator disabled during stop mode (default)

NOTE

This bit has the same functionality as the OSCSTOPENB CONFIG bit in MC68HC908GP20 and MC68HC908GR8 parts.

SSBPUENB — $\overline{SS}$ Pullup Enable Bit

Clearing SSBPUENB enables the $\overline{SS}$ pullup resistor.

1 = Disables $\overline{SS}$ pullup resistor.
0 = Enables $\overline{SS}$ pullup resistor.

COPRS — COP Rate Select Bit

COPRS selects the COP timeout period. Reset clears COPRS. See Chapter 6 Computer Operating Properly (COP) Module.

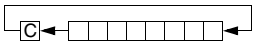
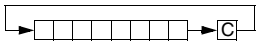
1 = COP timeout period = 8176 CGMXCLK cycles
0 = COP timeout period = 262,128 CGMXCLK cycles

LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

Table 7-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

Chapter 8
Internal Clock Generator (ICG) Module

8.1 Introduction

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The ICG generates the oscillator output clock (CGMXCLK), which is used by the computer operating properly (COP), low-voltage inhibit (LVI), and other modules. The ICG also generates the clock generator output (CGMOUT), which is fed to the system integration module (SIM) to create the bus clocks. The bus frequency will be one-fourth the frequency of CGMXCLK and one-half the frequency of CGMOUT. Finally, the ICG generates the timebase clock (TBMCLK), which is used in the timebase module (TBM).

8.2 Features

The ICG has these features:

- Selectable external clock generator, either 1-pin external source or 2-pin crystal, multiplexed with port pins
- Internal clock generator with programmable frequency output in integer multiples of a nominal frequency (307.2 kHz ± 25 percent)
- Internal oscillator trimmed accuracy of ±3.5 percent
- Bus clock software selectable from either internal or external clock (bus frequency range from 76.8 kHz ± 25 percent to 9.75 MHz ± 25 percent in 76.8-kHz increments)

NOTE

For the MC68HC908EY16, do not exceed the maximum bus frequency of 8 MHz at 5.0 V.

- Timebase clock automatically selected from external clock if external clock is available
- Clock monitor for both internal and external clocks

8.3 Functional Description

The ICG, shown in Figure 8-2, contains these major submodules:

- Clock enable circuit
- Internal clock generator
- External clock generator
- Clock monitor circuit
- Clock selection circuit

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of these actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the latch that caused the vector fetch.
- Software clear — Software can clear an interrupt latch by writing to the appropriate acknowledge bit in the interrupt status and control register (ISCR). Writing a 1 to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears both interrupt latches.

The external interrupt pin is falling-edge triggered and is software-configurable to be both falling-edge and low-level triggered. The MODE bit in the ISCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

When an interrupt pin is edge-triggered only, the interrupt latch remains set until a vector fetch, software clear, or reset occurs.

When an interrupt pin is both falling-edge and low-level-triggered, the interrupt latch remains set until both of these occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic 1

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the ISCR masks all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the corresponding IMASK bit is clear.

NOTE

The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests. See Figure 9-2.

9.4 $\overline{\text{IRQ}}$ Pin

A logic 0 on the $\overline{\text{IRQ}}$ pin can latch an interrupt request into the IRQ latch. A vector fetch, software clear, or reset clears the IRQ latch.

If the MODE bit is set, the $\overline{\text{IRQ}}$ pin is both falling-edge sensitive and low-level sensitive. With MODE set, both of these actions must occur to clear the IRQ latch:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a 1 to the ACK bit in the interrupt status and control register (ISCR). The ACK bit is useful in applications that poll the $\overline{\text{IRQ}}$ pin and require software to clear the IRQ latch. Writing to the ACK bit can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the $\overline{\text{IRQ}}$ pin. A falling edge on $\overline{\text{IRQ}}$ that occurs after writing to the ACK bit latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the vector address at locations $FFFA and $FFFB.
- Return of the $\overline{\text{IRQ}}$ pin to logic 1 — As long as the $\overline{\text{IRQ}}$ pin is at logic 0, the IRQ latch remains set.

The vector fetch or software clear and the return of the $\overline{\text{IRQ}}$ pin to logic 1 can occur in any order. The interrupt request remains pending as long as the $\overline{\text{IRQ}}$ pin is at logic 0. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

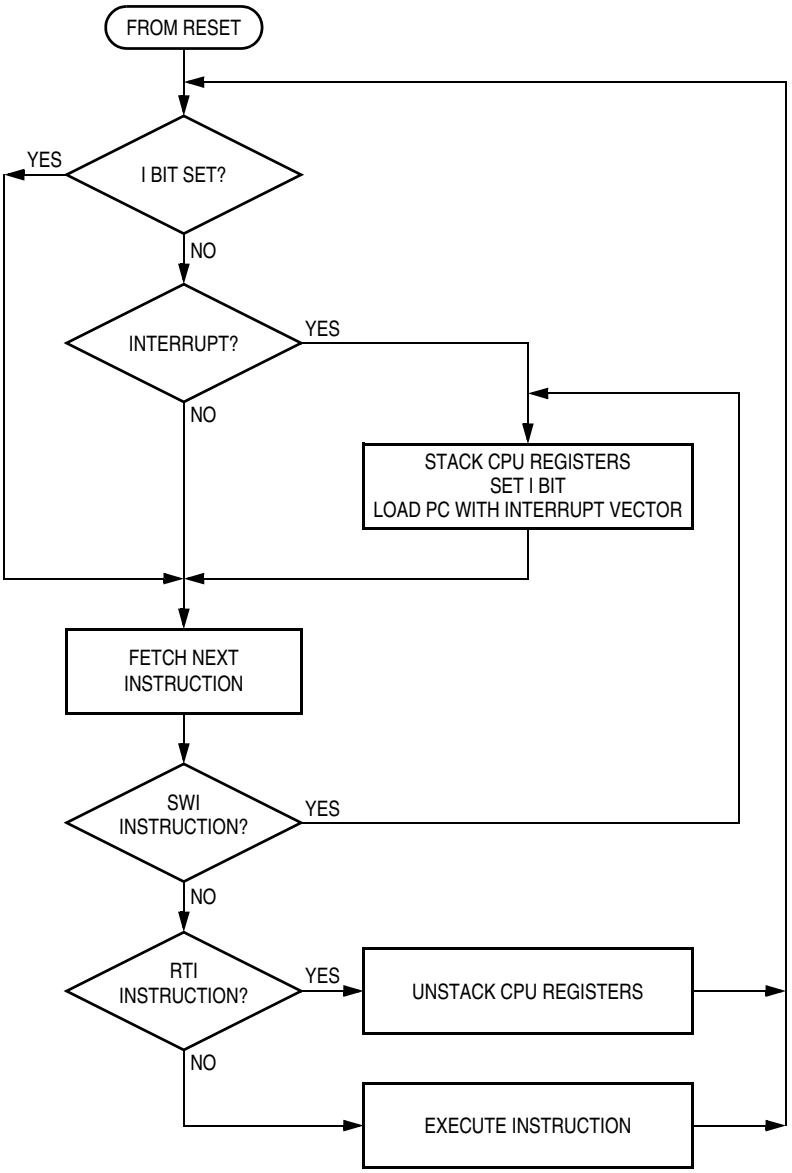


Figure 9-2. IRQ Interrupt Flowchart

If the MODE bit is clear, the $\overline{\text{IRQ}}$ pin is falling-edge sensitive only. With MODE clear, a vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in the ISCR register can be used to check for pending interrupts. The IRQF bit is not affected by the IMASK bit, which makes it useful in applications where polling is preferred.

Use the BIH or BIL instruction to read the logic level on the $\overline{\text{IRQ}}$ pin.

NOTE

When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine.

Chapter 10
Keyboard Interrupt (KBD) Module

10.1 Introduction

The keyboard interrupt (KBD) module provides five independently maskable external interrupt pins.

10.2 Features

KBD features include:

- Five keyboard interrupt pins (PTA4/$\overline{\text{KBD4}}$–PTA0/$\overline{\text{KBD0}}$) with internal pullups, with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Hysteresis buffers
- Programmable edge only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Exit from low-power modes

10.3 Functional Description

Writing to the KBIE4–KBIE0 bits in the keyboard interrupt enable register independently enables or disables each port as a keyboard interrupt pin. Enabling a keyboard interrupt pin also enables its internal pullup device. A logic 0 applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

A keyboard interrupt is latched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one pin because another pin is still low, software can disable the latter pin while it is low.
- If the keyboard interrupt is falling edge- and low level-sensitive, an interrupt request is present as long as any keyboard pin is low.

If the MODEK bit is set, the keyboard interrupt pins are both falling edge and low level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt pins and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine also can prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt pins. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the vector address at locations $FFE4 and $FFE5.
- Return of all enabled keyboard interrupt pins to logic 1. As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set.

10.7.2 Keyboard Interrupt Enable Register

The keyboard interrupt enable register enables or disables each port A pin to operate as a keyboard interrupt pin.

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-4. Keyboard Interrupt Enable Register (KBIER)

KBIE4–KBIE0 — Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin to latch interrupt requests. Reset clears the keyboard interrupt enable register.

1 = KBDx pin enabled as keyboard interrupt pin
0 = KBDx pin not enabled as keyboard interrupt pin

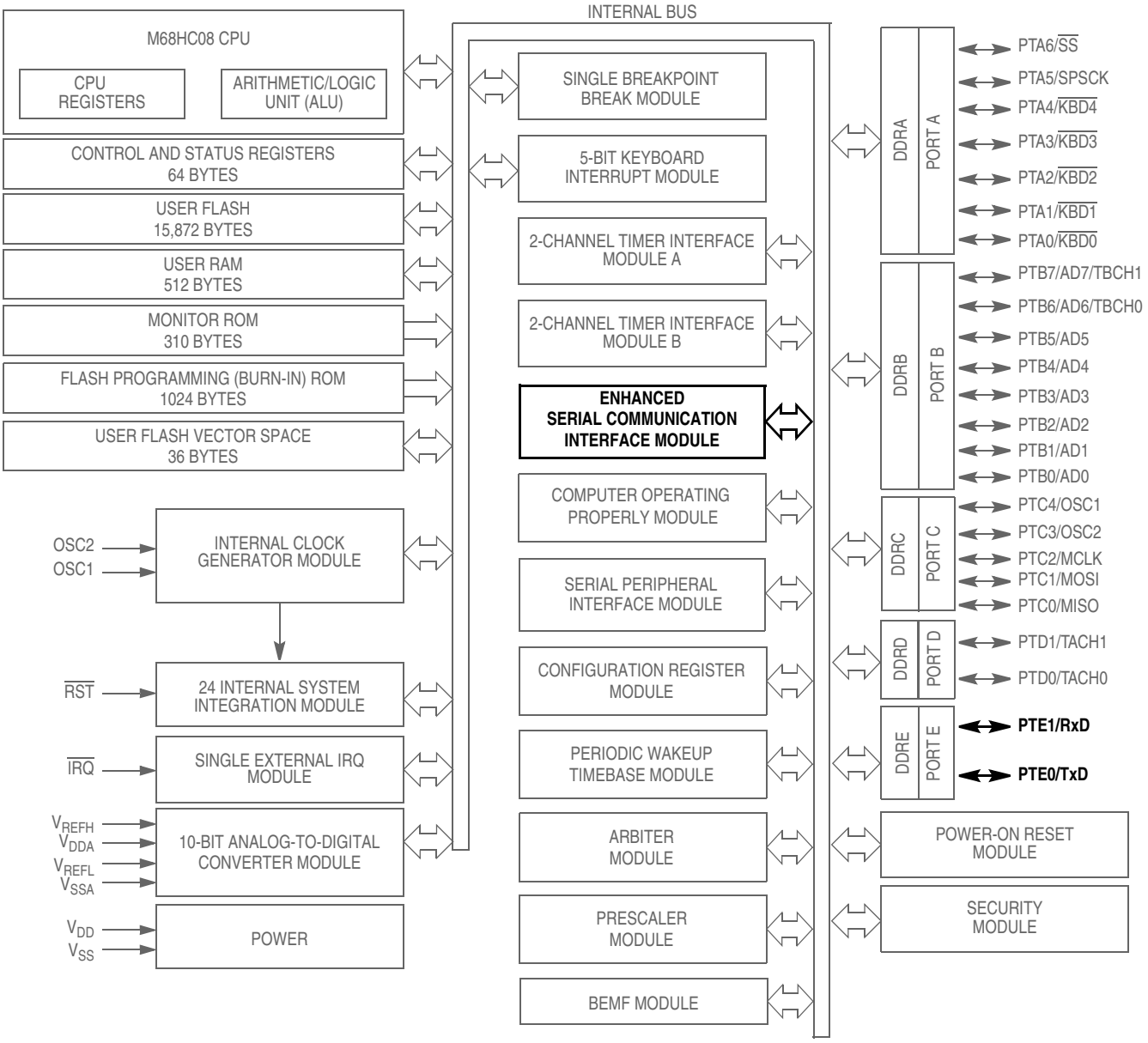


Figure 13-1. Block Diagram Highlighting ESCI Block and Pins

ESCI I/O lines are implemented by sharing parallel I/O port pins. The full name of an ESCI input or output reflects the name of the shared port pin. Table 13-1 shows the full names and the generic names of the ESCI I/O pins. The generic pin names appear in the text of this section.

Table 13-1. Pin Name Conventions

Generic Pin Names	RxD	TxD
Full Pin Names	PTE1/RxD	PTE0/TxD

Table 13-10. ESCI Prescaler Divisor Fine Adjust

PSSB[4:3:2:1:0]	Prescaler Divisor Fine Adjust (PDFA)
0 0 0 0 0	0/32 = 0
0 0 0 0 1	1/32 = 0.03125
0 0 0 1 0	2/32 = 0.0625
0 0 0 1 1	3/32 = 0.09375
0 0 1 0 0	4/32 = 0.125
0 0 1 0 1	5/32 = 0.15625
0 0 1 1 0	6/32 = 0.1875
0 0 1 1 1	7/32 = 0.21875
0 1 0 0 0	8/32 = 0.25
0 1 0 0 1	9/32 = 0.28125
0 1 0 1 0	10/32 = 0.3125
0 1 0 1 1	11/32 = 0.34375
0 1 1 0 0	12/32 = 0.375
0 1 1 0 1	13/32 = 0.40625
0 1 1 1 0	14/32 = 0.4375
0 1 1 1 1	15/32 = 0.46875
1 0 0 0 0	16/32 = 0.5
1 0 0 0 1	17/32 = 0.53125
1 0 0 1 0	18/32 = 0.5625
1 0 0 1 1	19/32 = 0.59375
1 0 1 0 0	20/32 = 0.625
1 0 1 0 1	21/32 = 0.65625
1 0 1 1 0	22/32 = 0.6875
1 0 1 1 1	23/32 = 0.71875
1 1 0 0 0	24/32 = 0.75
1 1 0 0 1	25/32 = 0.78125
1 1 0 1 0	26/32 = 0.8125
1 1 0 1 1	27/32 = 0.84375
1 1 1 0 0	28/32 = 0.875
1 1 1 0 1	29/32 = 0.90625
1 1 1 1 0	30/32 = 0.9375
1 1 1 1 1	31/32 = 0.96875

ARUN— Arbiter Counter Running Flag

This read-only bit indicates the arbiter counter is running. Reset clears ARUN.

1 = Arbiter counter running
0 = Arbiter counter stopped

AROVFL— Arbiter Counter Overflow Bit

This read-only bit indicates an arbiter counter overflow. Clear AROVFL by writing any value to SCIACTL. Writing 0s to AM1 and AM0 resets the counter keeps it in this idle state. Reset clears AROVFL.

1 = Arbiter counter overflow has occurred
0 = No arbiter counter overflow has occurred

ARD8— Arbiter Counter MSB

This read-only bit is the MSB of the 9-bit arbiter counter. Clear ARD8 by writing any value to SCIACTL. Reset clears ARD8.

13.9.2 ESCI Arbiter Data Register

Address: $0019

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-19. ESCI Arbiter Data Register (SCIADAT)

ARD7–ARD0 — Arbiter Least Significant Counter Bits

These read-only bits are the eight LSBs of the 9-bit arbiter counter. Clear ARD7–ARD0 by writing any value to SCIACTL. Writing 0s to AM1 and AM0 permanently resets the counter and keeps it in this idle state. Reset clears ARD7–ARD0.

13.9.3 Bit Time Measurement

Two bit time measurement modes, described here, are available according to the state of ACLK.

1. ACLK = 0 — The counter is clocked with one quarter of the bus clock. The counter is started when a falling edge on the RxD pin is detected. The counter will be stopped on the next falling edge. ARUN is set while the counter is running, AFIN is set on the second falling edge on RxD (for instance, the counter is stopped). This mode is used to recover the received baud rate. See Figure 13-20.
2. ACLK = 1 — The counter is clocked with one quarter of the ESCI input clock generated by the ESCI prescaler. The counter is started when a logic 0 is detected on RxD (see Figure 13-21). A logic 0 on RxD on enabling the bit time measurement with ACLK = 1 leads to immediate start of the counter (see Figure 13-22). The counter will be stopped on the next rising edge of RxD. This mode is used to measure the length of a received break.

13.9.4 Arbitration Mode

If AM[1:0] is set to 10, the arbiter module operates in arbitration mode. On every rising edge of SCI_TxD (output of the ESCI module, internal chip signal), the counter is started. When the counter reaches $38 (ACLK = 0) or $08 (ACLK = 1), RxD is statically sensed. If in this case, RxD is sensed low (for example,

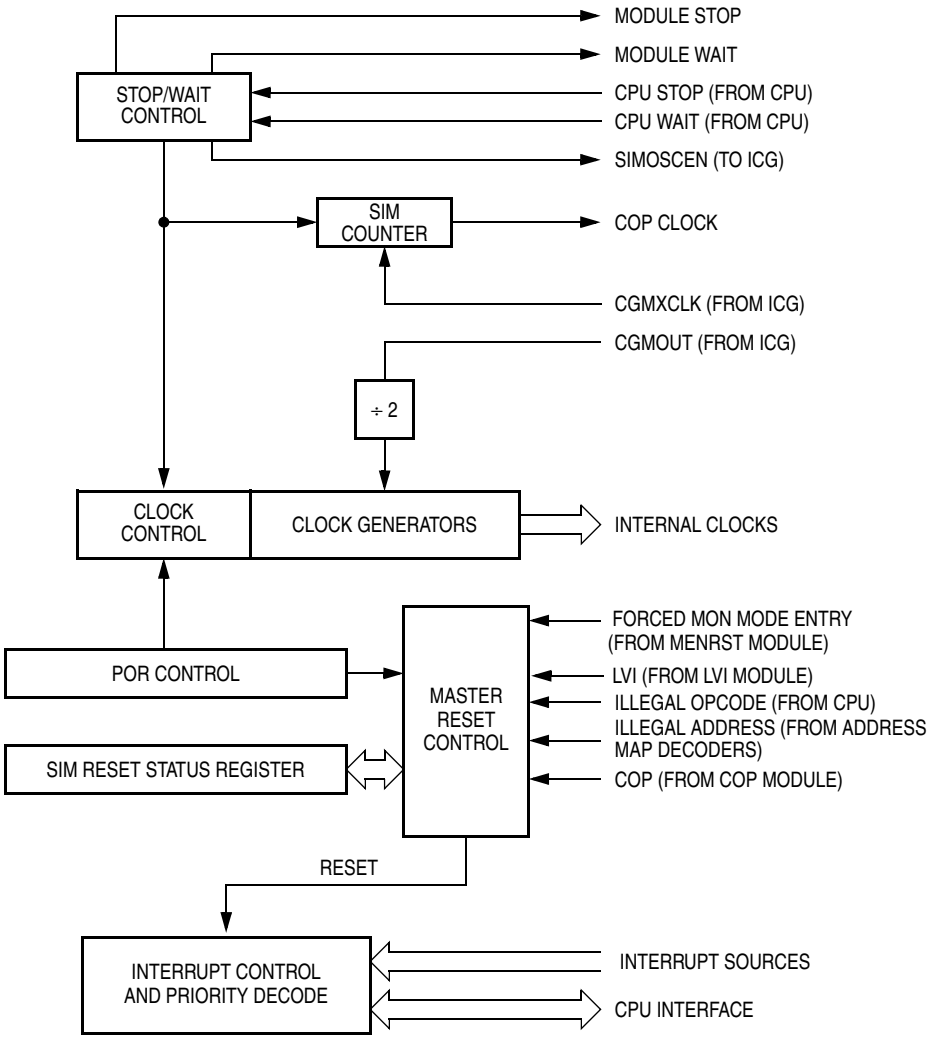


Figure 14-1. SIM Block Diagram

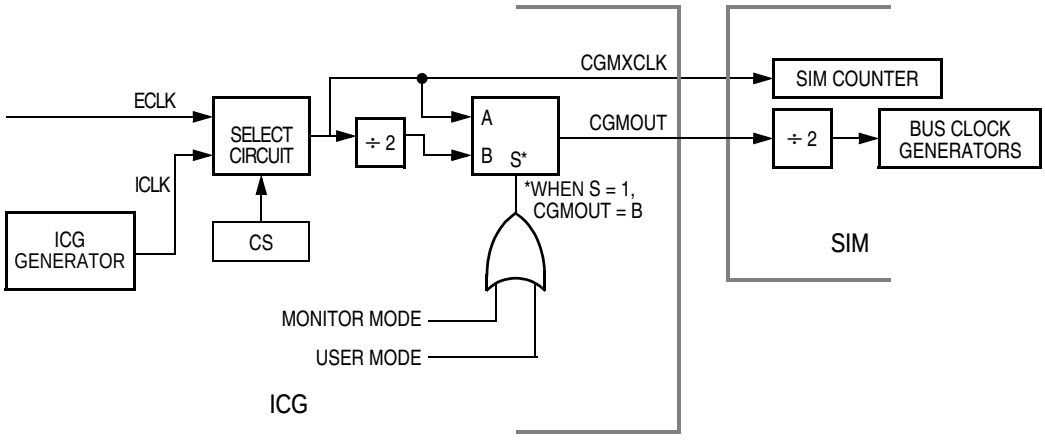


Figure 14-2. System Clock Signals

14.2.1 Bus Timing

In user mode, the internal bus frequency is the internal clock generator output (CGMXCLK) divided by four.

14.2.2 Clock Startup from POR or LVI Reset

When the power-on reset (POR) module or the low-voltage inhibit (LVI) module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after 4096 CGMXCLK cycles. The MCU is held in reset by the SIM during this entire period. The bus clocks start upon completion of the timeout.

14.2.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt or reset, the SIM allows CGMXCLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. Stop mode recovery timing is discussed in detail in 14.6.2 Stop Mode.

In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

14.3 Reset and System Initialization

The MCU has these internal reset sources:

- Power-on reset (POR) module
- Computer operating properly (COP) module
- Low-voltage inhibit (LVI) module
- Illegal opcode
- Illegal address
- Forced monitor mode entry reset (MENRST) module

All of these resets produce the vector $FFFE–$FFFF ($FEFE–$FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

These internal resets clear the SIM counter and set a corresponding bit in the SIM reset status register (SRSR). See 14.4 SIM Counter and 14.7.2 SIM Reset Status Register.

14.3.1 External Pin Reset

The $\overline{\text{RST}}$ pin circuits include an internal pullup device. Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for at least the minimum t_{IRL} time. Figure 14-3 shows the relative timing.

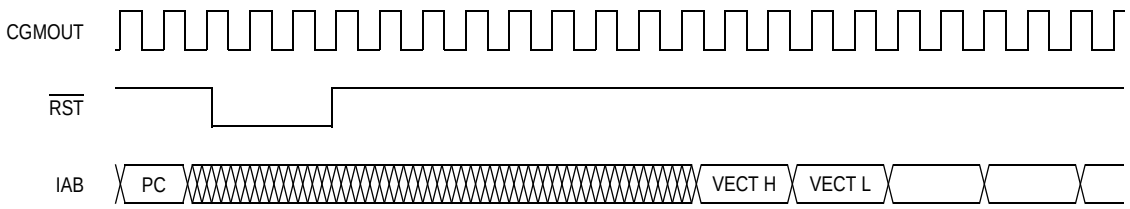


Figure 14-3. External Reset Timing

In a master SPI with the mode fault enable bit (MODFEN) set, the mode fault flag (MODF) is set if $\overline{SS}$ goes to logic 0. A mode fault in a master SPI causes the following events to occur:

- If ERRIE = 1, the SPI generates an SPI receiver/error CPU interrupt request.
- The SPE bit is cleared.
- The SPTE bit is set.
- The SPI state counter is cleared.
- The data direction register of the shared I/O port regains control of port drivers.

NOTE

To prevent bus contention with another master SPI after a mode fault error, clear all data direction register (DDR) bits associated with the SPI shared port pins.

NOTE

Setting the MODF flag (SPSCR) does not clear the SPMSTR bit. Reading SPMSTR when MODF = 1 will indicate a MODE fault error occurred in either master mode or slave mode.

When configured as a slave (SPMSTR = 0), the MODF flag is set if $\overline{SS}$ goes high during a transmission. When CPHA = 0, a transmission begins when $\overline{SS}$ goes low and ends once the incoming SPSCK returns to its idle level after the shift of the eighth data bit. When CPHA = 1, the transmission begins when the SPSCK leaves its idle level and $\overline{SS}$ is already low. The transmission continues until the SPSCK returns to its IDLE level after the shift of the last data bit. (See 15.5 Transmission Formats.)

NOTE

When CPHA = 0, a MODF occurs if a slave is selected ($\overline{SS}$ is at logic 0) and later deselected ($\overline{SS}$ is at logic 1) even if no SPSCK is sent to that slave. This happens because $\overline{SS}$ at logic 0 indicates the start of the transmission (MISO driven out with the value of MSB) for CPHA = 0. When CPHA = 1, a slave can be selected and then later deselected with no transmission occurring. Therefore, MODF does not occur since a transmission was never begun.

In a slave SPI (MSTR = 0), the MODF bit generates an SPI receiver/error CPU interrupt request if the ERRIE bit is set. The MODF bit does not clear the SPE bit or reset the SPI in any way. Software can abort the SPI transmission by toggling the SPE bit of the slave.

NOTE

A logic 1 voltage on the $\overline{SS}$ pin of a slave SPI puts the MISO pin in a high impedance state. Also, the slave SPI ignores all incoming SPSCK clocks, even if a transmission has begun.

To clear the MODF flag, read the SPSCR and then write to the SPCR register. This entire clearing procedure must occur with no MODF condition existing or else the flag will not be cleared.

17.7 I/O Signals

Port D shares two of its pins with the TIMA. There is no external clock input to the TIMA prescaler. The two TIMA channel I/O pins are PTD0/TACH0 and PTD1/TACH1. See Chapter 12 Input/Output (I/O) Ports (PORTS)

17.7.1 TIMA Channel I/O Pins (PTD0/TACH0, PTD1/TACH1)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTD0/TACH0 and PTD1/TACH1 can be configured as buffered output compare or buffered PWM pins.

17.8 I/O Registers

These I/O registers control and monitor TIMA operation:

- TIMA status and control register, TASC
- TIMA control registers, TACNTH–TACNTL
- TIMA counter modulo registers, TAMODH–TAMODL
- TIMA channel status and control registers, TASC0 and TASC1
- TIMA channel registers, TACH0H–TACH0L and TACH1H–TACH1L

17.8.1 TIMA Status and Control Register

The TIMA status and control register (TASC):

- Enables TIMA overflow interrupts
- Flags TIMA overflows
- Stops the TIMA counter
- Resets the TIMA counter
- Prescales the TIMA counter clock

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	R	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

R = Reserved

Figure 17-4. TIMA Status and Control Register (TASC)

TOF — TIMA Overflow Flag Bit

This read/write flag is set when the TIMA counter reaches the modulo value programmed in the TIMA counter modulo registers. Clear TOF by reading the TIMA status and control register when TOF is set and then writing a 0 to TOF. If another TIMA overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIMA counter has reached modulo value
0 = TIMA counter has not reached modulo value

20.10 Analog-to-Digital Converter (ADC) Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DDA}	4.5	—	5.5	V	V_{DDA} should be tied to the same potential as V_{DD} via separate traces
Input voltages	V_{ADIN}	0	—	V_{DDA}	V	V_{ADIN} <= V_{DDA}
Resolution	B_{AD}	10	—	10	Bits	
Absolute accuracy	A_{AD}	–4	—	+4	LSB	Includes quantization
ADC internal clock	f_{ADIC}	500 k	—	1.048 M	Hz	$t_{AIC} = 1/f_{ADIC}$
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V	
Power-up time	t_{ADPU}	16	—	—	t_{AIC} cycles	
Conversion time	t_{ADC}	16	—	17	t_{AIC} cycles	
Sample time	t_{ADS}	5	—	—	t_{AIC} cycles	
Monotonicity	M_{AD}	Guaranteed				
Zero input reading	Z_{ADI}	000	—	003	Hex	
Full-scale reading	F_{ADI}	3FC	—	3FF	Hex	
Input capacitance	C_{ADI}	—	—	30	pF	Not tested
V_{REFH}/V_{REFL} current	I_{VREF}	—	1.6	—	mA	
Absolute accuracy (8-bit truncated mode)	A_{AD}	–1	—	+1	LSB	Includes quantization
Zero input reading (8-bit truncated mode)	Z_{ADI}	00	—	01	Hex	
Full-scale reading (8-bit truncated mode)	F_{ADI}	FE	—	FF	Hex	
Quantization error (8-bit truncated mode)	—	—	—	+7/8 –1/8	LSB	

Chapter 21
Ordering Information and Mechanical Specifications

21.1 Introduction

This section contains ordering numbers for MC68HC908EY16. An example of the device numbering system is given in Figure 21-1. In addition, this section gives the package dimensions for the 32-pin quad flat pack (QFP).

21.2 MC Order Numbers

Table 21-1. MC Order Numbers

MC Order Number[1]	Operating Temperature Range
MC68HC908EY16KFA	–40°C to +135°C
MC68HC908EY16MFA	–40°C to +125°C
MC68HC908EY16VFA	–40°C to +105°C
MC68HC908EY16CFA	–40°C to +85°C

1. FA = Quad flat pack

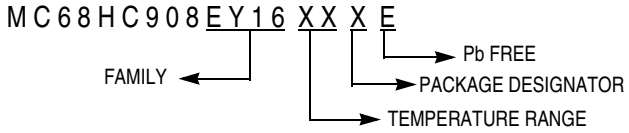


Figure 21-1. Device Numbering System