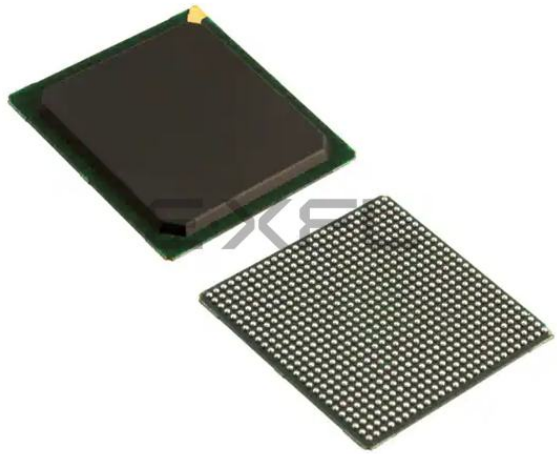

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4160
Number of Logic Elements/Cells	37440
Total RAM Bits	1548288
Number of I/O	519
Number of Gates	1800000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd1800a-4fgg676c

Package Marking

Figure 2 shows the top marking for Spartan-3A DSP FPGAs. The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

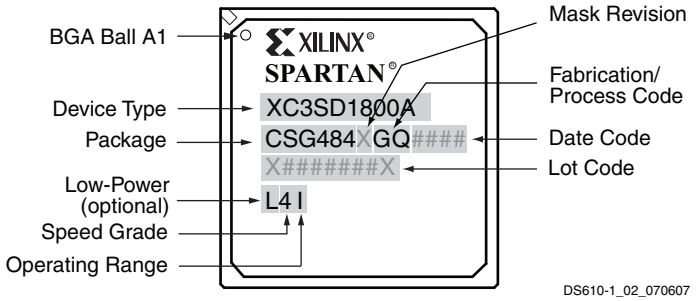
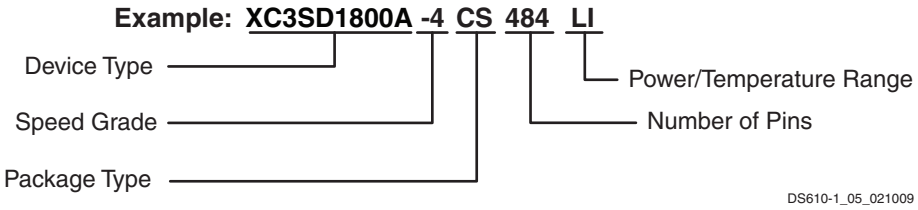


Figure 2: **Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

Spartan-3A DSP FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.



Device	Speed Grade		Package Type / Number of Pins		Power/Temperature Range (T_J)	
XC3SD1800A	-4	Standard Performance	CS484/ CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	C	Commercial (0°C to 85°C)
XC3SD3400A	-5	High Performance(1)	FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	I	Industrial (–40°C to 100°C)
					LI	Low-power Industrial (–40°C to 100°C)(2)

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. The low-power option (LI) is exclusively available in the CS(G)484 package and industrial temperature range.
3. See DS705, *XA Spartan-3A DSP Automotive FPGA Family Data Sheet* for the XA Automotive Spartan-3A DSP FPGAs.

Spartan-3A DSP FPGA Design Documentation

The functionality of the Spartan®-3A DSP FPGA family is described in the following documents. The topics covered in each guide are listed.

- DS706: E*xtended Spartan-3A Family Overview*
- UG331**:** *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- UG332**:** *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*
  - XtremeDSP DSP48A Slices
  - XtremeDSP DSP48A Pre-Adder

For specific hardware examples, please see the Spartan-3A DSP FPGA Starter Kit board web pages.

- **XtremeDSP Starter Platform—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/HW-SD1800A-DSP-SB-UNI-G.htm
- **XtremeDSP Starter Kit—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-DSP-SK-UNI-G.htm
- **XtremeDSP Video Starter Kit—Spartan-3A DSP Edition**
  http://www.xilinx.com/products/devkits/DO-S3ADSP-VIDEO-SK-UNI-G.htm
- **Embedded Development HW/SW Kit—Spartan-3A DSP S3D1800A MicroBlaze Processor Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-EDK-DK-UNI-G.htm

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Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(5)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(5)	16	–16		
	24(5)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(5)	12	–12		
	16(5)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(5)	8	–8		
	12(5)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(5)	4	–4		
	6(5)	6	–6		

Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
PCI33_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I (5)	8	–8	0.4	V_{CCO} – 0.4
HSTL_III (5)	24	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18(5)	16	–16	0.4	V_{CCO} – 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(5)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(5)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II(5)	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 10.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL}—the output current condition under which VOL is tested
   I_{OH}—the output current condition under which VOH is tested
   V_{OL}— the output voltage that indicates a Low logic level
   V_{OH}—the output voltage that indicates a High logic level
   V_{CCO}—the supply voltage for output drivers
   V_{TT}—the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.
5. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the *Using I/O Resources* chapter in UG331.

Differential I/O Standards

Differential Input Pairs

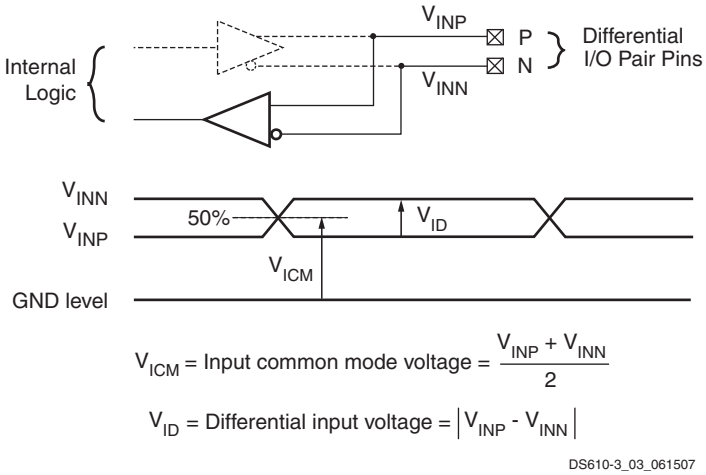

Figure 3: **Differential Input Voltages**

Table 12: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68	–	0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O."
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID}/2)$.
7. Requires V_{CCAUX} = 3.3V ±10%. (V_{CCAUX} - 300 mV) ≤ V_{ICM} ≤ (V_{CCAUX} - 37 mV).
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have VCCAUX at either 2.5V or 3.3V. Define your VCCAUX level using the CONFIG VCCAUX constraint.

Input Timing Adjustments

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0.00	0.00	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Timing Adjustments

Table 25: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 26: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs[2]		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Table 35: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Max	Max	
Clock to Out from Output Register Clock to Output Pin							
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.26	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins							
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes	Yes	3.16	3.63	ns
		–	Yes	No	1.94	2.23	ns
Clock to Out from Input Register Clock to Output Pins							
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	6.33	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	7.45	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.37	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	7.33	8.42	ns
Combinatorial Delays from Input Pins to Output Pins							
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	2.78	3.19	ns
		–	Yes	No	4.60	5.28	ns
		–	Yes	Yes	5.65	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	3.49	4.01	ns
		Yes	Yes	No	5.79	6.65	ns
		Yes	Yes	Yes	6.74	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	2.76	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	6.81	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	7.12	8.18	ns
Maximum Frequency							
F_{MAX}	All registers used	Yes	Yes	Yes	287	250	MHz

Notes:

1. To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.
2. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in Table 7.

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Byte Peripheral Interface (BPI) Configuration Timing

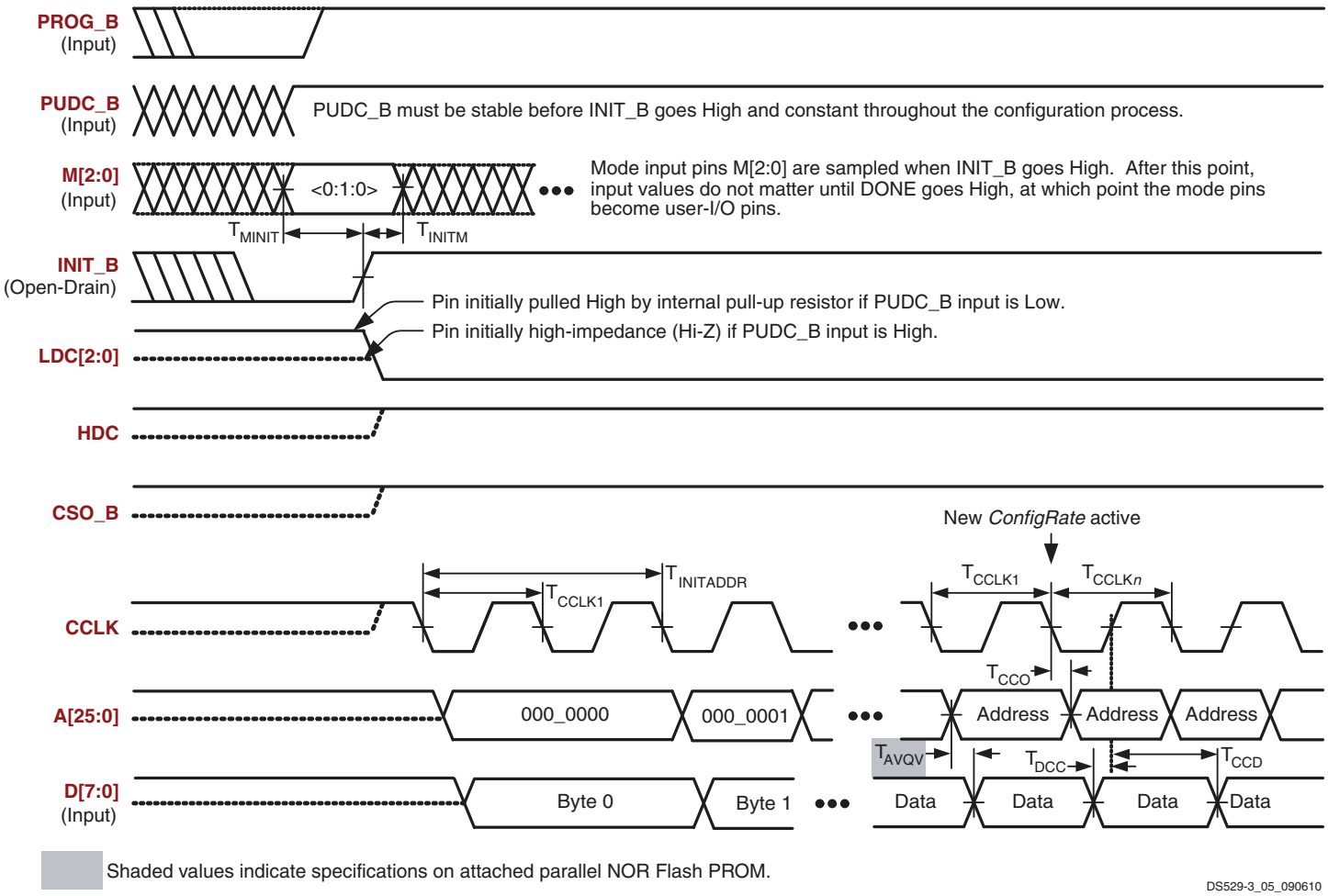

Figure 14: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

IEEE 1149.1/1532 JTAG Test Access Port Timing

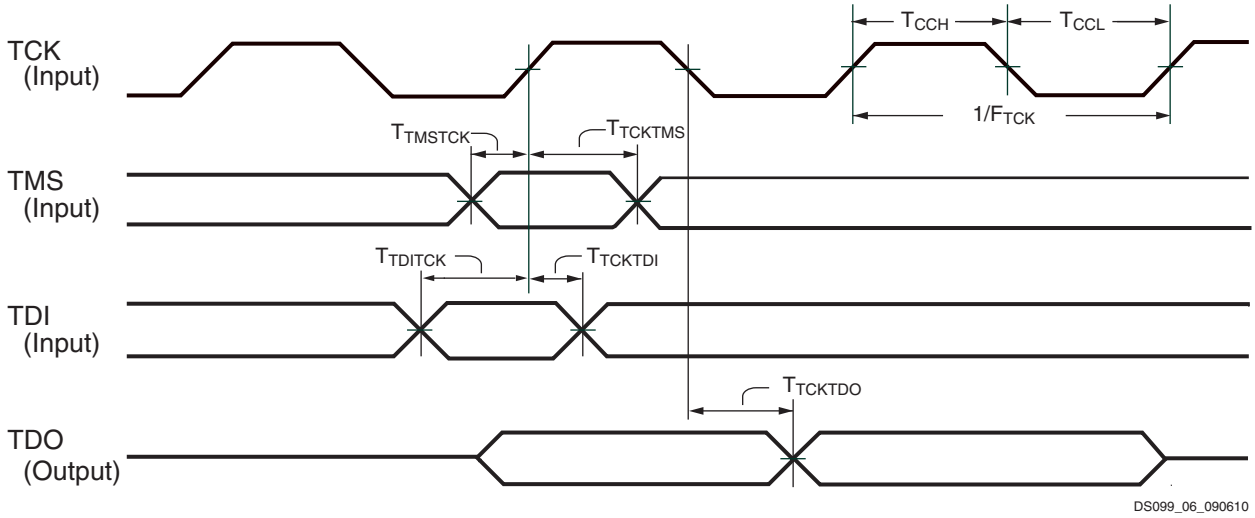

Figure 15: **JTAG Waveforms**

Table 56: **Timing for the JTAG[2] Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE)	13.0		
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	3.5		
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T_{CCL}	The Low pulse width at the TCK pin		5	–	ns
T_{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T_{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F_{TCK}	Frequency of the TCK signal	BYPASS or HIGHZ instructions	0	33	MHz
		All operations except for BYPASS or HIGHZ instructions		20	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. For details on JTAG, see Chapter 9, “JTAG Configuraton Mode and Boundary-Scan” in UG332: *Spartan-3 Generation Configuration User Guide*.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs *(Cont'd)***

Type/Color Code	Description	Pin Name(s) in Type
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected. Set on board and using CONFIG VCCAUX constraint.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 58.

Table 58: **Power and Ground Supply Pins by Package**

Package	Device	VCCINT	VCCAUX	VCCO	GND
CS484	XC3SD1800A	36	24	24	84
	XC3SD3400A	36	24	24	84
FG676	XC3SD1800A	23	14	36	77
	XC3SD3400A	36	24	40	100

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 59. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the *Using I/O Resources* chapter in UG331.

Table 59: **Maximum User I/O by Package**

Package	Device	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF[1]	CLK	N.C.
CS484	XC3SD1800A	309	60	140	156	41	52	28	32	0
	XC3SD3400A	309	60	140	156	41	52	28	32	0
FG676	XC3SD1800A	519	110	227	314	82	52	39	32	0
	XC3SD3400A	469	60	213	314	34	52	37	32	0

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and foot- prints are available for download from the Xilinx® website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Package Overview

Table 60 shows the two low-cost, space-saving production package styles for the Spartan-3A DSP family.

Table 60: **Spartan-3A DSP Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass(1) (g)
CS484 / CSG484	484	Chip-Scale Ball Grid Array (CS)	309	0.8	19 x 19	1.80	1.4
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	519	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
CS484	Package Drawing	PK230_CS484
CSG484		PK231_CSG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	T14	GND
GND	GND	T15	GND
GND	GND	T19	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U11	GND
GND	GND	U17	GND
GND	GND	W7	GND
GND	GND	W12	GND
GND	GND	W16	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	V19	PWRMGMT
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	DONE	AB21	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TMS	B1	JTAG
VCCAUX	TDO	B22	JTAG
VCCAUX	TDI	D2	JTAG
VCCAUX	VCCAUX	AA2	VCCAUX
VCCAUX	VCCAUX	AA21	VCCAUX
VCCAUX	VCCAUX	B2	VCCAUX
VCCAUX	VCCAUX	B21	VCCAUX
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	G12	VCCAUX
VCCAUX	VCCAUX	G14	VCCAUX
VCCAUX	VCCAUX	J16	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	L16	VCCAUX
VCCAUX	VCCAUX	M7	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N16	VCCAUX
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	T9	VCCAUX
VCCAUX	VCCAUX	T11	VCCAUX
VCCAUX	VCCAUX	T13	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G16	VCCINT
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	H15	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	J14	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	R8	VCCINT
VCCINT	VCCINT	R10	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	T7	VCCINT
VCCINT	VCCINT	T16	VCCINT

User I/Os by Bank

Table 64 and Table 65 indicates how the user-I/O pins are distributed between the four I/O banks on the CS484 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 64: **User I/Os Per Bank for the XC3SD1800A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Table 65: **User I/Os Per Bank for the XC3SD3400A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/O and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Footprint Migration Differences

There are no migration footprint differences between the XC3SD1800A and the XC3SD3400A in the CS484 package.

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IP_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	H25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	A23	GND
GND	GND	A26	GND
VCCAUX	SUSPEND	V20	PWRMGMT
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	TCK	A25	JTAG
VCCAUX	VCCAUX	W26	VCCAUX
VCCAUX	VCCAUX	V9	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	H23	VCCAUX
VCCAUX	VCCAUX	G26	VCCAUX
VCCAUX	VCCAUX	F9	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E20	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	D1	VCCAUX
VCCAUX	VCCAUX	AF2	VCCAUX
VCCAUX	VCCAUX	AB4	VCCAUX
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX
VCCAUX	VCCAUX	AB17	VCCAUX
VCCAUX	VCCAUX	AB22	VCCAUX
VCCAUX	VCCAUX	A24	VCCAUX
VCCINT	VCCINT	Y4	VCCINT
VCCINT	VCCINT	Y8	VCCINT
VCCINT	VCCINT	Y11	VCCINT
VCCINT	VCCINT	Y18	VCCINT
VCCINT	VCCINT	Y19	VCCINT
VCCINT	VCCINT	W18	VCCINT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
VCCINT	VCCINT	U12	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	G18	VCCINT
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	F18	VCCINT
VCCINT	VCCINT	E6	VCCINT
VCCINT	VCCINT	D5	VCCINT
VCCINT	VCCINT	C4	VCCINT
VCCINT	VCCINT	AA8	VCCINT

Right Half of FG676 Package (Top View)

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Right Half)**

Footprint Migration Differences

There are multiple migration footprint differences between the XC3SD1800A and the XC3SD3400A in the FG676 package. These migration footprint differences are shown in Table 70. Migration from the XC3S1400A Spartan-3A device in the FG676 package to a Spartan-3A DSP device in the FG676 package is also possible. The XC3S1800A pin migration differences have been added to Table 70 for designs migrating between these devices.

Table 70: **FG676 Footprint Migration Differences**

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
G16	IP_0	0	IP_0	0	GND	GND	G16
G18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	G18
F9	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	F9
F10	IP_0	0	IP_0	0	VCCINT	VCCINT	F10
F18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	F18
E6	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	E6
E9	N.C.	N.C.	IP_0	0	GND	GND	E9
E20	IP_0	0	IP_0	0	VCCAUX	VCCAUX	E20
D5	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	D5
D15	IP_0	0	IP_0	0	GND	GND	D15
D19	IP_0	0	IP_0	0	GND	GND	D19
C4	IP_0	0	IP_0	0	VCCINT	VCCINT	C4
B24	N.C.	N.C.	IP_0	0	GND	GND	B24
A5	IP_0	0	IP_0	0	GND	GND	A5
A7	IP_0	0	IP_0	0	VCCO_0	0	A7
A23	IP_0	0	IP_0	0	GND	GND	A23
A24	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	A24
Y26	IP_L16N_1	1	IP_L16N_1	1	IP_1	1	Y26
W25	IP_L16P_1	1	IP_L16P_1	1	GND	GND	W25
W26	IP_L20P_1	1	IP_L20P_1	1	VCCAUX	VCCAUX	W26
V26	IP_L20N_1/ VREF_1	1	IP_L20N_1/ VREF_1	1	IP_1/VREF_1	1	V26
U25	IP_L24P_1	1	IP_L24P_1	1	GND	GND	U25
U26	IP_L24N_1/ VREF_1	1	IP_L24N_1/ VREF_1	1	IP_1/VREF_1	1	U26
H23	IP_L48P_1	1	IP_L48P_1	1	VCCAUX	VCCAUX	H23
H24	IP_L48N_1	1	IP_L48N_1	1	IP_1	1	H24
H25	IP_L44N_1	1	IP_L44N_1	1	VCCO_1	1	H25
H26	IP_L44P_1/ VREF_1	1	IP_L44P_1/ VREF_1	1	IP_1/VREF_1	1	H26
G25	IP_L52N_1/ VREF_1	1	IP_L52N_1/ VREF_1	1	IP_1/VREF_1	1	G25
G26	IP_L52P_1	1	IP_L52P_1	1	VCCAUX	VCCAUX	G26
B25	IP_L65N_1	1	IP_L65N_1	1	GND	GND	B25
B26	IP_L65P_1/ VREF_1	1	IP_L65P_1/ VREF_1	1	IP_1/VREF_1	1	B26

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.1	Updates to Table 59, Table 63, Table 64, Table 65, Table 66, Table 67, Table 68, Table 69. Corrected VREF pins in XC3S1800A FG676 (Table 70). Updated FG676 package footprints for XC3SD1800A FPGA (Figure 16) and XC3SD3400A FPGA (Figure 17). Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options. Added advance thermal data to Table 62.
06/02/08	2.1	Added Package Overview section. Updated Thermal Characteristics in Table 62. Corrected name for AB14 in CS484 in Table 63. Updated links.
03/11/09	2.2	Corrected bank designation for SUSPEND to VCCAUX.
10/04/10	3.0	Revision update to match other data sheet modules.