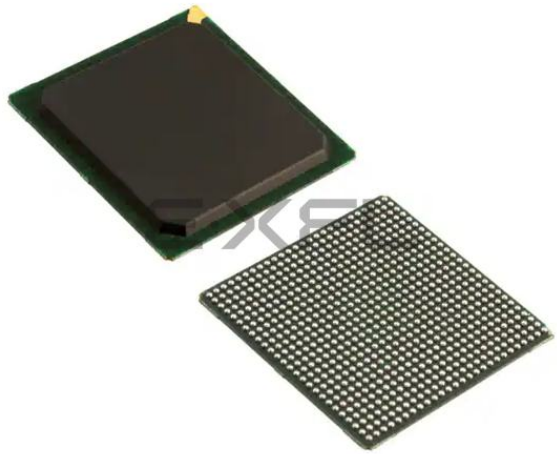

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4160
Number of Logic Elements/Cells	37440
Total RAM Bits	1548288
Number of I/O	519
Number of Gates	1800000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd1800a-4fgg676i

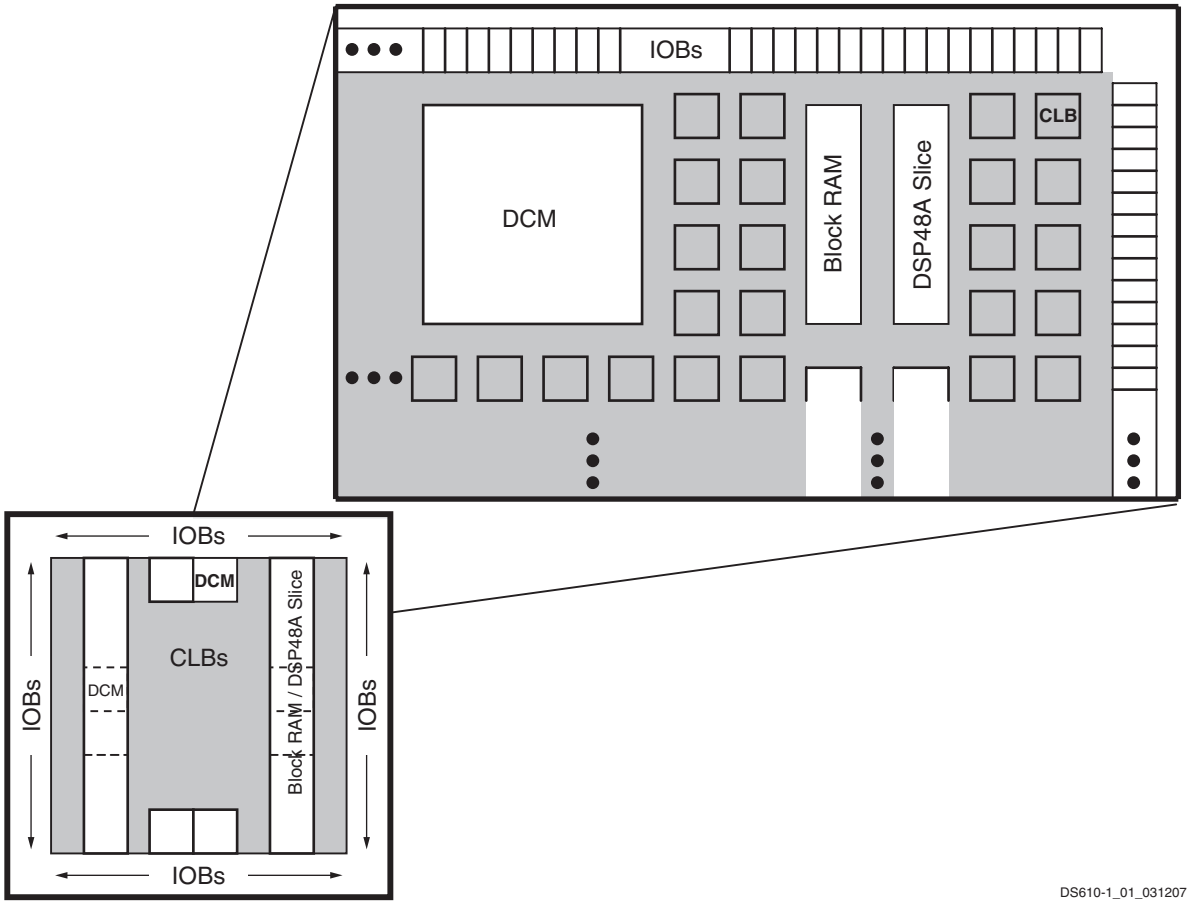
Architectural Overview

The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP™ DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XC3SD1800A has four columns of DSP48As, and the XC3SD3400A has five columns of DSP48As. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3SD1800A and XC3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer Block RAM/DSP48A columns of the 4 or 5 columns in the selected device, as shown in the diagram above.
2. A detailed diagram of the DSP48A can be found in UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide.*

Figure 1: **Spartan-3A DSP Family Architecture**

Package Marking

Figure 2 shows the top marking for Spartan-3A DSP FPGAs. The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

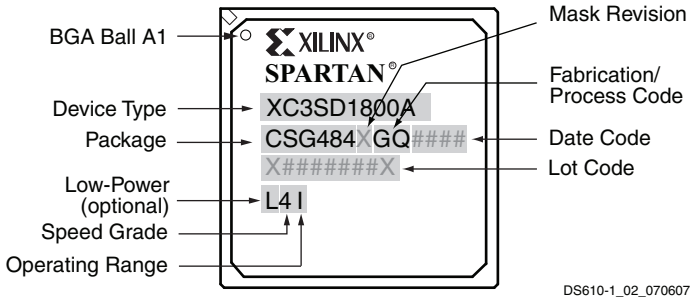
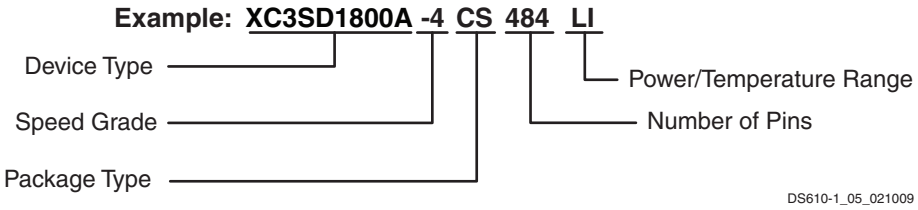


Figure 2: **Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

Spartan-3A DSP FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.



Device	Speed Grade		Package Type / Number of Pins		Power/Temperature Range (T_J)	
XC3SD1800A	-4	Standard Performance	CS484/ CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	C	Commercial (0°C to 85°C)
XC3SD3400A	-5	High Performance(1)	FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	I	Industrial (–40°C to 100°C)
					LI	Low-power Industrial (–40°C to 100°C)(2)

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. The low-power option (LI) is exclusively available in the CS(G)484 package and industrial temperature range.
3. See DS705, *XA Spartan-3A DSP Automotive FPGA Family Data Sheet* for the XA Automotive Spartan-3A DSP FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options.
06/02/08	2.1	Added reference to SCD 4103 for 750 Mbps performance. Add dual mark clarification to Package Marking. Updated links.
03/11/09	2.2	Simplified ordering information. Removed reference to SCD 4103.
10/04/10	3.0	Updated the Notice of Disclaimer section.

Notice of Disclaimer

Revision History

The following table shows the revision history for this document.

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04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options; no changes to this module.
06/02/08	2.1	Updated links.
03/11/09	2.2	Added link to DS706 on Extended Spartan-3A family.
10/04/10	3.0	Updated link to sign up for Alerts and updated Notice of Disclaimer.

Notice of Disclaimer

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 3: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 3: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

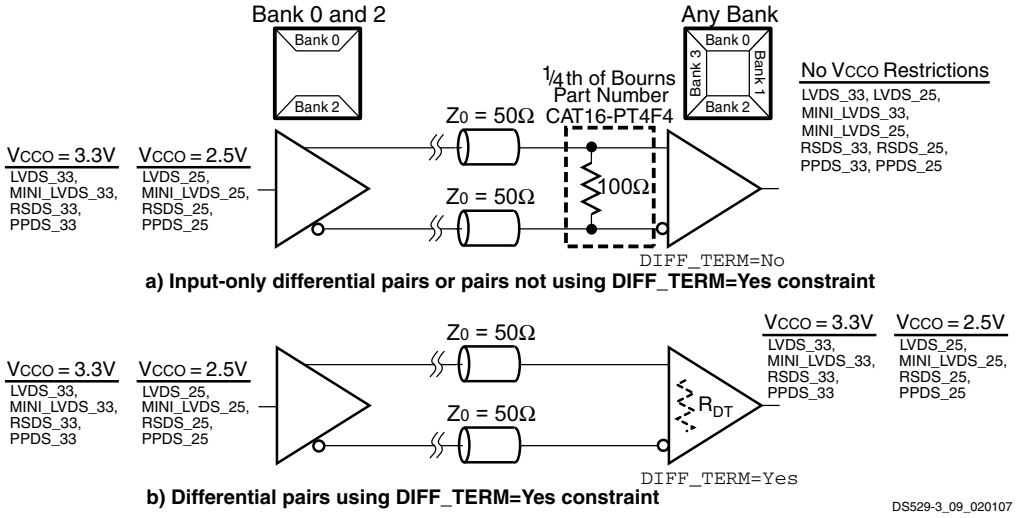

Figure 5: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

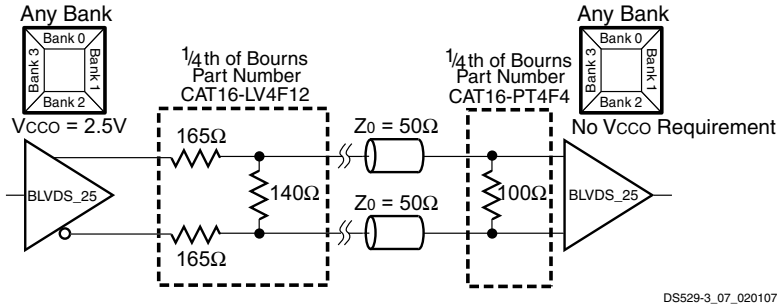

Figure 6: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

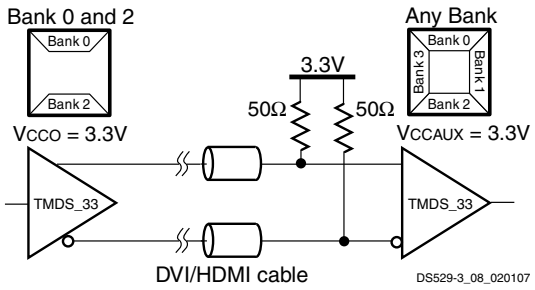

Figure 7: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 14: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A DSP FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 15. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs will require updating the Xilinx ISE development software with a future version and/or Service Pack.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 15. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 15: **Spartan-3A DSP v1.32 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3SD1800A			-4, -5
XC3SD3400A			-4, -5

Table 16 provides the recent history of the Spartan-3A DSP FPGA speed files.

Table 16: **Spartan-3A DSP Speed File Version History**

Version	ISE Release	Description
1.32	ISE 10.1.02	Updated DSP timing model to reflect higher performance for some implementations
1.31	ISE 10.1	Added Automotive support
1.30	ISE 9.2.03i	Added absolute minimum values
1.29	ISE 9.2.01i	Production Speed Files for -4 and -5 speed grades
1.28	ISE 9.2i	Minor updates
1.27	ISE 9.1.03i	Advance Speed Files for -4 speed grade

Table 19: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_ VALUE	Device	Speed		Units
					-5	-4	
					Min	Min	
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3SD1800A	–1.40	–1.40	ns
			2		–2.11	–2.11	ns
			3		–2.48	–2.48	ns
			4		–2.77	–2.77	ns
			5		–2.62	–2.62	ns
			6		–3.06	–3.06	ns
			7		–3.42	–3.42	ns
			8		–3.65	–3.65	ns
			1	XC3SD3400A	–1.31	–1.31	ns
			2		–1.88	–1.88	ns
			3		–2.44	–2.44	ns
			4		–2.89	–2.89	ns
			5		–2.83	–2.83	ns
			6		–3.33	–3.33	ns
			7		–3.63	–3.63	ns
			8		–3.96	–3.96	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 22.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 22. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 20: **Sample Window (Source Synchronous)**

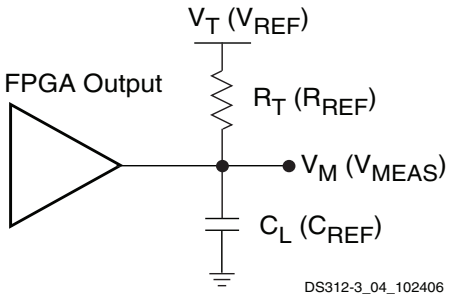
Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 8. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 8: **Output Test Setup**

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs[2]		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Table 30: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.44	–	1.72	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Table 31: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Block RAM Timing

Table 33: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
$T_{RCKO\_DOA\_NC}$	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.38	–	2.80	ns
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)	–	1.24	–	1.45	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.40	–	0.46	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.29	–	0.33	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.51	–	0.60	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	0.64	–	0.75	–	ns
T_{RCCK_REGCE}	Setup time for the CE input before the active transition at the CLK input of the block RAM	0.34	–	0.40	–	ns
T_{RCCK_RST}	Setup time for the RST input before the active transition at the CLK input of the block RAM	0.22	–	0.25	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_REGCE}	Hold time on the CE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_RST}	Hold time on the RST input after the active transition at the CLK input	0.09	–	0.10	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 35: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Max	Max	
Clock to Out from Output Register Clock to Output Pin							
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.26	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins							
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes	Yes	3.16	3.63	ns
		–	Yes	No	1.94	2.23	ns
Clock to Out from Input Register Clock to Output Pins							
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	6.33	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	7.45	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.37	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	7.33	8.42	ns
Combinatorial Delays from Input Pins to Output Pins							
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	2.78	3.19	ns
		–	Yes	No	4.60	5.28	ns
		–	Yes	Yes	5.65	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	3.49	4.01	ns
		Yes	Yes	No	5.79	6.65	ns
		Yes	Yes	Yes	6.74	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	2.76	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	6.81	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	7.12	8.18	ns
Maximum Frequency							
F_{MAX}	All registers used	Yes	Yes	Yes	287	250	MHz

Notes:

1. To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.
2. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in Table 7.

Phase Shifter (PS)

Table 40: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (FPSCLK)	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	–

Table 41: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS(2,3)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 40.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 37.

Miscellaneous DCM Timing

Table 42: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting[1]	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

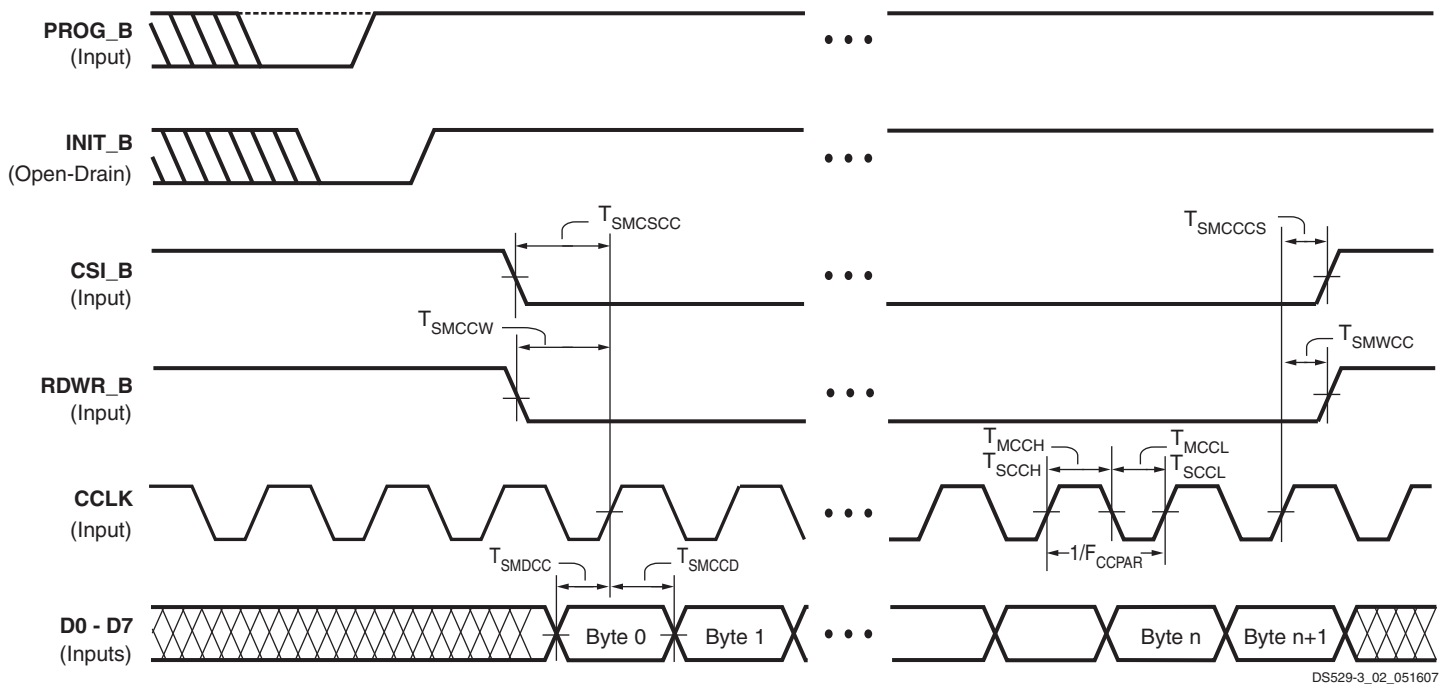
Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL} T_{SCCH}	CCLK Low and High time	5	∞	ns

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 12: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IP_0/VREF_0	D14	VREF
0	IO_L22P_0	D16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L17P_0	D18	I/O
0	IO_L11P_0	D20	I/O
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IP_0	A7	INPUT
0	IO_L38P_0	A8	I/O
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	IP_0	G16	INPUT
0	IP_0	E9	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	B24	INPUT
0	IP_0	A5	INPUT
0	IP_0	A23	INPUT
0	IP_0	F9	INPUT
0	IP_0	E20	INPUT
0	IP_0	A24	INPUT
0	IP_0	G18	INPUT
0	IP_0	F10	INPUT
0	IP_0	F18	INPUT
0	IP_0	E6	INPUT
0	IP_0	D5	INPUT
0	IP_0	C4	INPUT
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_L48N_1	H24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O
1	IP_L52N_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_L65P_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	IP_L16P_1	W25	INPUT
1	IP_L24P_1	U25	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L20P_1	W26	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52P_1	G26	INPUT
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IP_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	H25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF

Right Half of FG676 Package (Top View)

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Right Half)**