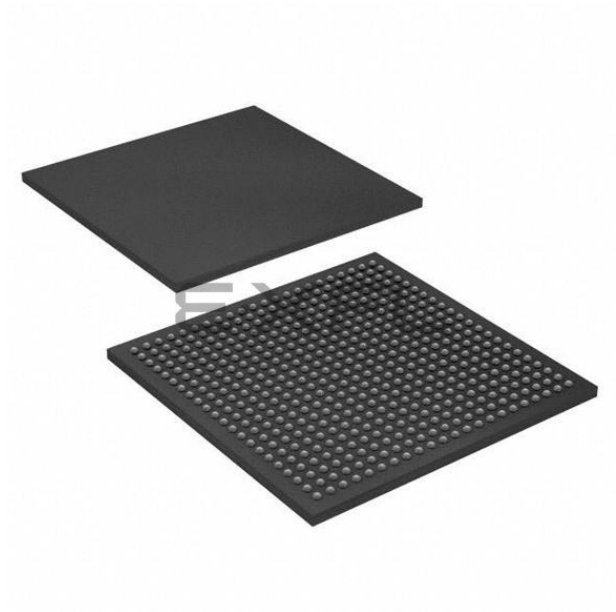

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Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4cs484c

General Recommended Operating Conditions

Table 7: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage (2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN} (3)	Input voltage	PCI™ IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# (4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time (5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 10 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 12 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(5)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(5)	16	–16		
	24(5)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(5)	12	–12		
	16(5)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(5)	8	–8		
	12(5)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(5)	4	–4		
	6(5)	6	–6		

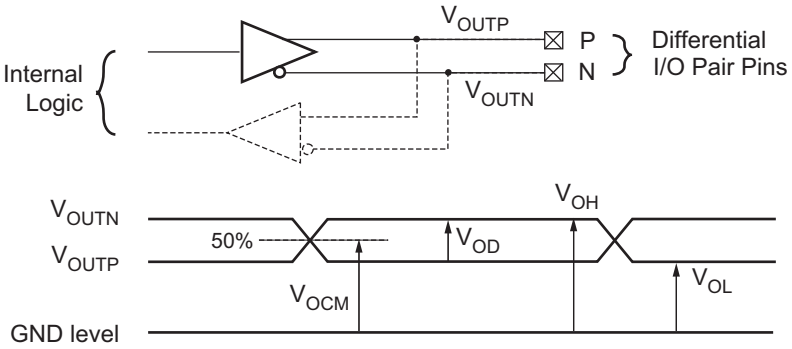
Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
PCI33_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I (5)	8	–8	0.4	V_{CCO} – 0.4
HSTL_III (5)	24	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18(5)	16	–16	0.4	V_{CCO} – 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(5)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(5)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II(5)	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 10.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL}—the output current condition under which VOL is tested
   I_{OH}—the output current condition under which VOH is tested
   V_{OL}— the output voltage that indicates a Low logic level
   V_{OH}—the output voltage that indicates a High logic level
   V_{CCO}—the supply voltage for output drivers
   V_{TT}—the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.
5. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the *Using I/O Resources* chapter in UG331.

Differential Output Pairs



V_{OCM} = Output common mode voltage = $\frac{V_{OUTP} + V_{OUTN}}{2}$

V_{OD} = Output differential voltage = $|V_{OUTP} - V_{OUTN}|$

V_{OH} = Output voltage indicating a High logic level

V_{OL} = Output voltage indicating a Low logic level

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Figure 4: **Differential Output Voltages**

Table 13: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.603	V_{TT} – 0.603
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} - 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} - 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 12.
2. See "External Termination Requirements for Differential I/O."
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 17: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, with DCM(3)	XC3SD1800A	3.28	3.51	ns
			XC3SD3400A	3.36	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, without DCM	XC3SD1800A	5.23	5.58	ns
			XC3SD3400A	5.51	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 22. If the latter is true, *add* the appropriate Output adjustment from Table 25.
3. DCM output jitter is included in all measurements.

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON} (2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON} (2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 26 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 8. Use parameter values V_T, R_T, and V_M from Table 26. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 25) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 27 and Table 28 provide the essential SSO guidelines. For each device/package combination, Table 27 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 28 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 28 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 27 and Table 28 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 27 x Table 28

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

Table 27: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*	
	CS484	FG676
XC3SD1800A	6	9
XC3SD3400A	6	10

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V)**

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Configurable Logic Block (CLB) Timing

Table 29: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0.00	–	0.00	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.00	–	0.00	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter (2)(3)(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz < FCLKIN < 15 MHz	All	–	5	–	5	ms
		FCLKIN > 15 MHz		–	600	–	600	µs

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for v1.29 production speed files. Noted banking rules in Table 11 and Table 12. Added DIFF_HSTL_I and DIFF_HSTL_III to Table 12, Table 13, and Table 26. Updated TMDS DC characteristics in Table 13. Updated I/O Test Method values in Table 26. Added Simultaneously Switching Output limits in Table 28. Updated DSP48A timing symbols, descriptions, and values in Table 34. Added power-on timing in Table 45. Added CCLK specifications for Commercial in Table 46 through Table 48. Updated Slave Parallel timing in Table 51. Updated JTAG specifications in Table 56.
07/16/07	2.0	Added Low-power options and updated typical values for quiescent current in Table 9. Updated DSP48A timing in Table 34 and Table 35.
06/02/08	2.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 4 and updated V_{CCO} POR levels in Figure 10. Added V_{IN} to Recommended Operating Conditions in Table 7 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 20%-44% in Table 9. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 10. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}–0.4V for LVCMOS15/18 in Table 11. Added reference to V_{CCAUX} in Simultaneously Switching Output Guidelines. Removed DNA_RETENTION limit of 10 years in Table 14 since number of Read cycles is the only unique limit. Updated speed files to v1.31 in Table 16 and elsewhere. Updated IOB Setup and Hold times with device-specific values in Table 19. Added reference to Sample Window in Table 20. Updated IOB Propagation times with device-specific values in Table 21. Improved SSTL_18_II SSO value in Table 28. Improved F_{BUFG} for -4 to 334 MHz in Table 32. Added references to 375 MHz performance via SCD 4103 in Table 32,Table 37, Table 38, and Table 39. Added explanatory footnotes to DSP48A Timing tables. Simplified DSP48A F_{MAX} to value with all registers used in Table 35. Improved FBUFG in Table 32 for -4 speed grade. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Replaced BPI with SPI specification descriptions in Table 52. Corrected BPI Figure 14 and Table 54 from falling edge to rising edge. Added references to Spartan-3 Generation User Guides. Updated links.
03/11/09	2.2	Changed typical quiescent current temperature from ambient to quiescent. Updated selected I/O standard DC characteristics. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added T_{IOPI} and T_{IOPID} to Table 21. Updated BPI configuration waveforms in Figure 14 and updated Table 55. Removed references to SCD 4103.
10/04/10	3.0	Added I_{IK} to Table 3. Updated description for V_{IN} in Table 7 including adding note 4. Also, added note 2 to I_L in Table 8 to note potential leakage between pins of a differential pair. Added note 6 to Table 10. Updated notes 5 and 6 in Table 12. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 44.

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IO_L03N_1/A1	V20	DUAL
1	IP_L08P_1	V22	INPUT
1	IO_L03P_1/A0	W19	DUAL
1	IP_L04N_1/VREF_1	W20	VREF
1	IP_L04P_1	W21	INPUT
1	IO_L06P_1	W22	I/O
1	IO_L02P_1/LDC1	Y21	DUAL
1	IO_L06N_1	Y22	I/O
1	VCCO_1	E21	VCCO
1	VCCO_1	J18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P18	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01P_2/M1	AA3	DUAL
2	IO_L04N_2	AA4	I/O
2	IP_2	AA6	INPUT
2	IO_L08N_2	AA8	I/O
2	IO_L12N_2/D6	AA10	DUAL
2	IO_L16P_2/GCLK14	AA12	GCLK
2	IO_L18N_2/GCLK3	AA14	GCLK
2	IO_L19P_2	AA15	I/O
2	IO_L22P_2/AWAKE	AA17	PWRMGMT
2	IO_L27N_2	AA19	I/O
2	IO_L30P_2	AA20	I/O
2	IP_2/VREF_2	AB2	VREF
2	IO_L01N_2/M0	AB3	DUAL
2	IO_L04P_2	AB4	I/O
2	IO_L05P_2	AB5	I/O
2	IO_L05N_2	AB6	I/O
2	IO_L08P_2	AB7	I/O
2	IO_L09P_2/VS1	AB8	DUAL
2	IO_L09N_2/VS0	AB9	DUAL
2	IO_L12P_2/D7	AB10	DUAL
2	IP_2/VREF_2	AB11	VREF
2	IO_L16N_2/GCLK15	AB12	GCLK
2	IO_L18P_2/GCLK2	AB13	GCLK
2	IO_L19N_2	AB14	I/O
2	IP_2	AB15	INPUT
2	IO_L22N_2/DOUT	AB16	DUAL
2	IO_L23P_2	AB17	I/O
2	IO_L23N_2	AB18	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IO_L27P_2	AB19	I/O
2	IO_L30N_2	AB20	I/O
2	IO_L02N_2/CSO_B	U7	DUAL
2	IO_L11N_2	U8	I/O
2	IO_L10N_2	U9	I/O
2	IO_L14N_2/D4	U10	DUAL
2	IO_L17P_2/GCLK0	U12	GCLK
2	IO_L20P_2	U13	I/O
2	IO_L25P_2	U14	I/O
2	IO_L25N_2	U15	I/O
2	IO_L28P_2	U16	I/O
2	IO_L02P_2/M2	V6	DUAL
2	IO_L11P_2	V7	I/O
2	IO_L06N_2	V8	I/O
2	IO_L10P_2	V10	I/O
2	IO_L14P_2/D5	V11	DUAL
2	IO_L17N_2/GCLK1	V12	GCLK
2	IO_L20N_2/MOSI/CSI_B	V13	DUAL
2	IP_2/VREF_2	V15	VREF
2	IO_L28N_2	V16	I/O
2	IO_L31N_2/CCLK	V17	DUAL
2	IP_2/VREF_2	W4	VREF
2	IO_L03P_2	W5	I/O
2	IO_L07N_2/VS2	W6	DUAL
2	IO_L06P_2	W8	I/O
2	IP_2/VREF_2	W9	VREF
2	IP_2	W10	INPUT
2	IP_2/VREF_2	W13	VREF
2	IO_L21N_2	W14	I/O
2	IO_L24P_2/INIT_B	W15	DUAL
2	IO_L31P_2/D0/DIN/MISO	W17	DUAL
2	IP_2/VREF_2	W18	VREF
2	IO_L03N_2	Y4	I/O
2	IO_L07P_2/RDWR_B	Y5	DUAL
2	IP_2	Y6	INPUT
2	IP_2	Y7	INPUT
2	IO_L13P_2	Y8	I/O
2	IO_L13N_2	Y9	I/O
2	IO_L15N_2/GCLK13	Y10	GCLK
2	IO_L15P_2/GCLK12	Y11	GCLK
2	IP_2	Y12	INPUT
2	IO_L21P_2	Y13	I/O

FG676: 676-Ball Fine-Pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports both the XC3SD1800A and the XC3SD3400A FPGAs. There are multiple pinout differences between the two devices. For a list of differences and migration advice, see the Footprint Migration Differences section.

XC3SD1800A FPGA

Table 66 lists all the FG676 package pins for the XC3SD1800A FPGA. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Pinout Table

Note: The grayed boxes denote a difference between the XC3SD1800A and the XC3SD3400A devices.

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA**

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L43N_0	K11	I/O
0	IO_L39N_0	K12	I/O
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L12N_0	K16	I/O
0	IP_0	J10	INPUT
0	IO_L43P_0	J11	I/O
0	IO_L39P_0	J12	I/O
0	IP_0	J13	INPUT
0	IO_L25N_0/GCLK5	J14	GCLK
0	IP_0	J15	INPUT
0	IO_L12P_0	J16	I/O
0	IP_0/VREF_0	J17	VREF
0	IO_L47N_0	H9	I/O
0	IO_L46N_0	H10	I/O
0	IO_L35N_0	H12	I/O
0	IP_0	H13	INPUT
0	IO_L16N_0	H15	I/O
0	IO_L08P_0	H17	I/O
0	IP_0	H18	INPUT
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L47P_0	G9	I/O
0	IO_L46P_0	G10	I/O
0	IP_0/VREF_0	G11	VREF
0	IO_L35P_0	G12	I/O
0	IO_L27N_0/GCLK9	G13	GCLK
0	IP_0	G14	INPUT
0	IO_L16P_0	G15	I/O
0	IO_L08N_0	G17	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L01P_0	G20	I/O
0	IO_L48P_0	F7	I/O
0	IO_L52P_0/VREF_0	F8	VREF
0	IO_L31N_0	F12	I/O
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L24N_0	F14	I/O
0	IO_L20P_0	F15	I/O
0	IO_L13P_0	F17	I/O
0	IO_L02N_0	F19	I/O
0	IO_L01N_0	F20	I/O
0	IO_L48N_0	E7	I/O
0	IO_L37P_0	E10	I/O
0	IP_0	E11	INPUT
0	IO_L31P_0	E12	I/O
0	IO_L24P_0	E14	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L13N_0	E17	I/O
0	IP_0	E18	INPUT
0	IO_L10P_0	E21	I/O
0	IO_L44N_0	D6	I/O
0	IP_0/VREF_0	D7	VREF
0	IO_L40N_0	D8	I/O
0	IO_L37N_0	D9	I/O
0	IO_L34N_0	D10	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IP_0	D12	INPUT
0	IO_L30P_0	D13	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_L48N_1	H24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O
1	IP_L52N_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_L65P_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	IP_L16P_1	W25	INPUT
1	IP_L24P_1	U25	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L20P_1	W26	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52P_1	G26	INPUT
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IO_L48P_3	T10	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L36N_3	R2	I/O
3	IO_L37P_3	R3	I/O
3	IO_L37N_3	R4	I/O
3	IO_L40P_3	R5	I/O
3	IO_L40N_3	R6	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L41P_3	P8	I/O
3	IO_L41N_3	P9	I/O
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L31P_3	N1	I/O
3	IO_L31N_3	N2	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28P_3	M5	I/O
3	IO_L28N_3	M6	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IO_L18N_3	L7	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IP_L24N_3	K1	INPUT
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_L12N_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_L16N_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_L04N_3/VREF_3	C1	VREF

XC3SD3400A FPGA

Table 68 lists all the FG676 package pins for the XC3SD3400A FPGA. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. Table 68 also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Note: The grayed boxes denote a difference between the XC3SD1800A and the XC3SD3400A devices.

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA**

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L43N_0	K11	I/O
0	IO_L39N_0	K12	I/O
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L12N_0	K16	I/O
0	IP_0	J10	INPUT
0	IO_L43P_0	J11	I/O
0	IO_L39P_0	J12	I/O
0	IP_0	J13	INPUT
0	IO_L25N_0/GCLK5	J14	GCLK
0	IP_0	J15	INPUT
0	IO_L12P_0	J16	I/O
0	IP_0/VREF_0	J17	VREF
0	IO_L47N_0	H9	I/O
0	IO_L46N_0	H10	I/O
0	IO_L35N_0	H12	I/O
0	IP_0	H13	INPUT
0	IO_L16N_0	H15	I/O
0	IO_L08P_0	H17	I/O
0	IP_0	H18	INPUT
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L47P_0	G9	I/O
0	IO_L46P_0	G10	I/O
0	IP_0/VREF_0	G11	VREF
0	IO_L35P_0	G12	I/O
0	IO_L27N_0/GCLK9	G13	GCLK
0	IP_0	G14	INPUT
0	IO_L16P_0	G15	I/O
0	IO_L08N_0	G17	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L01P_0	G20	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L48P_0	F7	I/O
0	IO_L52P_0/VREF_0	F8	VREF
0	IO_L31N_0	F12	I/O
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L24N_0	F14	I/O
0	IO_L20P_0	F15	I/O
0	IO_L13P_0	F17	I/O
0	IO_L02N_0	F19	I/O
0	IO_L01N_0	F20	I/O
0	IO_L48N_0	E7	I/O
0	IO_L37P_0	E10	I/O
0	IP_0	E11	INPUT
0	IO_L31P_0	E12	I/O
0	IO_L24P_0	E14	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L13N_0	E17	I/O
0	IP_0	E18	INPUT
0	IO_L10P_0	E21	I/O
0	IO_L44N_0	D6	I/O
0	IP_0/VREF_0	D7	VREF
0	IO_L40N_0	D8	I/O
0	IO_L37N_0	D9	I/O
0	IO_L34N_0	D10	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IP_0	D12	INPUT
0	IO_L30P_0	D13	I/O
0	IP_0/VREF_0	D14	VREF
0	IO_L22P_0	D16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L17P_0	D18	I/O
0	IO_L11P_0	D20	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF

FG676 Footprint – XC3SD3400A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

34 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

37 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

4 **JTAG:** Dedicated JTAG port pins.

100 **GND:** Ground

40 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with question marks inside indicate pin differences from the XC3SD1800A device. Please see the Footprint Migration Differences section for more information.

	Bank 0												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	GND ▽	GND	VCCO_0 ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT VREF_3 ▽	VCCO_3 ▽	GND	VCCINT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	VCCAUX ▽	GND ▽	I/O L06P_3	TMS	VCCINT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VCCINT ▽	I/O L48N_0	VCCO_0	GND ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	VCCAUX ▽	VCCINT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT ▽	GND ▽	I/O L14P_3	I/O L09N_3	GND ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT ▽	VCCINT ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	VCCINT ▽	I/O L05N_2	I/O L12P_2	VCCINT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	GND ▽	INPUT VREF_3 ▽	GND	I/O L02N_2 CSO_B	VCCINT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	GND ▽	VCCAUX ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	GND ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	GND ▽	I/O L08P_2	GND ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	GND ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	VCCAUX ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	VCCO_2 ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Left Half)**