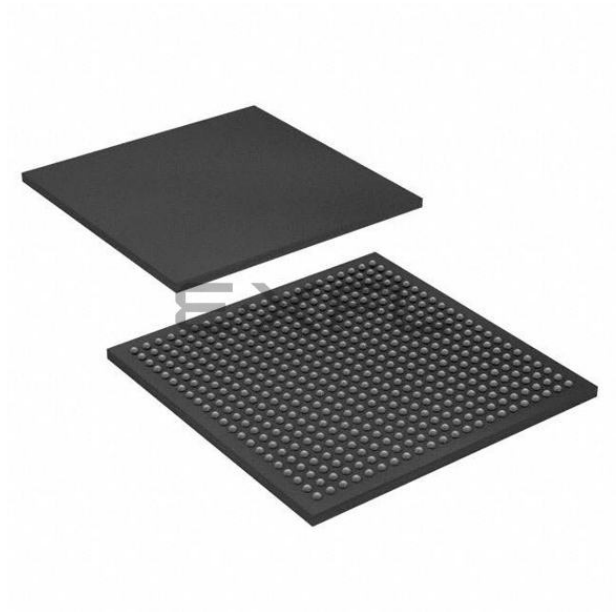

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4cs484i

Configuration

Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A DSP FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications
- Spartan-3A DSP FPGAs support the following differential standards:
- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Device	CS484 CSG484		FG676 FGG676	
	User	**Diff**	**User**	**Diff**
XC3SD1800A	**309**(1) *(60)*	**140** *(78)*	**519** *(110)*	**227** *(131)*
XC3SD3400A	**309** *(60)*	**140** *(78)*	**469** *(60)*	**213** *(117)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Spartan-3A DSP FPGA Design Documentation

The functionality of the Spartan®-3A DSP FPGA family is described in the following documents. The topics covered in each guide are listed.

- DS706: E*xtended Spartan-3A Family Overview*
- UG331**:** *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- UG332**:** *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*
  - XtremeDSP DSP48A Slices
  - XtremeDSP DSP48A Pre-Adder

For specific hardware examples, please see the Spartan-3A DSP FPGA Starter Kit board web pages.

- **XtremeDSP Starter Platform—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/HW-SD1800A-DSP-SB-UNI-G.htm
- **XtremeDSP Starter Kit—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-DSP-SK-UNI-G.htm
- **XtremeDSP Video Starter Kit—Spartan-3A DSP Edition**
  http://www.xilinx.com/products/devkits/DO-S3ADSP-VIDEO-SK-UNI-G.htm
- **Embedded Development HW/SW Kit—Spartan-3A DSP S3D1800A MicroBlaze Processor Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-EDK-DK-UNI-G.htm

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General Recommended Operating Conditions

Table 7: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage (2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN} (3)	Input voltage	PCI™ IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# (4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time (5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 10 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 12 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Table 21: **Propagation Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XC3SD1800A	1.79	2.04	ns
				XC3SD3400A	1.65	2.11	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XC3SD1800A	2.23	2.47	ns
			2		2.81	3.06	ns
			3		3.39	3.86	ns
			4		3.89	4.43	ns
			5		3.83	4.39	ns
			6		4.61	5.32	ns
			7		5.40	6.24	ns
			8		5.93	6.86	ns
			1	XC3SD3400A	2.21	2.67	ns
			2		2.71	3.25	ns
			3		3.58	4.04	ns
			4		4.15	4.62	ns
			5		4.03	4.49	ns
			6		4.57	5.31	ns
			7		5.34	6.18	ns
			8		5.84	6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Table 26: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs[2]		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V)**

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS12	Slow	2	40	40
		4	–	25
		6	–	18
	Fast	2	31	31
		4	–	13
		6	–	9
	QuietIO	2	55	55
		4	–	36
		6	–	36
PCI33_3			16	16
PCI66_3			–	13
HSTL_I			–	20
HSTL_III			–	8
HSTL_I_18			17	17
HSTL_II_18			–	5
HSTL_III_18			10	8
SSTL18_I			7	15
SSTL18_II			–	9
SSTL2_I			18	18
SSTL2_II			–	9
SSTL3_I			8	10
SSTL3_II			6	7

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)	Package Type	
	CS484, FG676	
	Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Differential Standards (Number of I/O Pairs or Channels)		
LVDS_25	22	–
LVDS_33	27	–
BLVDS_25	4	4
MINI_LVDS_25	22	–
MINI_LVDS_33	27	–
LVPECL_25	Inputs Only	
LVPECL_33	Inputs Only	
RSDS_25	22	–
RSDS_33	27	–
TMDS_33	27	–
PPDS_25	22	–
PPDS_33	27	–
DIFF_HSTL_I_18	8	8
DIFF_HSTL_II_18	–	2
DIFF_HSTL_III_18	5	4
DIFF_HSTL_I	–	10
DIFF_HSTL_III	–	4
DIFF_SSTL18_I	3	7
DIFF_SSTL18_II	–	4
DIFF_SSTL2_I	9	9
DIFF_SSTL2_II	–	4
DIFF_SSTL3_I	4	5
DIFF_SSTL3_II	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

DSP48A Timing

To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.

Table 34: **Setup Times for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times of Data/Control Pins to the Input Register Clock							
T_{DSPDCK_AA}	A input to A register CLK	–	–	–	0.04	0.04	ns
T_{DSPDCK_DB}	D input to B register CLK	Yes	–	–	1.64	1.88	ns
T_{DSPDCK_CC}	C input to C register CLK	–	–	–	0.05	0.05	ns
T_{DSPDCK_DD}	D input to D register CLK	–	–	–	0.04	0.04	ns
T_{DSPDCK_OPB}	OPMODE input to B register CLK	Yes	–	–	0.37	0.42	ns
T_{DSPDCK_OPOP}	OPMODE input to OPMODE register CLK	–	–	–	0.06	0.06	ns
Setup Times of Data Pins to the Pipeline Register Clock							
T_{DSPDCK_AM}	A input to M register CLK	–	Yes	–	3.30	3.79	ns
T_{DSPDCK_BM}	B input to M register CLK	Yes	Yes	–	4.33	4.97	ns
		No	Yes	–	3.30	3.79	ns
T_{DSPDCK_DM}	D input to M register CLK	Yes	Yes	–	4.41	5.06	ns
T_{DSPDCK_OPM}	OPMODE to M register CLK	Yes	Yes	–	4.72	5.42	ns
Setup Times of Data/Control Pins to the Output Register Clock							
T_{DSPDCK_AP}	A input to P register CLK	–	Yes	Yes	4.78	5.49	ns
T_{DSPDCK_BP}	B input to P register CLK	Yes	Yes	Yes	5.87	6.74	ns
		No	Yes	Yes	4.77	5.48	ns
T_{DSPDCK_DP}	D input to P register CLK	Yes	Yes	Yes	5.95	6.83	ns
T_{DSPDCK_CP}	C input to P register CLK	–	–	Yes	1.90	2.18	ns
T_{DSPDCK_OPP}	OPMODE input to P register CLK	Yes	Yes	Yes	6.25	7.18	ns

Notes:

1. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
2. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.2	333(5)	0.2	333(5)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.
5. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL} T_{SCCH}	CCLK Low and High time	5	∞	ns

Serial Peripheral Interface (SPI) Configuration Timing

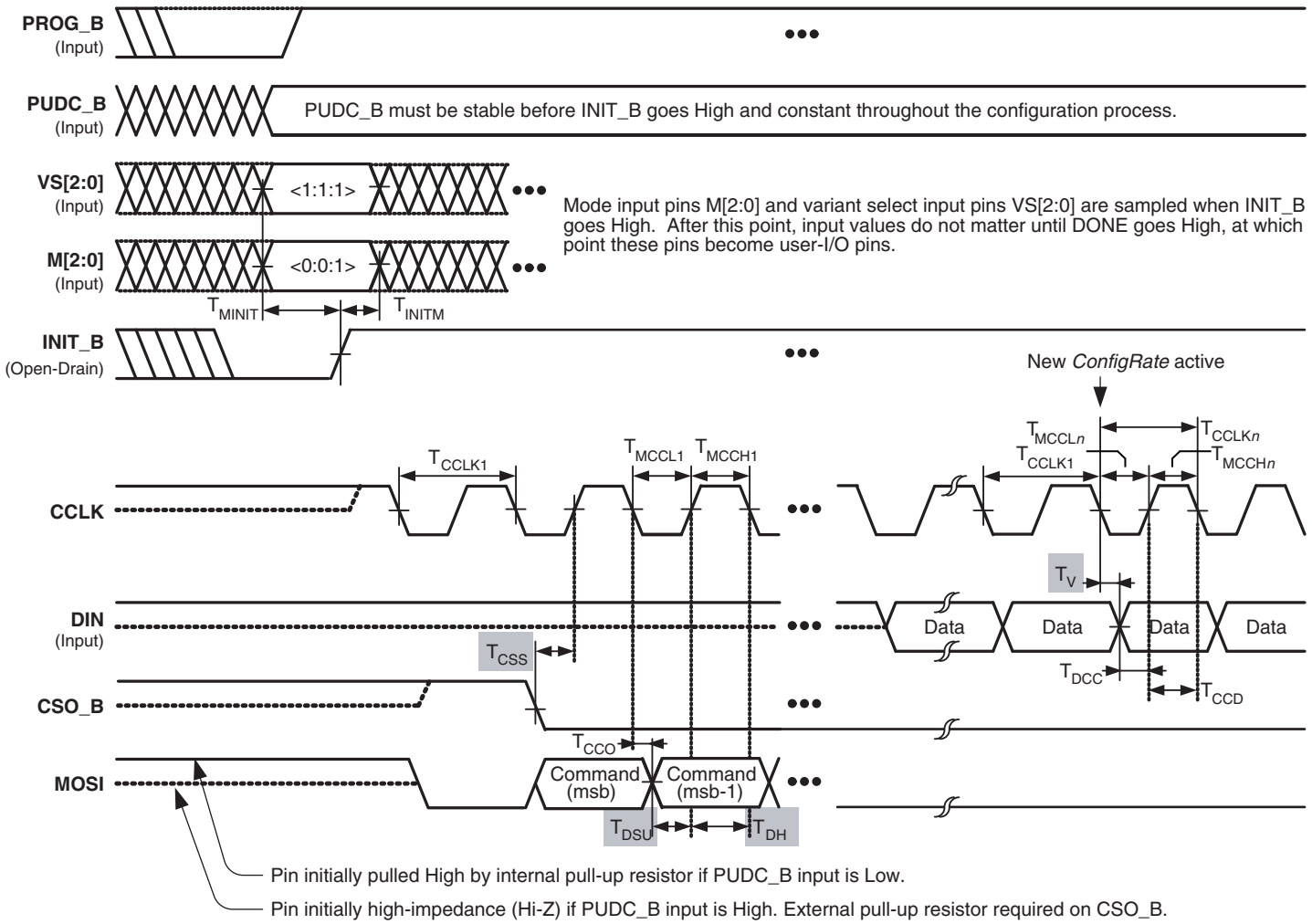

Figure 13: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 52: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on DIN data input before CCLK rising edge	See Table 50		
T_{CCD}	Hold time on DIN data input after CCLK rising edge	See Table 50		

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in UG331: *Spartan-3 Generation FPGA User Guide.*

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs**

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

CS484: 484-Ball Chip-Scale Ball Grid Array

The 484-ball chip-scale ball grid array, CS484, supports both the XC3SD1800A and XC3SD3400A FPGAs. There are no pinout differences between the two devices.

Table 63 lists all the CS484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 63: **Spartan-3A DSP CS484 Pinout**

Bank	Pin Name	CS484 Ball	Type
0	IO_L30N_0	A3	I/O
0	IO_L28N_0	A4	I/O
0	IO_L25N_0	A5	I/O
0	IO_L25P_0	A6	I/O
0	IO_L24N_0/VREF_0	A7	VREF
0	IO_L20P_0/GCLK10	A8	GCLK
0	IO_L18P_0/GCLK6	A9	GCLK
0	IP_0	A10	INPUT
0	IO_L15N_0	A11	I/O
0	IP_0	A12	INPUT
0	IO_L11P_0	A13	I/O
0	IO_L10P_0	A14	I/O
0	IP_0	A15	INPUT
0	IO_L06P_0/VREF_0	A16	VREF
0	IO_L06N_0	A17	I/O
0	IP_0	A18	INPUT
0	IO_L07N_0	A19	I/O
0	IO_0	A20	I/O
0	IO_L30P_0	B3	I/O
0	IO_L28P_0	B4	I/O
0	IO_L24P_0	B6	I/O
0	IO_L20N_0/GCLK11	B8	GCLK
0	IO_L18N_0/GCLK7	B9	GCLK
0	IO_L15P_0	B11	I/O
0	IO_L11N_0	B13	I/O
0	IO_L10N_0	B15	I/O
0	IO_L03P_0	B17	I/O
0	IO_L02N_0	B19	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L07P_0	B20	I/O
0	IO_L29N_0	C4	I/O
0	IP_0	C5	INPUT
0	IO_L21P_0	C6	I/O
0	IO_L26P_0	C7	I/O
0	IO_L22P_0	C8	I/O
0	IO_L16P_0	C9	I/O
0	IP_0	C10	INPUT
0	IP_0/VREF_0	C11	VREF
0	IO_L14N_0	C12	I/O
0	IO_L14P_0	C13	I/O
0	IP_0	C14	INPUT
0	IO_L12N_0/VREF_0	C15	VREF
0	IO_L08N_0	C16	I/O
0	IO_L03N_0	C17	I/O
0	IO_L02P_0/VREF_0	C18	VREF
0	IO_L01N_0	C19	I/O
0	IO_L29P_0	D5	I/O
0	IO_L21N_0	D6	I/O
0	IO_L26N_0	D7	I/O
0	IO_L22N_0	D9	I/O
0	IO_L16N_0	D10	I/O
0	IO_L09N_0	D13	I/O
0	IO_L12P_0	D14	I/O
0	IO_L08P_0	D15	I/O
0	IP_0	D17	INPUT
0	IP_0	D18	INPUT
0	IO_L01P_0	D19	I/O
0	IP_0	E6	INPUT
0	IO_L31P_0/VREF_0	E7	VREF
0	IO_L27N_0	E8	I/O
0	IP_0	E10	INPUT
0	IO_L19N_0/GCLK9	E11	GCLK
0	IO_L17P_0/GCLK4	E12	GCLK
0	IO_L09P_0	E13	I/O
0	IO_L05P_0	E15	I/O
0	IO_L04P_0	E16	I/O
0	IP_0	E17	INPUT
0	IO_L31N_0/PUDC_B	F7	DUAL
0	IO_L27P_0	F8	I/O
0	IO_L23N_0	F9	I/O

CS484 Footprint

Left Half of Package (Top View)

156 **I/O:** Unrestricted, general-purpose user I/O.

41 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

28 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins.

4 **JTAG:** Dedicated JTAG port pins.

84 **GND:** Ground.

24 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	I/O L30N_0	I/O L28N_0	I/O L25N_0	I/O L25P_0	I/O L24N_0 VREF_0	I/O L20P_0 GCLK10	I/O L18P_0 GCLK6	INPUT	I/O L15N_0
B	TMS	VCCAUX	I/O L30P_0	I/O L28P_0	VCCO_0	I/O L24P_0	GND	I/O L20N_0 GCLK11	I/O L18N_0 GCLK7	VCCO_0	I/O L15P_0
C	I/O L02N_3	I/O L02P_3	GND	I/O L29N_0	INPUT	I/O L21P_0	I/O L26P_0	I/O L22P_0	I/O L16P_0	INPUT	INPUT 0 VREF_0
D	INPUT L04P_3	TDI	INPUT L08P_3	INPUT L08N_3	I/O L29P_0	I/O L21N_0	I/O L26N_0	GND	I/O L22N_0	I/O L16N_0	GND
E	INPUT L04N_3 VREF_3	VCCO_3	I/O L09P_3	I/O L09N_3	VCCAUX	INPUT	I/O L31P_0 VREF_0	I/O L27N_0	VCCO_0	INPUT	I/O L19N_0 GCLK9
F	I/O L06N_3	I/O L06P_3	I/O L01P_3	I/O L03P_3	I/O L03N_3	GND	I/O L31N_0 PUDC_B	I/O L27P_0	I/O L23N_0	I/O L19P_0 GCLK8	I/O L17N_0 GCLK5
G	I/O L11P_3	GND	I/O L01N_3	GND	I/O L07P_3	I/O L07N_3	VCCINT	I/O L23P_0	GND	VCCAUX	GND
H	I/O L11N_3	I/O L14P_3	I/O L05P_3	I/O L05N_3	I/O L10P_3	I/O L10N_3	GND	GND	VCCINT	GND	VCCINT
J	I/O L14N_3 VREF_3	VCCO_3	INPUT L16P_3	INPUT L16N_3	VCCO_3	INPUT L12P_3	INPUT L12N_3 VREF_3	VCCINT	GND	VCCINT	GND
K	I/O L19P_3 LHCLK2	I/O L17P_3	I/O L17N_3	I/O L13P_3	I/O L13N_3	I/O L15P_3	VCCAUX	GND	VCCINT	GND	VCCINT
L	I/O L19N_3 IRDY2 LHCLK3	GND	I/O L20P_3 LHCLK4	VCCAUX	I/O L15N_3	I/O L18P_3 LHCLK0	GND	VCCINT	GND	VCCINT	GND
M	I/O L22P_3 VREF_3	I/O L20N_3 LHCLK5	INPUT L23P_3	GND	I/O L18N_3 LHCLK1	I/O L21P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	GND	VCCINT
N	I/O L22N_3	VCCO_3	INPUT L31P_3	INPUT L23N_3	I/O L24N_3	I/O L24P_3	I/O L21N_3 LHCLK7	VCCINT	GND	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT L31N_3	I/O L32P_3 VREF_3	VCCO_3	I/O L26P_3	VCCAUX	GND	VCCINT	GND	VCCINT
R	I/O L28N_3	I/O L28P_3	I/O L34P_3	GND	I/O L32N_3	I/O L26N_3	GND	VCCINT	GND	VCCINT	GND
T	I/O L30P_3	GND	INPUT L27P_3	I/O L34N_3	I/O L29N_3	I/O L29P_3	VCCINT	GND	VCCAUX	GND	VCCAUX
U	I/O L30N_3	I/O L33P_3	INPUT L27N_3	I/O L38P_3	I/O L38N_3	GND	I/O L02N_2 CSO_B	I/O L11N_2	I/O L10N_2	I/O L14N_2 D4	GND
V	I/O L33N_3	VCCO_3	I/O L36N_3	I/O L36P_3	VCCAUX	I/O L02P_2 M2	I/O L11P_2	I/O L06N_2	VCCO_2	I/O L10P_2	I/O L14P_2 D5
W	I/O L35N_3	I/O L37N_3	I/O L37P_3	INPUT 2 VREF_2	I/O L03P_2	I/O L07N_2 VS2	GND	I/O L06P_2	INPUT 2 VREF_2	INPUT	VCCAUX
Y	I/O L35P_3	INPUT L39P_3	GND	I/O L03N_2	I/O L07P_2 RDWR_B	INPUT	INPUT	I/O L13P_2	I/O L13N_2	I/O L15N_2 GCLK13	I/O L15P_2 GCLK12
AA	INPUT L39N_3 VREF_3	VCCAUX	I/O L01P_2 M1	I/O L04N_2	VCCO_2	INPUT	GND	I/O L08N_2	VCCO_2	I/O L12N_2 D6	GND
AB	GND	INPUT 2 VREF_2	I/O L01N_2 M0	I/O L04P_2	I/O L05P_2	I/O L05N_2	I/O L08P_2	I/O L09P_2 VS1	I/O L09N_2 VS0	I/O L12P_2 D7	INPUT 2 VREF_2

Bank 3 (left) **Bank 2** (bottom)

Figure 15: **CS484 Package Footprint (Top View–Left Half)**

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_L16N_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_L20N_1/VREF_1	V26	VREF
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_L24N_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IP_L04P_3	C2	INPUT
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L16P_3	G2	INPUT
3	IP_L12P_3	G5	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L58P_3	AA4	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L54N_3	Y4	INPUT
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IP_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	H25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_3/VREF_3	C1	VREF
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_3/VREF_3	AA5	VREF
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	C2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	W25	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	U25	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND

Footprint Migration Differences

There are multiple migration footprint differences between the XC3SD1800A and the XC3SD3400A in the FG676 package. These migration footprint differences are shown in Table 70. Migration from the XC3S1400A Spartan-3A device in the FG676 package to a Spartan-3A DSP device in the FG676 package is also possible. The XC3S1800A pin migration differences have been added to Table 70 for designs migrating between these devices.

Table 70: **FG676 Footprint Migration Differences**

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
G16	IP_0	0	IP_0	0	GND	GND	G16
G18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	G18
F9	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	F9
F10	IP_0	0	IP_0	0	VCCINT	VCCINT	F10
F18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	F18
E6	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	E6
E9	N.C.	N.C.	IP_0	0	GND	GND	E9
E20	IP_0	0	IP_0	0	VCCAUX	VCCAUX	E20
D5	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	D5
D15	IP_0	0	IP_0	0	GND	GND	D15
D19	IP_0	0	IP_0	0	GND	GND	D19
C4	IP_0	0	IP_0	0	VCCINT	VCCINT	C4
B24	N.C.	N.C.	IP_0	0	GND	GND	B24
A5	IP_0	0	IP_0	0	GND	GND	A5
A7	IP_0	0	IP_0	0	VCCO_0	0	A7
A23	IP_0	0	IP_0	0	GND	GND	A23
A24	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	A24
Y26	IP_L16N_1	1	IP_L16N_1	1	IP_1	1	Y26
W25	IP_L16P_1	1	IP_L16P_1	1	GND	GND	W25
W26	IP_L20P_1	1	IP_L20P_1	1	VCCAUX	VCCAUX	W26
V26	IP_L20N_1/ VREF_1	1	IP_L20N_1/ VREF_1	1	IP_1/VREF_1	1	V26
U25	IP_L24P_1	1	IP_L24P_1	1	GND	GND	U25
U26	IP_L24N_1/ VREF_1	1	IP_L24N_1/ VREF_1	1	IP_1/VREF_1	1	U26
H23	IP_L48P_1	1	IP_L48P_1	1	VCCAUX	VCCAUX	H23
H24	IP_L48N_1	1	IP_L48N_1	1	IP_1	1	H24
H25	IP_L44N_1	1	IP_L44N_1	1	VCCO_1	1	H25
H26	IP_L44P_1/ VREF_1	1	IP_L44P_1/ VREF_1	1	IP_1/VREF_1	1	H26
G25	IP_L52N_1/ VREF_1	1	IP_L52N_1/ VREF_1	1	IP_1/VREF_1	1	G25
G26	IP_L52P_1	1	IP_L52P_1	1	VCCAUX	VCCAUX	G26
B25	IP_L65N_1	1	IP_L65N_1	1	GND	GND	B25
B26	IP_L65P_1/ VREF_1	1	IP_L65P_1/ VREF_1	1	IP_1/VREF_1	1	B26