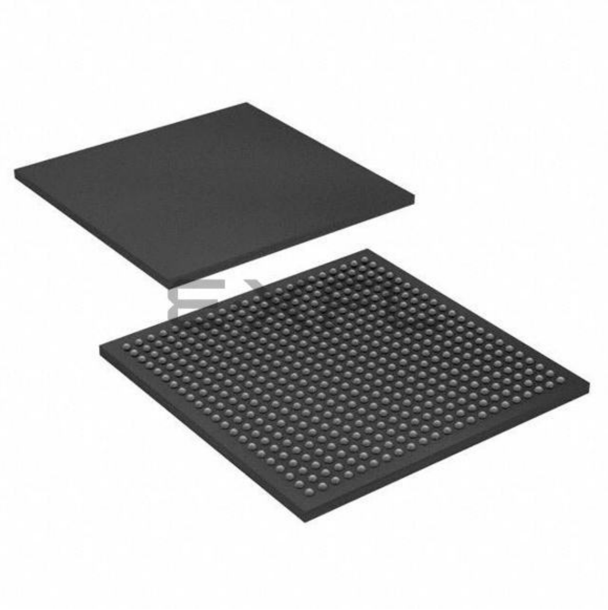
AMD Xilinx - XC3SD3400A-4CSG484I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4csg484i

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options.
06/02/08	2.1	Added reference to SCD 4103 for 750 Mbps performance. Add dual mark clarification to Package Marking. Updated links.
03/11/09	2.2	Simplified ordering information. Removed reference to SCD 4103.
10/04/10	3.0	Updated the Notice of Disclaimer section.

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External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

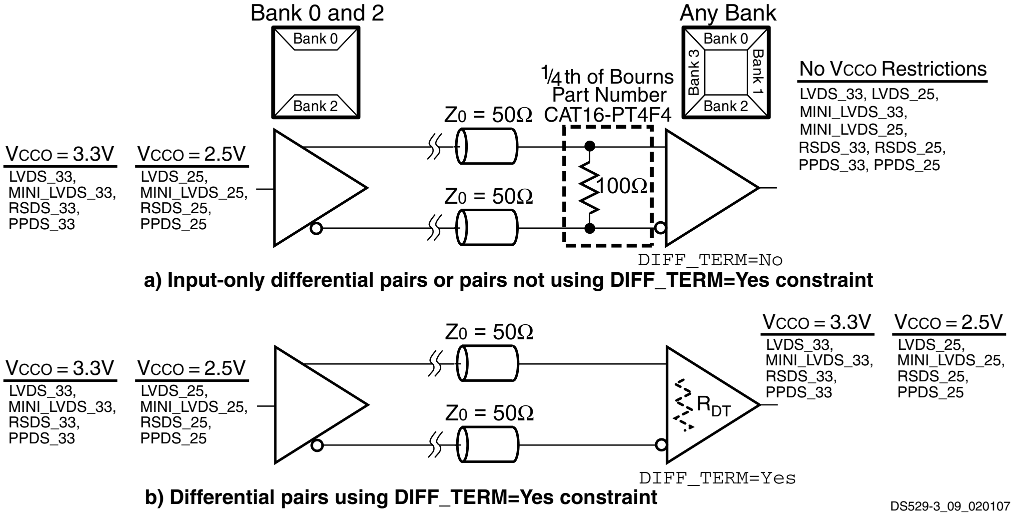

Figure 5: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

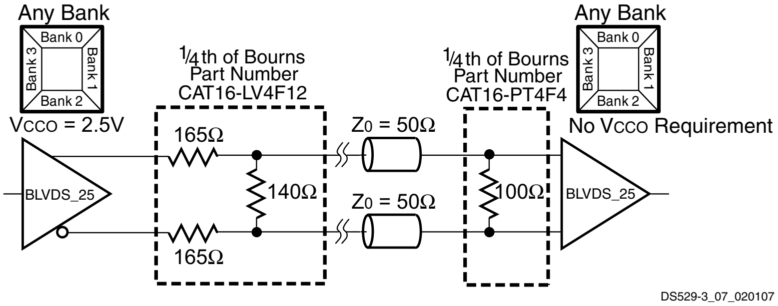

Figure 6: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

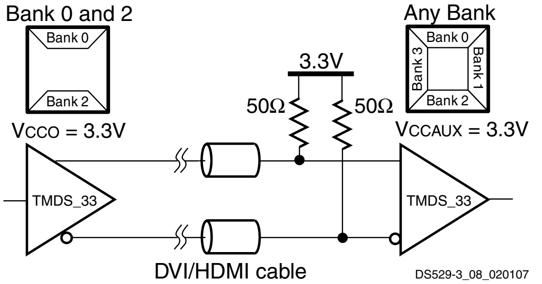

Figure 7: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 14: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A DSP FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 15. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs will require updating the Xilinx ISE development software with a future version and/or Service Pack.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 15. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 15: **Spartan-3A DSP v1.32 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3SD1800A			-4, -5
XC3SD3400A			-4, -5

Table 16 provides the recent history of the Spartan-3A DSP FPGA speed files.

Table 16: **Spartan-3A DSP Speed File Version History**

Version	ISE Release	Description
1.32	ISE 10.1.02	Updated DSP timing model to reflect higher performance for some implementations
1.31	ISE 10.1	Added Automotive support
1.30	ISE 9.2.03i	Added absolute minimum values
1.29	ISE 9.2.01i	Production Speed Files for -4 and -5 speed grades
1.28	ISE 9.2i	Minor updates
1.27	ISE 9.1.03i	Advance Speed Files for -4 speed grade

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 17: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25[(2)], 12 mA output drive, Fast slew rate, with DCM[(3)]	XC3SD1800A	3.28	3.51	ns
			XC3SD3400A	3.36	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25[(2)], 12 mA output drive, Fast slew rate, without DCM	XC3SD1800A	5.23	5.58	ns
			XC3SD3400A	5.51	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 22. If the latter is true, *add* the appropriate Output adjustment from Table 25.
3. DCM output jitter is included in all measurements.

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			**Package Type**	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	**Left, Right** (Banks 1, 3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	–	11
		24	–	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	–	3
		24	–	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	–	36
		24	–	8

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			**Package Type**	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	**Left, Right** (Banks 1, 3)
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	–	13
		16	–	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	–	4
		16	–	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	–	36
		16	–	24
LVCMOS15	Slow	2	55	55
		4	31	31
		6	18	18
		8	–	15
		12	–	10
	Fast	2	25	25
		4	10	10
		6	6	6
		8	–	4
		12	–	3
	QuietIO	2	70	70
		4	40	40
		6	31	31
		8	–	31
		12	–	20

Table 30: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.44	–	1.72	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
$T_{AH,}$ T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Table 31: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

DNA Port Timing

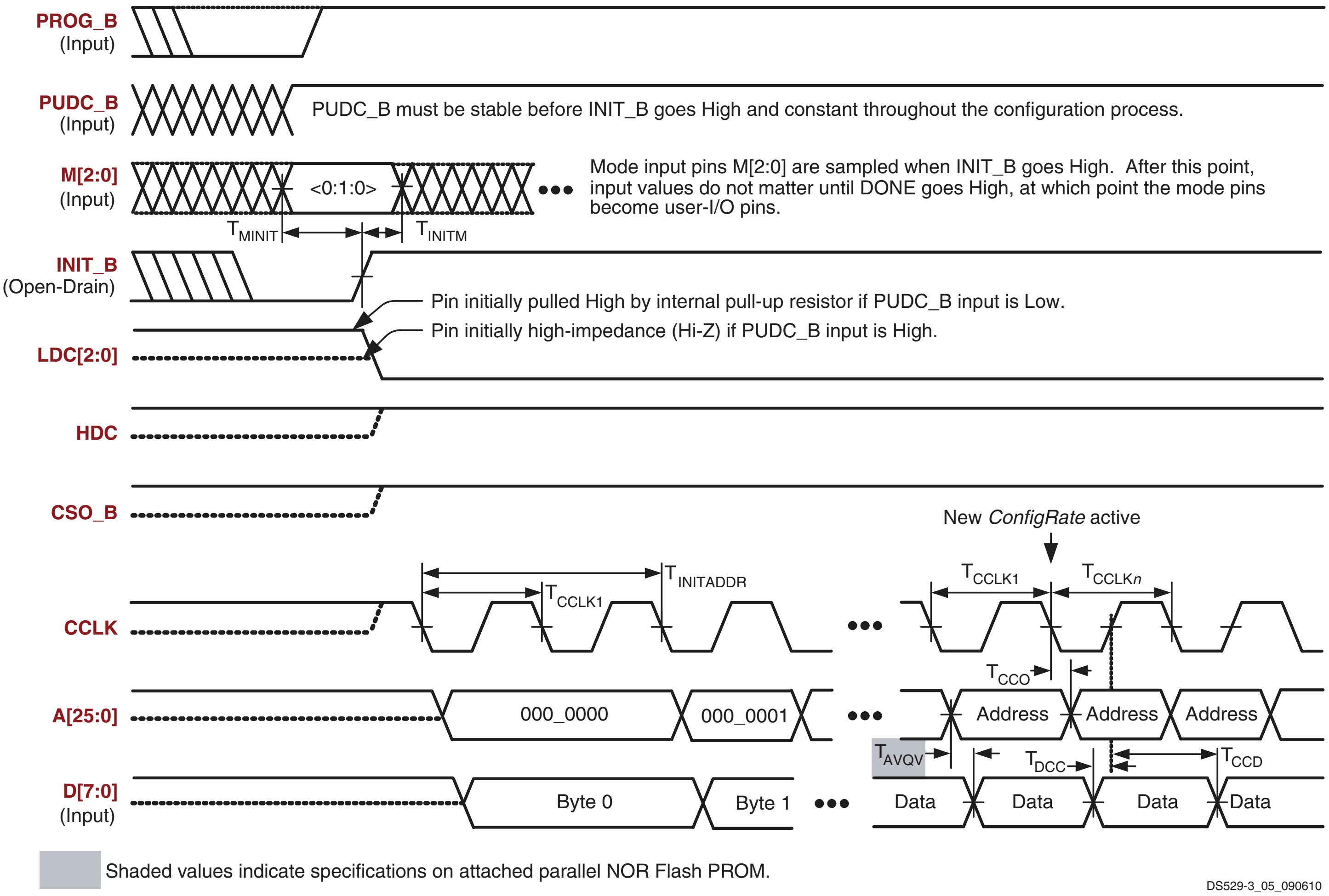
Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Byte Peripheral Interface (BPI) Configuration Timing



PUDC_B must be stable before INIT_B goes High and constant throughout the configuration process.

Mode input pins M[2:0] are sampled when INIT_B goes High. After this point, input values do not matter until DONE goes High, at which point the mode pins become user-I/O pins.

Pin initially pulled High by internal pull-up resistor if PUDC_B input is Low.

Pin initially high-impedance (Hi-Z) if PUDC_B input is High.

New *ConfigRate* active

▨ Shaded values indicate specifications on attached parallel NOR Flash PROM.

Figure 14: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Spartan-3A DSP FPGA Family: Pinout Descriptions

DS610 (v3.0) October 4, 2010 **Product Specification**

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in UG331: *Spartan-3 Generation FPGA User Guide.*

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs**

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Table 57: **Types of Pins on Spartan-3A DSP FPGAs *(Cont'd)***

Type/Color Code	Description	Pin Name(s) in Type
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected. Set on board and using CONFIG VCCAUX constraint.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 58.

Table 58: **Power and Ground Supply Pins by Package**

Package	Device	VCCINT	VCCAUX	VCCO	GND
CS484	XC3SD1800A	36	24	24	84
	XC3SD3400A	36	24	24	84
FG676	XC3SD1800A	23	14	36	77
	XC3SD3400A	36	24	40	100

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 59. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the *Using I/O Resources* chapter in UG331.

Table 59: **Maximum User I/O by Package**

Package	Device	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF[1]	CLK	N.C.
CS484	XC3SD1800A	309	60	140	156	41	52	28	32	0
	XC3SD3400A	309	60	140	156	41	52	28	32	0
FG676	XC3SD1800A	519	110	227	314	82	52	39	32	0
	XC3SD3400A	469	60	213	314	34	52	37	32	0

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A DSP FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 62 provides the thermal characteristics for the various Spartan-3A DSP device package offerings. This information is also available using the Thermal Query tool.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 62: **Spartan-3A DSP FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
CS484 CSG484	XC3SD1800A	4.1	6.8	18.0	13.3	12.3	11.5	°C/W
	XC3SD3400A	3.5	5.6	16.9	12.2	11.0	10.4	°C/W
FG676 FGG676	XC3SD1800A	4.7	7.8	15.9	11.6	10.6	10.0	°C/W
	XC3SD3400A	3.8	6.4	14.7	10.5	9.4	8.9	°C/W

Right Half of CS484 Package (Top View)

Bank 0

12	13	14	15	16	17	18	19	20	21	22	
INPUT	I/O L11P_0	I/O L10P_0	INPUT	I/O L06P_0 VREF_0	I/O L06N_0	INPUT	I/O L07N_0	I/O 0	TCK	GND	A
GND	I/O L11N_0	VCCO_0	I/O L10N_0	GND	I/O L03P_0	VCCO_0	I/O L02N_0	I/O L07P_0	VCCAUX	TDO	B
I/O L14N_0	I/O L14P_0	INPUT	I/O L12N_0 VREF_0	I/O L08N_0	I/O L03N_0	I/O L02P_0 VREF_0	I/O L01N_0	GND	INPUT L39N_1	INPUT L39P_1 VREF_1	C
VCCAUX	I/O L09N_0	I/O L12P_0	I/O L08P_0	GND	INPUT	INPUT	I/O L01P_0	I/O L36P_1 A20	I/O L37P_1 A22	I/O L37N_1 A23	D
I/O L17P_0 GCLK4	I/O L09P_0	VCCO_0	I/O L05P_0	I/O L04P_0	INPUT	VCCAUX	I/O L36N_1 A21	I/O L35N_1	VCCO_1	I/O L33N_1	E
INPUT	I/O L13N_0	I/O L13P_0	I/O L05N_0	I/O L04N_0	GND	I/O L38N_1 A25	I/O L38P_1 A24	I/O L30N_1 A19	I/O L35P_1	I/O L33P_1	F
VCCAUX	GND	VCCAUX	GND	VCCINT	I/O L34P_1	I/O L34N_1	I/O L30P_1 A18	INPUT L31N_1	GND	I/O L28N_1	G
GND	VCCINT	GND	VCCINT	GND	I/O L26P_1 A14	I/O L26N_1 A15	GND	I/O L32N_1	INPUT L31P_1 VREF_1	I/O L28P_1	H
VCCINT	GND	VCCINT	GND	VCCAUX	I/O L29N_1 A17	VCCO_1	I/O L32P_1	I/O L25N_1 A13	INPUT L27P_1	INPUT L27N_1	J
GND	VCCINT	GND	VCCINT	I/O L29P_1 A16	INPUT L23N_1	I/O L24N_1	I/O L24P_1	I/O L25P_1 A12	VCCO_1	I/O L22N_1 A11	K
VCCINT	GND	VCCINT	GND	VCCAUX	I/O L21N_1 RHCLK7	INPUT L23P_1 VREF_1	GND	I/O L20N_1 RHCLK5	I/O L20P_1 RHCLK4	I/O L22P_1 A10	L
GND	VCCINT	GND	VCCINT	GND	I/O L18N_1 RHCLK1	I/O L21P_1 IRDY1 RHCLK6	VCCAUX	I/O L19N_1 TRDY1 RHCLK3	GND	I/O L17N_1 A9	M
VCCINT	GND	VCCINT	GND	VCCAUX	I/O L13P_1 A2	I/O L18P_1 RHCLK0	I/O L15N_1 A7	I/O L15P_1 A6	I/O L19P_1 RHCLK2	I/O L17P_1 A8	N
GND	VCCINT	GND	VCCINT	I/O L13N_1 A3	INPUT L12N_1 VREF_1	VCCO_1	I/O L10P_1	INPUT L16N_1	VCCO_1	I/O L14N_1 A5	P
VCCINT	GND	VCCINT	GND	GND	INPUT L12P_1	I/O L10N_1	I/O L07P_1	I/O L07N_1	INPUT L16P_1 VREF_1	I/O L14P_1 A4	R
GND	VCCAUX	GND	GND	VCCINT	I/O L05N_1	I/O L05P_1	GND	I/O L09N_1	GND	I/O L11N_1 VREF_1	T
I/O L17P_2 GCLK0	I/O L20P_2	I/O L25P_2	I/O L25N_2	I/O L28P_2	GND	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L09P_1	INPUT L08N_1 VREF_1	I/O L11P_1	U
I/O L17N_2 GCLK1	I/O L20N_2 MOSI CSI_B	VCCO_2	INPUT 2 VREF_2	I/O L28N_2	I/O L31N_2 CCLK	VCCAUX	SUSPEND	I/O L03N_1 A1	VCCO_1	INPUT L08P_1	V
GND	INPUT 2 VREF_2	I/O L21N_2	I/O L24P_2 INIT_B	GND	I/O L31P_2 D0 DIN/MISO	INPUT 2 VREF_2	I/O L03P_1 A0	INPUT L04N_1 VREF_1	INPUT L04P_1	I/O L06P_1	W
INPUT	I/O L21P_2	INPUT 2 VREF_2	I/O L24N_2 D3	I/O L29N_2	I/O L29P_2	I/O L26P_2 D2	I/O L26N_2 D1	GND	I/O L02P_1 LDC1	I/O L06N_1	Y
I/O L16P_2 GCLK14	VCCO_2	I/O L18N_2 GCLK3	I/O L19P_2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27N_2	I/O L30P_2	VCCAUX	I/O L02N_1 LDC0	AA
I/O L16N_2 GCLK15	I/O L18P_2 GCLK2	I/O L19N_2	INPUT	I/O L22N_2 DOUT	I/O L23P_2	I/O L23N_2	I/O L27P_2	I/O L30N_2	DONE	GND	AB

Bank 2

Figure 16: CS484 Package Footprint (Top View–Right Half)

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA** ***(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IP_2	AF7	INPUT
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA** ***(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
2	VCCO_2	AF7	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA** ***(Cont'd)***

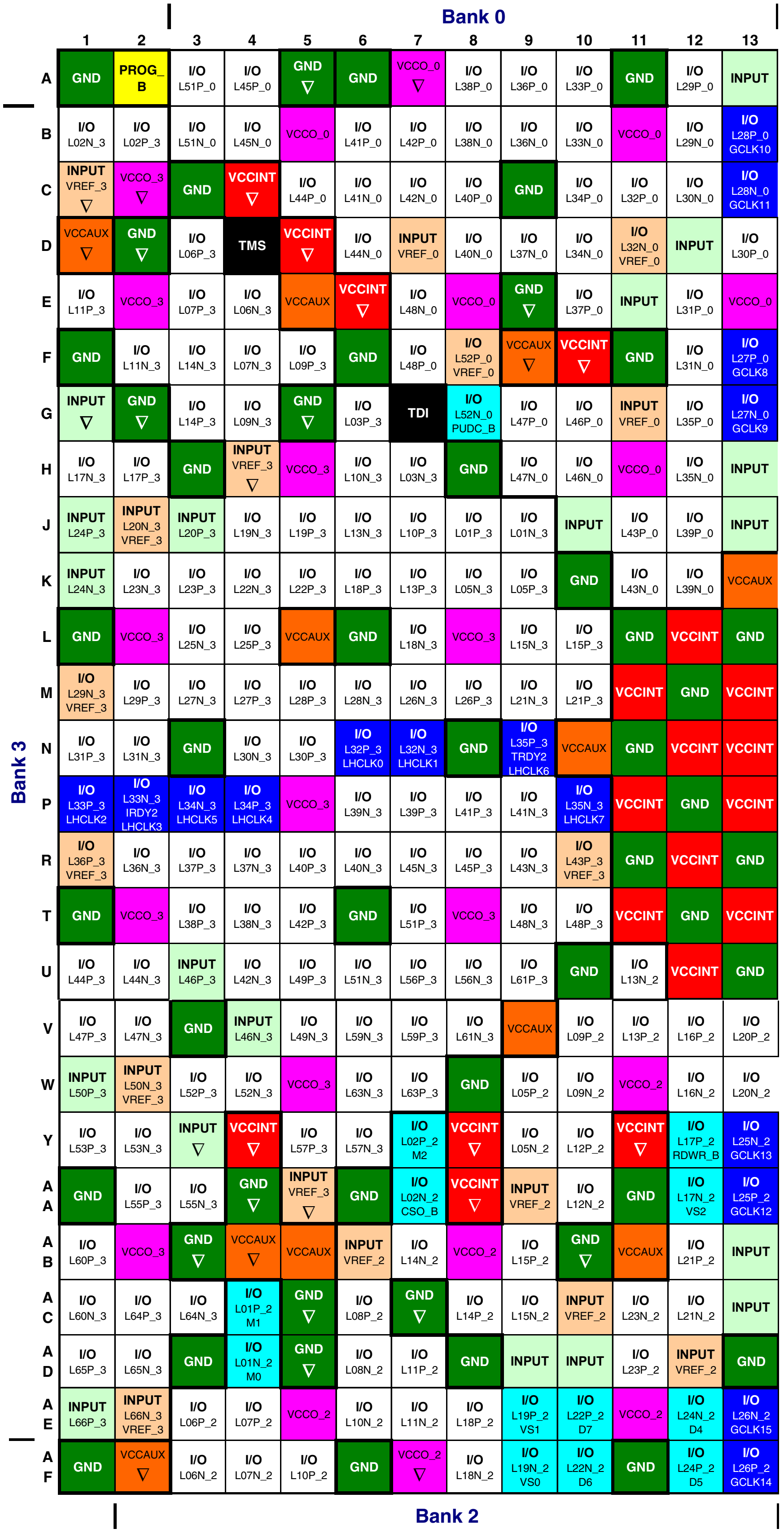
Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L36N_3	R2	I/O
3	IO_L37P_3	R3	I/O
3	IO_L37N_3	R4	I/O
3	IO_L40P_3	R5	I/O
3	IO_L40N_3	R6	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L41P_3	P8	I/O
3	IO_L41N_3	P9	I/O
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L31P_3	N1	I/O
3	IO_L31N_3	N2	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28P_3	M5	I/O
3	IO_L28N_3	M6	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L18N_3	L7	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IP_L24N_3	K1	INPUT

FG676 Footprint – XC3SD3400A FPGA

Left Half of Package (Top View)

314	**I/O:** Unrestricted, general-purpose user I/O.
34	**INPUT:** Unrestricted, general-purpose input pin.
51	**DUAL:** Configuration pins, then possible user I/O.
37	**VREF:** User I/O or input voltage reference for bank.
32	**CLK:** User I/O, input, or clock buffer input.
2	**CONFIG:** Dedicated configuration pins.
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
4	**JTAG:** Dedicated JTAG port pins.
100	**GND:** Ground
40	**VCCO:** Output voltage supply for bank.
36	**VCCINT:** Internal core supply voltage (+1.2V).
24	**VCCAUX:** Auxiliary supply voltage.

Note: The boxes with question marks inside indicate pin differences from the XC3SD1800A device. Please see the Footprint Migration Differences section for more information.



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	GND ▽	GND	VCCO_0 ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT VREF_3 ▽	VCCO_3 ▽	GND	VCCINT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	VCCAUX ▽	GND ▽	I/O L06P_3	TMS	VCCINT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VCCINT ▽	I/O L48N_0	VCCO_0	GND ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	VCCAUX ▽	VCCINT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT ▽	GND ▽	I/O L14P_3	I/O L09N_3	GND ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT ▽	VCCINT ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	VCCINT ▽	I/O L05N_2	I/O L12P_2	VCCINT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	GND ▽	INPUT VREF_3 ▽	GND	I/O L02N_2 CSO_B	VCCINT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	GND ▽	VCCAUX ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	GND ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	GND ▽	I/O L08P_2	GND ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	GND ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	VCCAUX ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	VCCO_2 ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Left Half)**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.1	Updates to Table 59, Table 63, Table 64, Table 65, Table 66, Table 67, Table 68, Table 69. Corrected VREF pins in XC3S1800A FG676 (Table 70). Updated FG676 package footprints for XC3SD1800A FPGA (Figure 16) and XC3SD3400A FPGA (Figure 17). Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options. Added advance thermal data to Table 62.
06/02/08	2.1	Added Package Overview section. Updated Thermal Characteristics in Table 62. Corrected name for AB14 in CS484 in Table 63. Updated links.
03/11/09	2.2	Corrected bank designation for SUSPEND to VCCAUX.
10/04/10	3.0	Revision update to match other data sheet modules.