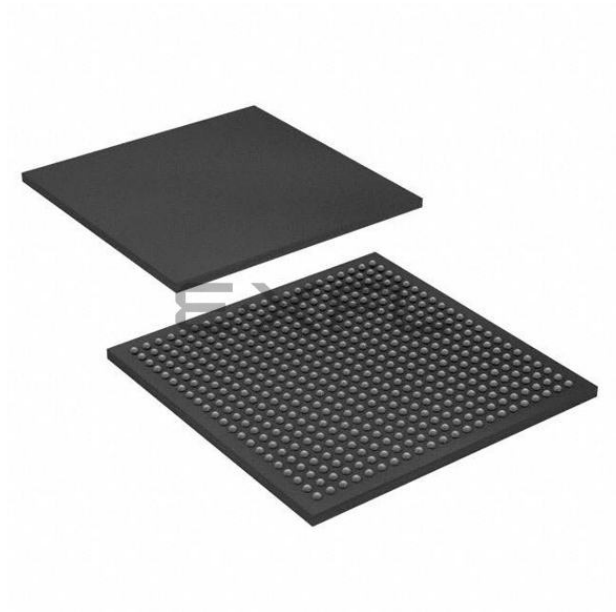
AMD Xilinx - XC3SD3400A-4CSG484LI Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4csg484li

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options.
06/02/08	2.1	Added reference to SCD 4103 for 750 Mbps performance. Add dual mark clarification to Package Marking. Updated links.
03/11/09	2.2	Simplified ordering information. Removed reference to SCD 4103.
10/04/10	3.0	Updated the Notice of Disclaimer section.

Notice of Disclaimer

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 3: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 3: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 4: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the UG331 chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the UG331 chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

Pin-to-Pin Setup and Hold Times

Table 18: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	2.65	3.11	ns
			XC3SD3400A	2.25	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	2.98	3.39	ns
			XC3SD3400A	2.78	3.08	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	–0.38	–0.38	ns
			XC3SD3400A	–0.26	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	–0.71	–0.71	ns
			XC3SD3400A	–0.65	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 19: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_ VALUE	Device	Speed		Units
					-5	-4	
					Min	Min	
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3SD1800A	–1.40	–1.40	ns
			2		–2.11	–2.11	ns
			3		–2.48	–2.48	ns
			4		–2.77	–2.77	ns
			5		–2.62	–2.62	ns
			6		–3.06	–3.06	ns
			7		–3.42	–3.42	ns
			8		–3.65	–3.65	ns
			1	XC3SD3400A	–1.31	–1.31	ns
			2		–1.88	–1.88	ns
			3		–2.44	–2.44	ns
			4		–2.89	–2.89	ns
			5		–2.83	–2.83	ns
			6		–3.33	–3.33	ns
			7		–3.63	–3.63	ns
			8		–3.96	–3.96	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 22.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 22. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 20: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON} (2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON} (2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Configurable Logic Block (CLB) Timing

Table 29: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0.00	–	0.00	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.00	–	0.00	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.2	333(5)	0.2	333(5)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.
5. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Phase Shifter (PS)

Table 40: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (FPSCLK)	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	–

Table 41: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS(2,3)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 40.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 37.

Miscellaneous DCM Timing

Table 42: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Suspend Mode Timing

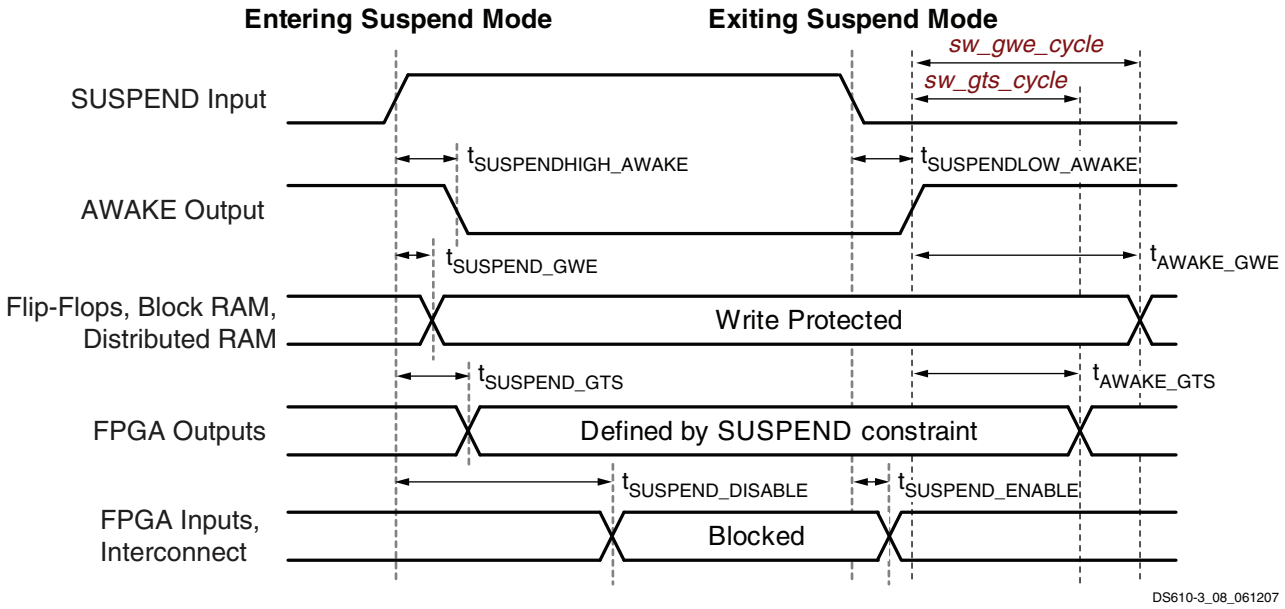


Figure 9: **Suspend Mode Timing**

Table 44: **Suspend Mode Timing Parameters**

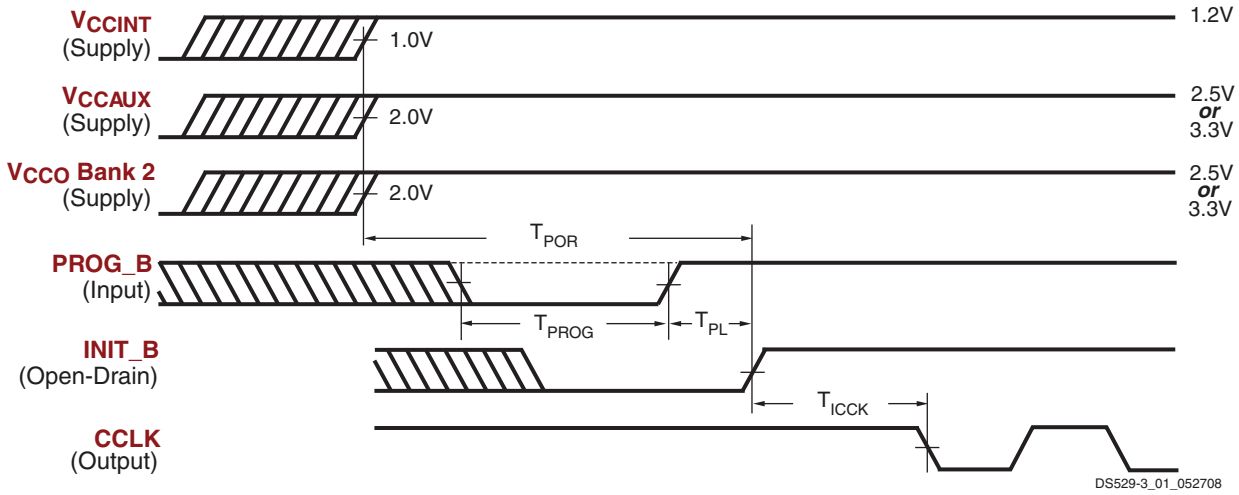
Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A DSP Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Master Serial and Slave Serial Mode Timing

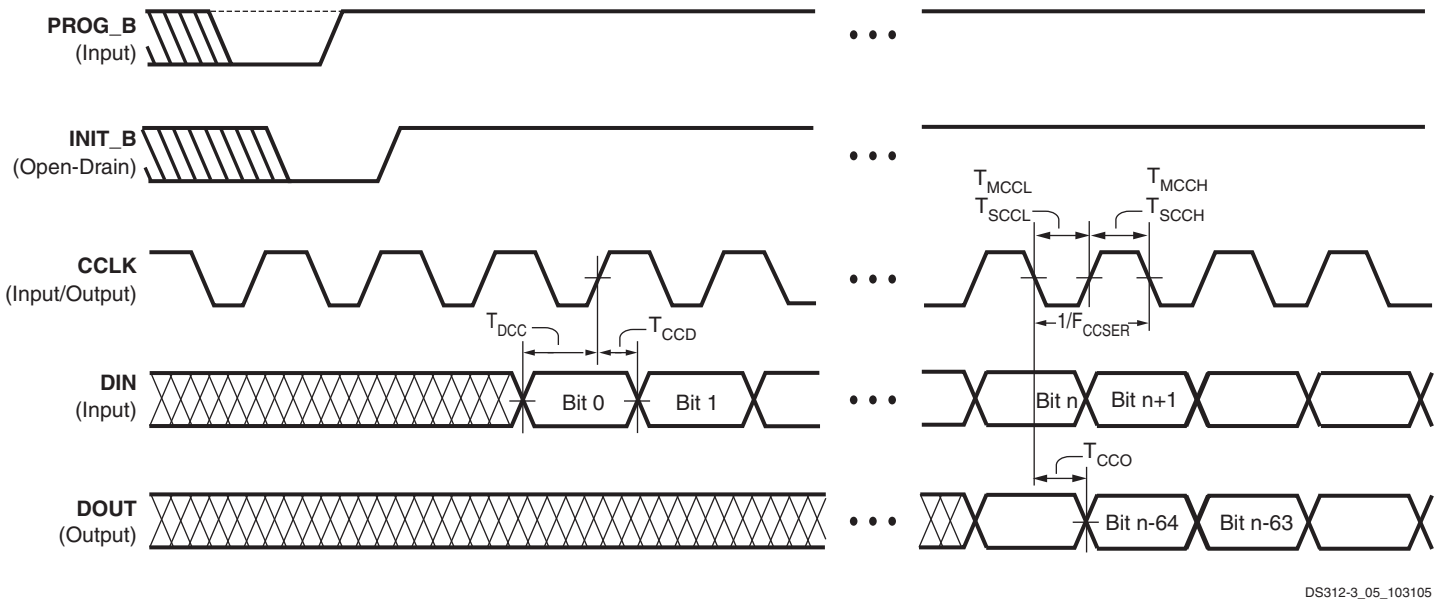


Figure 11: **Waveforms for Master Serial and Slave Serial Configuration**

Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0.0	–	ns
			Slave	1.0	–	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin(2)	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for v1.29 production speed files. Noted banking rules in Table 11 and Table 12. Added DIFF_HSTL_I and DIFF_HSTL_III to Table 12, Table 13, and Table 26. Updated TMDS DC characteristics in Table 13. Updated I/O Test Method values in Table 26. Added Simultaneously Switching Output limits in Table 28. Updated DSP48A timing symbols, descriptions, and values in Table 34. Added power-on timing in Table 45. Added CCLK specifications for Commercial in Table 46 through Table 48. Updated Slave Parallel timing in Table 51. Updated JTAG specifications in Table 56.
07/16/07	2.0	Added Low-power options and updated typical values for quiescent current in Table 9. Updated DSP48A timing in Table 34 and Table 35.
06/02/08	2.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 4 and updated V_{CCO} POR levels in Figure 10. Added V_{IN} to Recommended Operating Conditions in Table 7 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 20%-44% in Table 9. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 10. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}–0.4V for LVCMOS15/18 in Table 11. Added reference to V_{CCAUX} in Simultaneously Switching Output Guidelines. Removed DNA_RETENTION limit of 10 years in Table 14 since number of Read cycles is the only unique limit. Updated speed files to v1.31 in Table 16 and elsewhere. Updated IOB Setup and Hold times with device-specific values in Table 19. Added reference to Sample Window in Table 20. Updated IOB Propagation times with device-specific values in Table 21. Improved SSTL_18_II SSO value in Table 28. Improved F_{BUFG} for -4 to 334 MHz in Table 32. Added references to 375 MHz performance via SCD 4103 in Table 32,Table 37, Table 38, and Table 39. Added explanatory footnotes to DSP48A Timing tables. Simplified DSP48A F_{MAX} to value with all registers used in Table 35. Improved FBUFG in Table 32 for -4 speed grade. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Replaced BPI with SPI specification descriptions in Table 52. Corrected BPI Figure 14 and Table 54 from falling edge to rising edge. Added references to Spartan-3 Generation User Guides. Updated links.
03/11/09	2.2	Changed typical quiescent current temperature from ambient to quiescent. Updated selected I/O standard DC characteristics. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added T_{IOPI} and T_{IOPID} to Table 21. Updated BPI configuration waveforms in Figure 14 and updated Table 55. Removed references to SCD 4103.
10/04/10	3.0	Added I_{IK} to Table 3. Updated description for V_{IN} in Table 7 including adding note 4. Also, added note 2 to I_L in Table 8 to note potential leakage between pins of a differential pair. Added note 6 to Table 10. Updated notes 5 and 6 in Table 12. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 44.

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in UG331: *Spartan-3 Generation FPGA User Guide.*

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs**

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
3	IO_L36P_3	V4	I/O
3	IO_L35N_3	W1	I/O
3	IO_L37N_3	W2	I/O
3	IO_L37P_3	W3	I/O
3	IO_L35P_3	Y1	I/O
3	IP_L39P_3	Y2	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J5	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA7	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B7	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND
GND	GND	D8	GND
GND	GND	D11	GND
GND	GND	D16	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G4	GND
GND	GND	G9	GND
GND	GND	G11	GND
GND	GND	G13	GND
GND	GND	G15	GND
GND	GND	G21	GND
GND	GND	H7	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	H12	GND
GND	GND	H14	GND
GND	GND	H16	GND

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	H19	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J15	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K14	GND
GND	GND	L2	GND
GND	GND	L7	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L19	GND
GND	GND	M4	GND
GND	GND	M8	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	M21	GND
GND	GND	N9	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	N15	GND
GND	GND	P8	GND
GND	GND	P10	GND
GND	GND	P12	GND
GND	GND	P14	GND
GND	GND	R4	GND
GND	GND	R7	GND
GND	GND	R9	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	R16	GND
GND	GND	T2	GND
GND	GND	T8	GND
GND	GND	T10	GND
GND	GND	T12	GND

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IP_2	AF7	INPUT
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O

FG676 Footprint – XC3SD1800A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

82 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

39 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

4 **JTAG:** Dedicated JTAG port pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

77 **GND:** Ground

36 **VCCO:** Output voltage supply for bank.

23 **VCCINT:** Internal core supply voltage (+1.2V).

14 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with triangles inside indicate pin differences from the XC3SD3400A device. Please see the Footprint Migration Differences section for more information.

Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	INPUT ▽	GND	INPUT ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT L04N_3 VREF_3 ▽	INPUT L04P_3 ▽	GND	INPUT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	INPUT L08N_3 ▽	INPUT L08P_3 ▽	I/O L06P_3	TMS	INPUT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	INPUT ▽	I/O L48N_0	VCCO_0	INPUT ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	INPUT ▽	INPUT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT L16N_3 ▽	INPUT L16P_3 ▽	I/O L14P_3	I/O L09N_3	INPUT L12P_3 ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT L12N_3 VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT L54P_3 ▽	INPUT L54N_3 ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	INPUT ▽	I/O L05N_2	I/O L12P_2	INPUT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	INPUT L58P_3 ▽	INPUT L58N_3 VREF_3 ▽	GND	I/O L02N_2 CSO_B	INPUT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	INPUT L62P_3 ▽	INPUT L62N_3 ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	INPUT VREF_2 ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	INPUT ▽	I/O L08P_2	INPUT ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	INPUT ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	INPUT ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	INPUT ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 16: **FG676 Package Footprint for XC3SD1800A FPGA (Top View–Left Half)**

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF