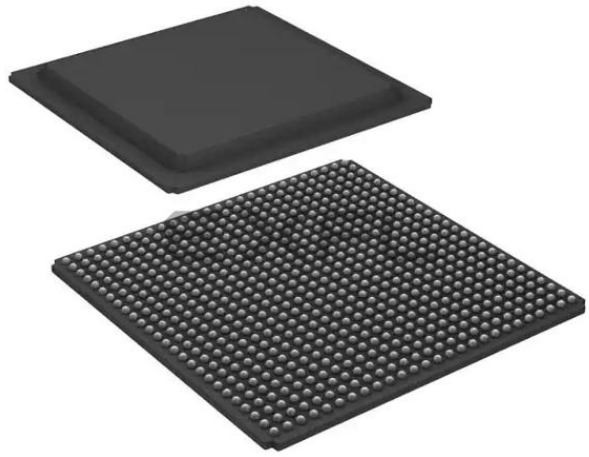

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4fg676c

Configuration

Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A DSP FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications
- Spartan-3A DSP FPGAs support the following differential standards:
- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Device	CS484 CSG484		FG676 FGG676	
	User	**Diff**	**User**	**Diff**
XC3SD1800A	**309**(1) *(60)*	**140** *(78)*	**519** *(110)*	**227** *(131)*
XC3SD3400A	**309** *(60)*	**140** *(78)*	**469** *(60)*	**213** *(117)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Package Marking

Figure 2 shows the top marking for Spartan-3A DSP FPGAs. The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

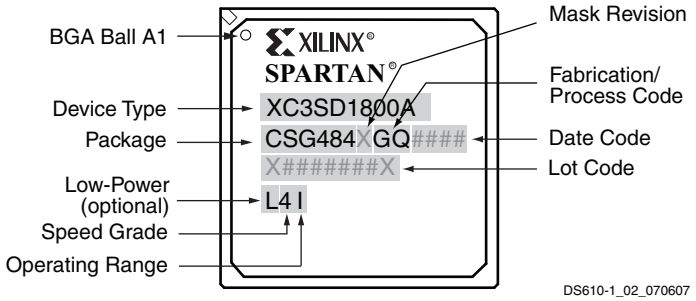
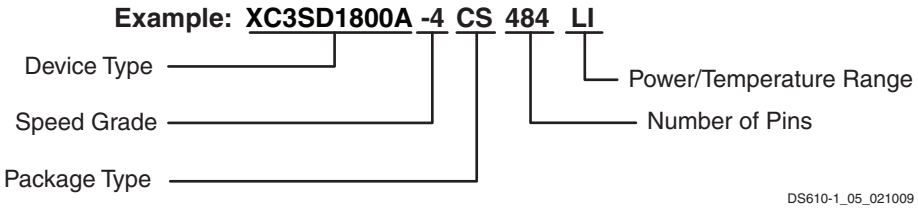


Figure 2: **Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

Spartan-3A DSP FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.



Device	Speed Grade		Package Type / Number of Pins		Power/Temperature Range (T_J)	
XC3SD1800A	-4	Standard Performance	CS484/ CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	C	Commercial (0°C to 85°C)
XC3SD3400A	-5	High Performance(1)	FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	I	Industrial (–40°C to 100°C)
					LI	Low-power Industrial (–40°C to 100°C)(2)

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. The low-power option (LI) is exclusively available in the CS(G)484 package and industrial temperature range.
3. See DS705, *XA Spartan-3A DSP Automotive FPGA Family Data Sheet* for the XA Automotive Spartan-3A DSP FPGAs.

Pin-to-Pin Setup and Hold Times

Table 18: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	2.65	3.11	ns
			XC3SD3400A	2.25	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	2.98	3.39	ns
			XC3SD3400A	2.78	3.08	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	–0.38	–0.38	ns
			XC3SD3400A	–0.26	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	–0.71	–0.71	ns
			XC3SD3400A	–0.65	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Timing Adjustments

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0.00	0.00	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

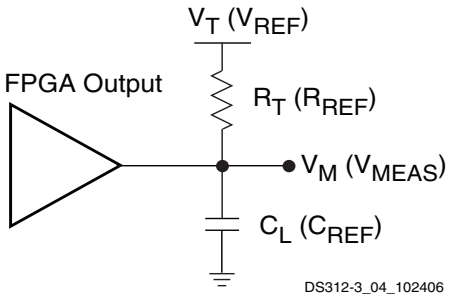
1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 8. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 8: **Output Test Setup**

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs[2]		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Table 35: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Max	Max	
Clock to Out from Output Register Clock to Output Pin							
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.26	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins							
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes	Yes	3.16	3.63	ns
		–	Yes	No	1.94	2.23	ns
Clock to Out from Input Register Clock to Output Pins							
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	6.33	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	7.45	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.37	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	7.33	8.42	ns
Combinatorial Delays from Input Pins to Output Pins							
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	2.78	3.19	ns
		–	Yes	No	4.60	5.28	ns
		–	Yes	Yes	5.65	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	3.49	4.01	ns
		Yes	Yes	No	5.79	6.65	ns
		Yes	Yes	Yes	6.74	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	2.76	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	6.81	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	7.12	8.18	ns
Maximum Frequency							
F_{MAX}	All registers used	Yes	Yes	Yes	287	250	MHz

Notes:

1. To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.
2. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter (2)(3)(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz < FCLKIN < 15 MHz	All	–	5	–	5	ms
		FCLKIN > 15 MHz		–	600	–	600	µs

Table 39: **Switching Characteristics for the DFS**

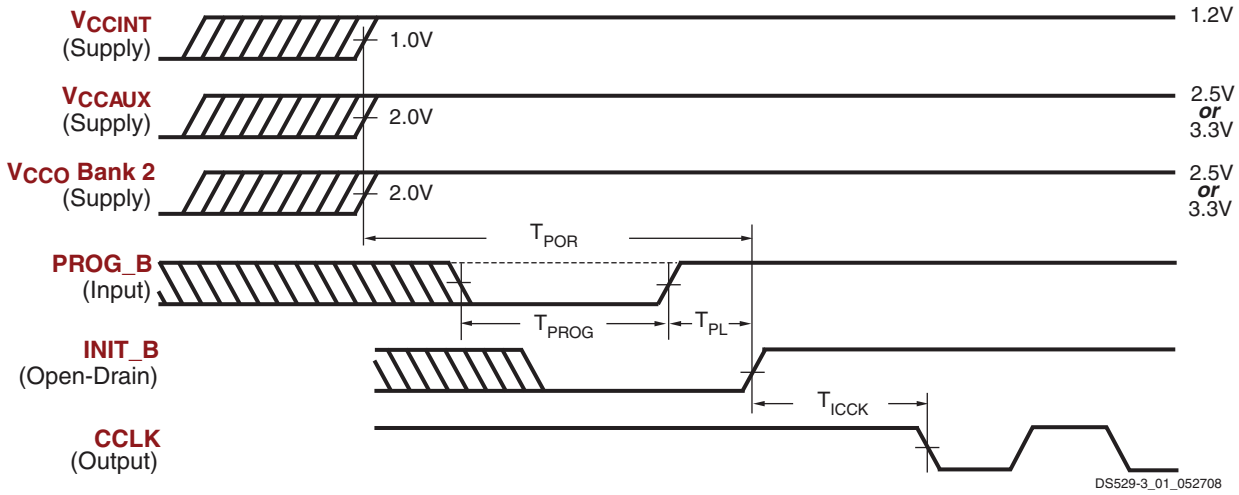
Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX[2]	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	311	MHz
Output Clock Jitter [3][4]								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN ≤ 20 MHz	All	Typ	Max	Typ	Max	
				Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle[5][6]								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment[6]								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps
Lock Time								
LOCK_FX[2][3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	–	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 38.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting[1]	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Master Serial and Slave Serial Mode Timing

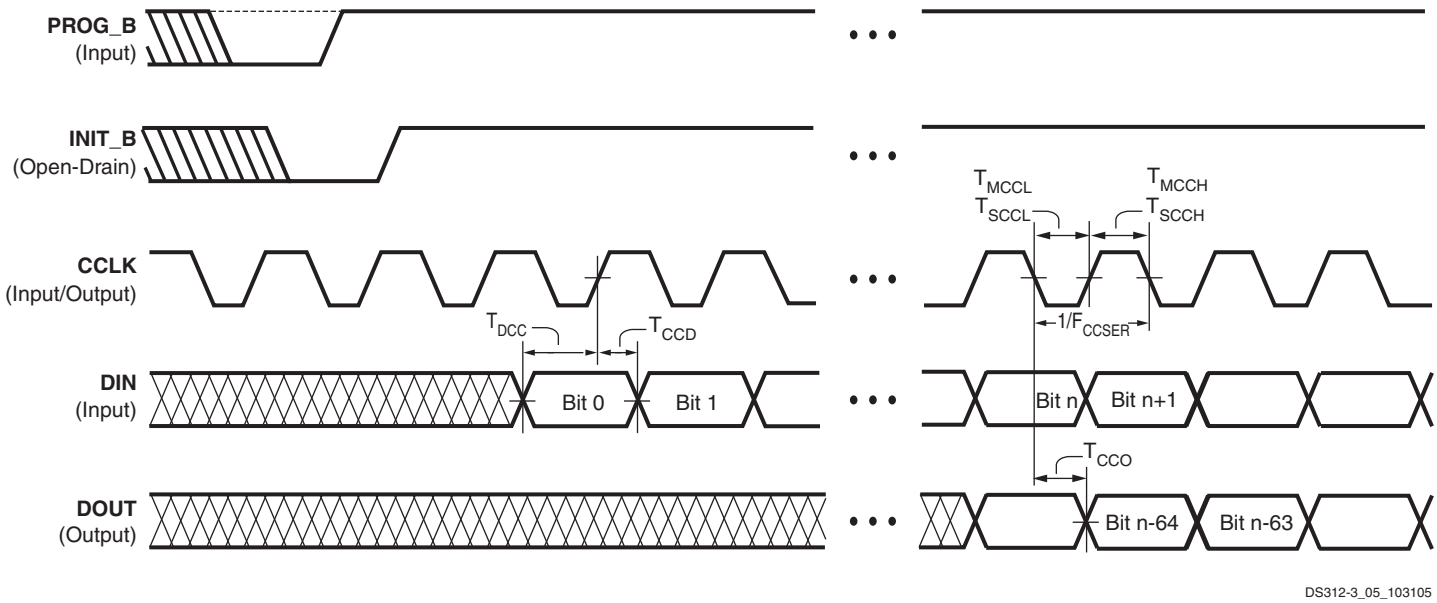


Figure 11: **Waveforms for Master Serial and Slave Serial Configuration**

Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0.0	–	ns
			Slave	1.0	–	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin(2)	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs *(Cont'd)***

Type/Color Code	Description	Pin Name(s) in Type
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected. Set on board and using CONFIG VCCAUX constraint.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 58.

Table 58: **Power and Ground Supply Pins by Package**

Package	Device	VCCINT	VCCAUX	VCCO	GND
CS484	XC3SD1800A	36	24	24	84
	XC3SD3400A	36	24	24	84
FG676	XC3SD1800A	23	14	36	77
	XC3SD3400A	36	24	40	100

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 59. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the *Using I/O Resources* chapter in UG331.

Table 59: **Maximum User I/O by Package**

Package	Device	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF[1]	CLK	N.C.
CS484	XC3SD1800A	309	60	140	156	41	52	28	32	0
	XC3SD3400A	309	60	140	156	41	52	28	32	0
FG676	XC3SD1800A	519	110	227	314	82	52	39	32	0
	XC3SD3400A	469	60	213	314	34	52	37	32	0

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

CS484: 484-Ball Chip-Scale Ball Grid Array

The 484-ball chip-scale ball grid array, CS484, supports both the XC3SD1800A and XC3SD3400A FPGAs. There are no pinout differences between the two devices.

Table 63 lists all the CS484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 63: **Spartan-3A DSP CS484 Pinout**

Bank	Pin Name	CS484 Ball	Type
0	IO_L30N_0	A3	I/O
0	IO_L28N_0	A4	I/O
0	IO_L25N_0	A5	I/O
0	IO_L25P_0	A6	I/O
0	IO_L24N_0/VREF_0	A7	VREF
0	IO_L20P_0/GCLK10	A8	GCLK
0	IO_L18P_0/GCLK6	A9	GCLK
0	IP_0	A10	INPUT
0	IO_L15N_0	A11	I/O
0	IP_0	A12	INPUT
0	IO_L11P_0	A13	I/O
0	IO_L10P_0	A14	I/O
0	IP_0	A15	INPUT
0	IO_L06P_0/VREF_0	A16	VREF
0	IO_L06N_0	A17	I/O
0	IP_0	A18	INPUT
0	IO_L07N_0	A19	I/O
0	IO_0	A20	I/O
0	IO_L30P_0	B3	I/O
0	IO_L28P_0	B4	I/O
0	IO_L24P_0	B6	I/O
0	IO_L20N_0/GCLK11	B8	GCLK
0	IO_L18N_0/GCLK7	B9	GCLK
0	IO_L15P_0	B11	I/O
0	IO_L11N_0	B13	I/O
0	IO_L10N_0	B15	I/O
0	IO_L03P_0	B17	I/O
0	IO_L02N_0	B19	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L07P_0	B20	I/O
0	IO_L29N_0	C4	I/O
0	IP_0	C5	INPUT
0	IO_L21P_0	C6	I/O
0	IO_L26P_0	C7	I/O
0	IO_L22P_0	C8	I/O
0	IO_L16P_0	C9	I/O
0	IP_0	C10	INPUT
0	IP_0/VREF_0	C11	VREF
0	IO_L14N_0	C12	I/O
0	IO_L14P_0	C13	I/O
0	IP_0	C14	INPUT
0	IO_L12N_0/VREF_0	C15	VREF
0	IO_L08N_0	C16	I/O
0	IO_L03N_0	C17	I/O
0	IO_L02P_0/VREF_0	C18	VREF
0	IO_L01N_0	C19	I/O
0	IO_L29P_0	D5	I/O
0	IO_L21N_0	D6	I/O
0	IO_L26N_0	D7	I/O
0	IO_L22N_0	D9	I/O
0	IO_L16N_0	D10	I/O
0	IO_L09N_0	D13	I/O
0	IO_L12P_0	D14	I/O
0	IO_L08P_0	D15	I/O
0	IP_0	D17	INPUT
0	IP_0	D18	INPUT
0	IO_L01P_0	D19	I/O
0	IP_0	E6	INPUT
0	IO_L31P_0/VREF_0	E7	VREF
0	IO_L27N_0	E8	I/O
0	IP_0	E10	INPUT
0	IO_L19N_0/GCLK9	E11	GCLK
0	IO_L17P_0/GCLK4	E12	GCLK
0	IO_L09P_0	E13	I/O
0	IO_L05P_0	E15	I/O
0	IO_L04P_0	E16	I/O
0	IP_0	E17	INPUT
0	IO_L31N_0/PUDC_B	F7	DUAL
0	IO_L27P_0	F8	I/O
0	IO_L23N_0	F9	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IO_L03N_1/A1	V20	DUAL
1	IP_L08P_1	V22	INPUT
1	IO_L03P_1/A0	W19	DUAL
1	IP_L04N_1/VREF_1	W20	VREF
1	IP_L04P_1	W21	INPUT
1	IO_L06P_1	W22	I/O
1	IO_L02P_1/LDC1	Y21	DUAL
1	IO_L06N_1	Y22	I/O
1	VCCO_1	E21	VCCO
1	VCCO_1	J18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P18	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01P_2/M1	AA3	DUAL
2	IO_L04N_2	AA4	I/O
2	IP_2	AA6	INPUT
2	IO_L08N_2	AA8	I/O
2	IO_L12N_2/D6	AA10	DUAL
2	IO_L16P_2/GCLK14	AA12	GCLK
2	IO_L18N_2/GCLK3	AA14	GCLK
2	IO_L19P_2	AA15	I/O
2	IO_L22P_2/AWAKE	AA17	PWRMGMT
2	IO_L27N_2	AA19	I/O
2	IO_L30P_2	AA20	I/O
2	IP_2/VREF_2	AB2	VREF
2	IO_L01N_2/M0	AB3	DUAL
2	IO_L04P_2	AB4	I/O
2	IO_L05P_2	AB5	I/O
2	IO_L05N_2	AB6	I/O
2	IO_L08P_2	AB7	I/O
2	IO_L09P_2/VS1	AB8	DUAL
2	IO_L09N_2/VS0	AB9	DUAL
2	IO_L12P_2/D7	AB10	DUAL
2	IP_2/VREF_2	AB11	VREF
2	IO_L16N_2/GCLK15	AB12	GCLK
2	IO_L18P_2/GCLK2	AB13	GCLK
2	IO_L19N_2	AB14	I/O
2	IP_2	AB15	INPUT
2	IO_L22N_2/DOUT	AB16	DUAL
2	IO_L23P_2	AB17	I/O
2	IO_L23N_2	AB18	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IO_L27P_2	AB19	I/O
2	IO_L30N_2	AB20	I/O
2	IO_L02N_2/CSO_B	U7	DUAL
2	IO_L11N_2	U8	I/O
2	IO_L10N_2	U9	I/O
2	IO_L14N_2/D4	U10	DUAL
2	IO_L17P_2/GCLK0	U12	GCLK
2	IO_L20P_2	U13	I/O
2	IO_L25P_2	U14	I/O
2	IO_L25N_2	U15	I/O
2	IO_L28P_2	U16	I/O
2	IO_L02P_2/M2	V6	DUAL
2	IO_L11P_2	V7	I/O
2	IO_L06N_2	V8	I/O
2	IO_L10P_2	V10	I/O
2	IO_L14P_2/D5	V11	DUAL
2	IO_L17N_2/GCLK1	V12	GCLK
2	IO_L20N_2/MOSI/CSI_B	V13	DUAL
2	IP_2/VREF_2	V15	VREF
2	IO_L28N_2	V16	I/O
2	IO_L31N_2/CCLK	V17	DUAL
2	IP_2/VREF_2	W4	VREF
2	IO_L03P_2	W5	I/O
2	IO_L07N_2/VS2	W6	DUAL
2	IO_L06P_2	W8	I/O
2	IP_2/VREF_2	W9	VREF
2	IP_2	W10	INPUT
2	IP_2/VREF_2	W13	VREF
2	IO_L21N_2	W14	I/O
2	IO_L24P_2/INIT_B	W15	DUAL
2	IO_L31P_2/D0/DIN/MISO	W17	DUAL
2	IP_2/VREF_2	W18	VREF
2	IO_L03N_2	Y4	I/O
2	IO_L07P_2/RDWR_B	Y5	DUAL
2	IP_2	Y6	INPUT
2	IP_2	Y7	INPUT
2	IO_L13P_2	Y8	I/O
2	IO_L13N_2	Y9	I/O
2	IO_L15N_2/GCLK13	Y10	GCLK
2	IO_L15P_2/GCLK12	Y11	GCLK
2	IP_2	Y12	INPUT
2	IO_L21P_2	Y13	I/O

User I/Os by Bank

Table 64 and Table 65 indicates how the user-I/O pins are distributed between the four I/O banks on the CS484 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 64: **User I/Os Per Bank for the XC3SD1800A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Table 65: **User I/Os Per Bank for the XC3SD3400A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/O and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Footprint Migration Differences

There are no migration footprint differences between the XC3SD1800A and the XC3SD3400A in the CS484 package.

CS484 Footprint

Left Half of Package (Top View)

156 **I/O:** Unrestricted, general-purpose user I/O.

41 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

28 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins.

4 **JTAG:** Dedicated JTAG port pins.

84 **GND:** Ground.

24 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	I/O L30N_0	I/O L28N_0	I/O L25N_0	I/O L25P_0	I/O L24N_0 VREF_0	I/O L20P_0 GCLK10	I/O L18P_0 GCLK6	INPUT	I/O L15N_0
B	TMS	VCCAUX	I/O L30P_0	I/O L28P_0	VCCO_0	I/O L24P_0	GND	I/O L20N_0 GCLK11	I/O L18N_0 GCLK7	VCCO_0	I/O L15P_0
C	I/O L02N_3	I/O L02P_3	GND	I/O L29N_0	INPUT	I/O L21P_0	I/O L26P_0	I/O L22P_0	I/O L16P_0	INPUT	INPUT 0 VREF_0
D	INPUT L04P_3	TDI	INPUT L08P_3	INPUT L08N_3	I/O L29P_0	I/O L21N_0	I/O L26N_0	GND	I/O L22N_0	I/O L16N_0	GND
E	INPUT L04N_3 VREF_3	VCCO_3	I/O L09P_3	I/O L09N_3	VCCAUX	INPUT	I/O L31P_0 VREF_0	I/O L27N_0	VCCO_0	INPUT	I/O L19N_0 GCLK9
F	I/O L06N_3	I/O L06P_3	I/O L01P_3	I/O L03P_3	I/O L03N_3	GND	I/O L31N_0 PUDC_B	I/O L27P_0	I/O L23N_0	I/O L19P_0 GCLK8	I/O L17N_0 GCLK5
G	I/O L11P_3	GND	I/O L01N_3	GND	I/O L07P_3	I/O L07N_3	VCCINT	I/O L23P_0	GND	VCCAUX	GND
H	I/O L11N_3	I/O L14P_3	I/O L05P_3	I/O L05N_3	I/O L10P_3	I/O L10N_3	GND	GND	VCCINT	GND	VCCINT
J	I/O L14N_3 VREF_3	VCCO_3	INPUT L16P_3	INPUT L16N_3	VCCO_3	INPUT L12P_3	INPUT L12N_3 VREF_3	VCCINT	GND	VCCINT	GND
K	I/O L19P_3 LHCLK2	I/O L17P_3	I/O L17N_3	I/O L13P_3	I/O L13N_3	I/O L15P_3	VCCAUX	GND	VCCINT	GND	VCCINT
L	I/O L19N_3 IRDY2 LHCLK3	GND	I/O L20P_3 LHCLK4	VCCAUX	I/O L15N_3	I/O L18P_3 LHCLK0	GND	VCCINT	GND	VCCINT	GND
M	I/O L22P_3 VREF_3	I/O L20N_3 LHCLK5	INPUT L23P_3	GND	I/O L18N_3 LHCLK1	I/O L21P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	GND	VCCINT
N	I/O L22N_3	VCCO_3	INPUT L31P_3	INPUT L23N_3	I/O L24N_3	I/O L24P_3	I/O L21N_3 LHCLK7	VCCINT	GND	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT L31N_3	I/O L32P_3 VREF_3	VCCO_3	I/O L26P_3	VCCAUX	GND	VCCINT	GND	VCCINT
R	I/O L28N_3	I/O L28P_3	I/O L34P_3	GND	I/O L32N_3	I/O L26N_3	GND	VCCINT	GND	VCCINT	GND
T	I/O L30P_3	GND	INPUT L27P_3	I/O L34N_3	I/O L29N_3	I/O L29P_3	VCCINT	GND	VCCAUX	GND	VCCAUX
U	I/O L30N_3	I/O L33P_3	INPUT L27N_3	I/O L38P_3	I/O L38N_3	GND	I/O L02N_2 CSO_B	I/O L11N_2	I/O L10N_2	I/O L14N_2 D4	GND
V	I/O L33N_3	VCCO_3	I/O L36N_3	I/O L36P_3	VCCAUX	I/O L02P_2 M2	I/O L11P_2	I/O L06N_2	VCCO_2	I/O L10P_2	I/O L14P_2 D5
W	I/O L35N_3	I/O L37N_3	I/O L37P_3	INPUT 2 VREF_2	I/O L03P_2	I/O L07N_2 VS2	GND	I/O L06P_2	INPUT 2 VREF_2	INPUT	VCCAUX
Y	I/O L35P_3	INPUT L39P_3	GND	I/O L03N_2	I/O L07P_2 RDWR_B	INPUT	INPUT	I/O L13P_2	I/O L13N_2	I/O L15N_2 GCLK13	I/O L15P_2 GCLK12
AA	INPUT L39N_3 VREF_3	VCCAUX	I/O L01P_2 M1	I/O L04N_2	VCCO_2	INPUT	GND	I/O L08N_2	VCCO_2	I/O L12N_2 D6	GND
AB	GND	INPUT 2 VREF_2	I/O L01N_2 M0	I/O L04P_2	I/O L05P_2	I/O L05N_2	I/O L08P_2	I/O L09P_2 VS1	I/O L09N_2 VS0	I/O L12P_2 D7	INPUT 2 VREF_2

Bank 3 (left) **Bank 2** (bottom)

Figure 15: **CS484 Package Footprint (Top View–Left Half)**

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_L48N_1	H24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O
1	IP_L52N_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_L65P_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	IP_L16P_1	W25	INPUT
1	IP_L24P_1	U25	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L20P_1	W26	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52P_1	G26	INPUT
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IP_L04P_3	C2	INPUT
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L16P_3	G2	INPUT
3	IP_L12P_3	G5	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L58P_3	AA4	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L54N_3	Y4	INPUT
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_1	H24	INPUT
1	IP_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O

FG676 Footprint – XC3SD3400A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

34 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

37 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

4 **JTAG:** Dedicated JTAG port pins.

100 **GND:** Ground

40 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with question marks inside indicate pin differences from the XC3SD1800A device. Please see the Footprint Migration Differences section for more information.

	Bank 0												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	GND ▽	GND	VCCO_0 ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT VREF_3 ▽	VCCO_3 ▽	GND	VCCINT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	VCCAUX ▽	GND ▽	I/O L06P_3	TMS	VCCINT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VCCINT ▽	I/O L48N_0	VCCO_0	GND ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	VCCAUX ▽	VCCINT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT ▽	GND ▽	I/O L14P_3	I/O L09N_3	GND ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT ▽	VCCINT ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	VCCINT ▽	I/O L05N_2	I/O L12P_2	VCCINT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	GND ▽	INPUT VREF_3 ▽	GND	I/O L02N_2 CSO_B	VCCINT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	GND ▽	VCCAUX ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	GND ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	GND ▽	I/O L08P_2	GND ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	GND ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	VCCAUX ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	VCCO_2 ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Left Half)**