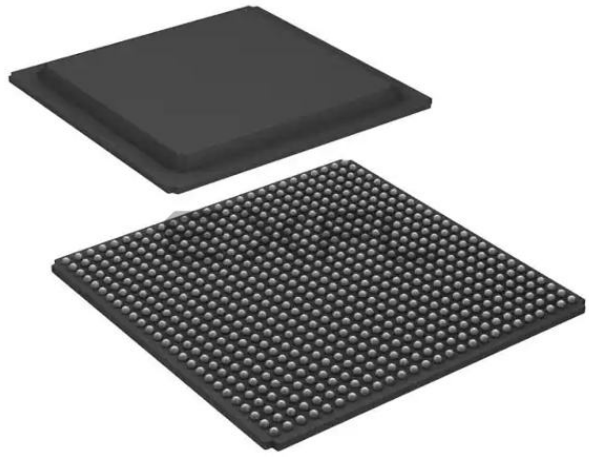
AMD Xilinx - XC3SD3400A-4FG676I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4fg676i

General DC Characteristics for I/O Pins

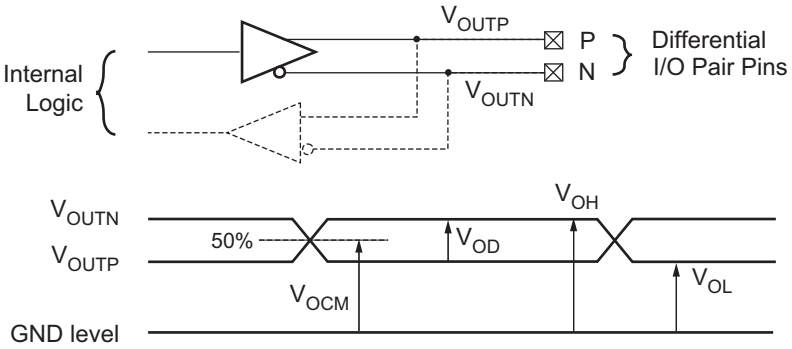
Table 8: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins** (1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU} (3)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD} (3)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO}/I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.

Differential Output Pairs



V_{OCM} = Output common mode voltage = $\frac{V_{OUTP} + V_{OUTN}}{2}$

V_{OD} = Output differential voltage = $|V_{OUTP} - V_{OUTN}|$

V_{OH} = Output voltage indicating a High logic level

V_{OL} = Output voltage indicating a Low logic level

DS312-3_03_090510

Figure 4: **Differential Output Voltages**

Table 13: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.603	V_{TT} – 0.603
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} - 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} - 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 12.
2. See "External Termination Requirements for Differential I/O."
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

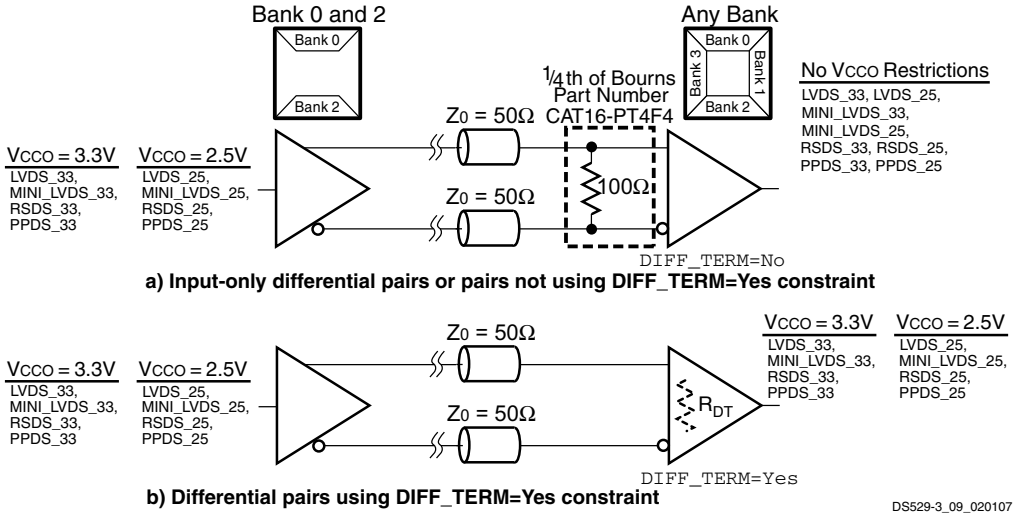


Figure 5: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

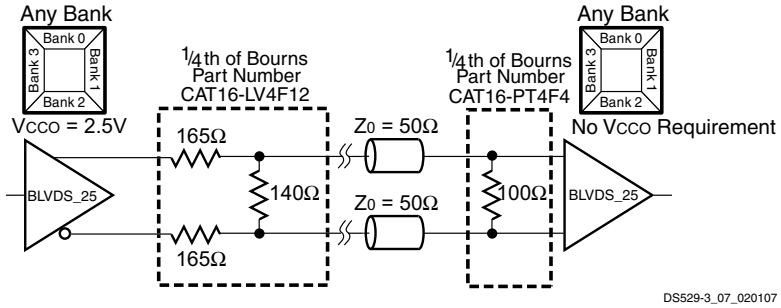


Figure 6: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

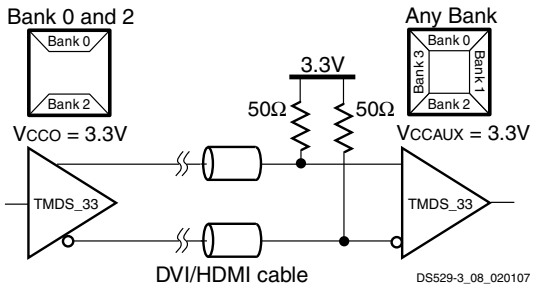


Figure 7: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 14: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Input Setup and Hold Times

Table 19: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	DELAY_ VALUE	Device	Speed		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	IFD_DELAY_VALUE=0	XC3SD1800A	1.65	1.81	ns
				XC3SD3400A	1.51	1.88	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XC3SD1800A	2.09	2.24	ns
			2		2.67	2.83	ns
			3		3.25	3.64	ns
			4		3.75	4.20	ns
			5		3.69	4.16	ns
			6		4.47	5.09	ns
			7		5.27	6.02	ns
			8		5.79	6.63	ns
			1	XC3SD3400A	2.07	2.44	ns
			2		2.57	3.02	ns
			3		3.44	3.81	ns
			4		4.01	4.39	ns
			5		3.89	4.26	ns
			6		4.43	5.08	ns
			7		5.20	5.95	ns
			8		5.70	6.55	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XC3SD1800A	–0.63	–0.52	ns
				XC3SD3400A	–0.56	–0.56	ns

Table 21: **Propagation Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XC3SD1800A	1.79	2.04	ns
				XC3SD3400A	1.65	2.11	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XC3SD1800A	2.23	2.47	ns
			2		2.81	3.06	ns
			3		3.39	3.86	ns
			4		3.89	4.43	ns
			5		3.83	4.39	ns
			6		4.61	5.32	ns
			7		5.40	6.24	ns
			8		5.93	6.86	ns
			1	XC3SD3400A	2.21	2.67	ns
			2		2.71	3.25	ns
			3		3.58	4.04	ns
			4		4.15	4.62	ns
			5		4.03	4.49	ns
			6		4.57	5.31	ns
			7		5.34	6.18	ns
			8		5.84	6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	–	11
		24	–	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	–	3
		24	–	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	–	36
		24	–	8

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	–	13
		16	–	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	–	4
		16	–	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	–	36
		16	–	24
LVCMOS15	Slow	2	55	55
		4	31	31
		6	18	18
		8	–	15
		12	–	10
	Fast	2	25	25
		4	10	10
		6	6	6
		8	–	4
		12	–	3
	QuietIO	2	70	70
		4	40	40
		6	31	31
		8	–	31
		12	–	20

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS12	Slow	2	40	40
		4	–	25
		6	–	18
	Fast	2	31	31
		4	–	13
		6	–	9
	QuietIO	2	55	55
		4	–	36
		6	–	36
PCI33_3			16	16
PCI66_3			–	13
HSTL_I			–	20
HSTL_III			–	8
HSTL_I_18			17	17
HSTL_II_18			–	5
HSTL_III_18			10	8
SSTL18_I			7	15
SSTL18_II			–	9
SSTL2_I			18	18
SSTL2_II			–	9
SSTL3_I			8	10
SSTL3_II			6	7

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)	Package Type	
	CS484, FG676	
	Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Differential Standards (Number of I/O Pairs or Channels)		
LVDS_25	22	–
LVDS_33	27	–
BLVDS_25	4	4
MINI_LVDS_25	22	–
MINI_LVDS_33	27	–
LVPECL_25	Inputs Only	
LVPECL_33	Inputs Only	
RSDS_25	22	–
RSDS_33	27	–
TMDS_33	27	–
PPDS_25	22	–
PPDS_33	27	–
DIFF_HSTL_I_18	8	8
DIFF_HSTL_II_18	–	2
DIFF_HSTL_III_18	5	4
DIFF_HSTL_I	–	10
DIFF_HSTL_III	–	4
DIFF_SSTL18_I	3	7
DIFF_SSTL18_II	–	4
DIFF_SSTL2_I	9	9
DIFF_SSTL2_II	–	4
DIFF_SSTL3_I	4	5
DIFF_SSTL3_II	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Clock Buffer/Multiplexer Switching Characteristics

Table 32: **Clock Distribution Switching Characteristics**

Symbol	Description	Minimum	Maximum		Units
			Speed Grade		
			-5	-4	
T_{GIO}	Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	–	0.22	0.23	ns
T_{GSI}	Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	–	0.56	0.63	ns
F_{BUFG}	Frequency of signals distributed on global buffers (all sides)	0	350	334	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Block RAM Timing

Table 33: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
$T_{RCKO\_DOA\_NC}$	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.38	–	2.80	ns
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)	–	1.24	–	1.45	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.40	–	0.46	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.29	–	0.33	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.51	–	0.60	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	0.64	–	0.75	–	ns
T_{RCCK_REGCE}	Setup time for the CE input before the active transition at the CLK input of the block RAM	0.34	–	0.40	–	ns
T_{RCCK_RST}	Setup time for the RST input before the active transition at the CLK input of the block RAM	0.22	–	0.25	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_REGCE}	Hold time on the CE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_RST}	Hold time on the RST input after the active transition at the CLK input	0.09	–	0.10	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter (2)(3)(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz < FCLKIN < 15 MHz	All	–	5	–	5	ms
		FCLKIN > 15 MHz		–	600	–	600	µs

Table 37: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.2	333(5)	0.2	333(5)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.
5. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for v1.29 production speed files. Noted banking rules in Table 11 and Table 12. Added DIFF_HSTL_I and DIFF_HSTL_III to Table 12, Table 13, and Table 26. Updated TMDS DC characteristics in Table 13. Updated I/O Test Method values in Table 26. Added Simultaneously Switching Output limits in Table 28. Updated DSP48A timing symbols, descriptions, and values in Table 34. Added power-on timing in Table 45. Added CCLK specifications for Commercial in Table 46 through Table 48. Updated Slave Parallel timing in Table 51. Updated JTAG specifications in Table 56.
07/16/07	2.0	Added Low-power options and updated typical values for quiescent current in Table 9. Updated DSP48A timing in Table 34 and Table 35.
06/02/08	2.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 4 and updated V_{CCO} POR levels in Figure 10. Added V_{IN} to Recommended Operating Conditions in Table 7 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 20%-44% in Table 9. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 10. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}–0.4V for LVCMOS15/18 in Table 11. Added reference to V_{CCAUX} in Simultaneously Switching Output Guidelines. Removed DNA_RETENTION limit of 10 years in Table 14 since number of Read cycles is the only unique limit. Updated speed files to v1.31 in Table 16 and elsewhere. Updated IOB Setup and Hold times with device-specific values in Table 19. Added reference to Sample Window in Table 20. Updated IOB Propagation times with device-specific values in Table 21. Improved SSTL_18_II SSO value in Table 28. Improved F_{BUFG} for -4 to 334 MHz in Table 32. Added references to 375 MHz performance via SCD 4103 in Table 32,Table 37, Table 38, and Table 39. Added explanatory footnotes to DSP48A Timing tables. Simplified DSP48A F_{MAX} to value with all registers used in Table 35. Improved FBUFG in Table 32 for -4 speed grade. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Replaced BPI with SPI specification descriptions in Table 52. Corrected BPI Figure 14 and Table 54 from falling edge to rising edge. Added references to Spartan-3 Generation User Guides. Updated links.
03/11/09	2.2	Changed typical quiescent current temperature from ambient to quiescent. Updated selected I/O standard DC characteristics. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added T_{IOPI} and T_{IOPID} to Table 21. Updated BPI configuration waveforms in Figure 14 and updated Table 55. Removed references to SCD 4103.
10/04/10	3.0	Added I_{IK} to Table 3. Updated description for V_{IN} in Table 7 including adding note 4. Also, added note 2 to I_L in Table 8 to note potential leakage between pins of a differential pair. Added note 6 to Table 10. Updated notes 5 and 6 in Table 12. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 44.

CS484: 484-Ball Chip-Scale Ball Grid Array

The 484-ball chip-scale ball grid array, CS484, supports both the XC3SD1800A and XC3SD3400A FPGAs. There are no pinout differences between the two devices.

Table 63 lists all the CS484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 63: **Spartan-3A DSP CS484 Pinout**

Bank	Pin Name	CS484 Ball	Type
0	IO_L30N_0	A3	I/O
0	IO_L28N_0	A4	I/O
0	IO_L25N_0	A5	I/O
0	IO_L25P_0	A6	I/O
0	IO_L24N_0/VREF_0	A7	VREF
0	IO_L20P_0/GCLK10	A8	GCLK
0	IO_L18P_0/GCLK6	A9	GCLK
0	IP_0	A10	INPUT
0	IO_L15N_0	A11	I/O
0	IP_0	A12	INPUT
0	IO_L11P_0	A13	I/O
0	IO_L10P_0	A14	I/O
0	IP_0	A15	INPUT
0	IO_L06P_0/VREF_0	A16	VREF
0	IO_L06N_0	A17	I/O
0	IP_0	A18	INPUT
0	IO_L07N_0	A19	I/O
0	IO_0	A20	I/O
0	IO_L30P_0	B3	I/O
0	IO_L28P_0	B4	I/O
0	IO_L24P_0	B6	I/O
0	IO_L20N_0/GCLK11	B8	GCLK
0	IO_L18N_0/GCLK7	B9	GCLK
0	IO_L15P_0	B11	I/O
0	IO_L11N_0	B13	I/O
0	IO_L10N_0	B15	I/O
0	IO_L03P_0	B17	I/O
0	IO_L02N_0	B19	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L07P_0	B20	I/O
0	IO_L29N_0	C4	I/O
0	IP_0	C5	INPUT
0	IO_L21P_0	C6	I/O
0	IO_L26P_0	C7	I/O
0	IO_L22P_0	C8	I/O
0	IO_L16P_0	C9	I/O
0	IP_0	C10	INPUT
0	IP_0/VREF_0	C11	VREF
0	IO_L14N_0	C12	I/O
0	IO_L14P_0	C13	I/O
0	IP_0	C14	INPUT
0	IO_L12N_0/VREF_0	C15	VREF
0	IO_L08N_0	C16	I/O
0	IO_L03N_0	C17	I/O
0	IO_L02P_0/VREF_0	C18	VREF
0	IO_L01N_0	C19	I/O
0	IO_L29P_0	D5	I/O
0	IO_L21N_0	D6	I/O
0	IO_L26N_0	D7	I/O
0	IO_L22N_0	D9	I/O
0	IO_L16N_0	D10	I/O
0	IO_L09N_0	D13	I/O
0	IO_L12P_0	D14	I/O
0	IO_L08P_0	D15	I/O
0	IP_0	D17	INPUT
0	IP_0	D18	INPUT
0	IO_L01P_0	D19	I/O
0	IP_0	E6	INPUT
0	IO_L31P_0/VREF_0	E7	VREF
0	IO_L27N_0	E8	I/O
0	IP_0	E10	INPUT
0	IO_L19N_0/GCLK9	E11	GCLK
0	IO_L17P_0/GCLK4	E12	GCLK
0	IO_L09P_0	E13	I/O
0	IO_L05P_0	E15	I/O
0	IO_L04P_0	E16	I/O
0	IP_0	E17	INPUT
0	IO_L31N_0/PUDC_B	F7	DUAL
0	IO_L27P_0	F8	I/O
0	IO_L23N_0	F9	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IO_L03N_1/A1	V20	DUAL
1	IP_L08P_1	V22	INPUT
1	IO_L03P_1/A0	W19	DUAL
1	IP_L04N_1/VREF_1	W20	VREF
1	IP_L04P_1	W21	INPUT
1	IO_L06P_1	W22	I/O
1	IO_L02P_1/LDC1	Y21	DUAL
1	IO_L06N_1	Y22	I/O
1	VCCO_1	E21	VCCO
1	VCCO_1	J18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P18	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01P_2/M1	AA3	DUAL
2	IO_L04N_2	AA4	I/O
2	IP_2	AA6	INPUT
2	IO_L08N_2	AA8	I/O
2	IO_L12N_2/D6	AA10	DUAL
2	IO_L16P_2/GCLK14	AA12	GCLK
2	IO_L18N_2/GCLK3	AA14	GCLK
2	IO_L19P_2	AA15	I/O
2	IO_L22P_2/AWAKE	AA17	PWRMGMT
2	IO_L27N_2	AA19	I/O
2	IO_L30P_2	AA20	I/O
2	IP_2/VREF_2	AB2	VREF
2	IO_L01N_2/M0	AB3	DUAL
2	IO_L04P_2	AB4	I/O
2	IO_L05P_2	AB5	I/O
2	IO_L05N_2	AB6	I/O
2	IO_L08P_2	AB7	I/O
2	IO_L09P_2/VS1	AB8	DUAL
2	IO_L09N_2/VS0	AB9	DUAL
2	IO_L12P_2/D7	AB10	DUAL
2	IP_2/VREF_2	AB11	VREF
2	IO_L16N_2/GCLK15	AB12	GCLK
2	IO_L18P_2/GCLK2	AB13	GCLK
2	IO_L19N_2	AB14	I/O
2	IP_2	AB15	INPUT
2	IO_L22N_2/DOUT	AB16	DUAL
2	IO_L23P_2	AB17	I/O
2	IO_L23N_2	AB18	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IO_L27P_2	AB19	I/O
2	IO_L30N_2	AB20	I/O
2	IO_L02N_2/CSO_B	U7	DUAL
2	IO_L11N_2	U8	I/O
2	IO_L10N_2	U9	I/O
2	IO_L14N_2/D4	U10	DUAL
2	IO_L17P_2/GCLK0	U12	GCLK
2	IO_L20P_2	U13	I/O
2	IO_L25P_2	U14	I/O
2	IO_L25N_2	U15	I/O
2	IO_L28P_2	U16	I/O
2	IO_L02P_2/M2	V6	DUAL
2	IO_L11P_2	V7	I/O
2	IO_L06N_2	V8	I/O
2	IO_L10P_2	V10	I/O
2	IO_L14P_2/D5	V11	DUAL
2	IO_L17N_2/GCLK1	V12	GCLK
2	IO_L20N_2/MOSI/CSI_B	V13	DUAL
2	IP_2/VREF_2	V15	VREF
2	IO_L28N_2	V16	I/O
2	IO_L31N_2/CCLK	V17	DUAL
2	IP_2/VREF_2	W4	VREF
2	IO_L03P_2	W5	I/O
2	IO_L07N_2/VS2	W6	DUAL
2	IO_L06P_2	W8	I/O
2	IP_2/VREF_2	W9	VREF
2	IP_2	W10	INPUT
2	IP_2/VREF_2	W13	VREF
2	IO_L21N_2	W14	I/O
2	IO_L24P_2/INIT_B	W15	DUAL
2	IO_L31P_2/D0/DIN/MISO	W17	DUAL
2	IP_2/VREF_2	W18	VREF
2	IO_L03N_2	Y4	I/O
2	IO_L07P_2/RDWR_B	Y5	DUAL
2	IP_2	Y6	INPUT
2	IP_2	Y7	INPUT
2	IO_L13P_2	Y8	I/O
2	IO_L13N_2	Y9	I/O
2	IO_L15N_2/GCLK13	Y10	GCLK
2	IO_L15P_2/GCLK12	Y11	GCLK
2	IP_2	Y12	INPUT
2	IO_L21P_2	Y13	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IP_2/VREF_2	Y14	VREF
2	IO_L24N_2/D3	Y15	DUAL
2	IO_L29N_2	Y16	I/O
2	IO_L29P_2	Y17	I/O
2	IO_L26P_2/D2	Y18	DUAL
2	IO_L26N_2/D1	Y19	DUAL
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
2	VCCO_2	V9	VCCO
2	VCCO_2	V14	VCCO
3	IP_L39N_3/VREF_3	AA1	VREF
3	IO_L02N_3	C1	I/O
3	IO_L02P_3	C2	I/O
3	IP_L04P_3	D1	INPUT
3	IP_L08P_3	D3	INPUT
3	IP_L08N_3	D4	INPUT
3	IP_L04N_3/VREF_3	E1	VREF
3	IO_L09P_3	E3	I/O
3	IO_L09N_3	E4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L01P_3	F3	I/O
3	IO_L03P_3	F4	I/O
3	IO_L03N_3	F5	I/O
3	IO_L11P_3	G1	I/O
3	IO_L01N_3	G3	I/O
3	IO_L07P_3	G5	I/O
3	IO_L07N_3	G6	I/O
3	IO_L11N_3	H1	I/O
3	IO_L14P_3	H2	I/O
3	IO_L05P_3	H3	I/O
3	IO_L05N_3	H4	I/O
3	IO_L10P_3	H5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L14N_3/VREF_3	J1	VREF
3	IP_L16P_3	J3	INPUT
3	IP_L16N_3	J4	INPUT
3	IP_L12P_3	J6	INPUT
3	IP_L12N_3/VREF_3	J7	VREF
3	IO_L19P_3/LHCLK2	K1	LHCLK

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
3	IO_L17P_3	K2	I/O
3	IO_L17N_3	K3	I/O
3	IO_L13P_3	K4	I/O
3	IO_L13N_3	K5	I/O
3	IO_L15P_3	K6	I/O
3	IO_L19N_3/IRDY2/LHCLK3	L1	LHCLK
3	IO_L20P_3/LHCLK4	L3	LHCLK
3	IO_L15N_3	L5	I/O
3	IO_L18P_3/LHCLK0	L6	LHCLK
3	IO_L22P_3/VREF_3	M1	VREF
3	IO_L20N_3/LHCLK5	M2	LHCLK
3	IP_L23P_3	M3	INPUT
3	IO_L18N_3/LHCLK1	M5	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	M6	LHCLK
3	IO_L22N_3	N1	I/O
3	IP_L31P_3	N3	INPUT
3	IP_L23N_3	N4	INPUT
3	IO_L24N_3	N5	I/O
3	IO_L24P_3	N6	I/O
3	IO_L21N_3/LHCLK7	N7	LHCLK
3	IO_L25P_3	P1	I/O
3	IO_L25N_3	P2	I/O
3	IP_L31N_3	P3	INPUT
3	IO_L32P_3/VREF_3	P4	VREF
3	IO_L26P_3	P6	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	R2	I/O
3	IO_L34P_3	R3	I/O
3	IO_L32N_3	R5	I/O
3	IO_L26N_3	R6	I/O
3	IO_L30P_3	T1	I/O
3	IP_L27P_3	T3	INPUT
3	IO_L34N_3	T4	I/O
3	IO_L29N_3	T5	I/O
3	IO_L29P_3	T6	I/O
3	IO_L30N_3	U1	I/O
3	IO_L33P_3	U2	I/O
3	IP_L27N_3	U3	INPUT
3	IO_L38P_3	U4	I/O
3	IO_L38N_3	U5	I/O
3	IO_L33N_3	V1	I/O
3	IO_L36N_3	V3	I/O

FG676: 676-Ball Fine-Pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports both the XC3SD1800A and the XC3SD3400A FPGAs. There are multiple pinout differences between the two devices. For a list of differences and migration advice, see the Footprint Migration Differences section.

XC3SD1800A FPGA

Table 66 lists all the FG676 package pins for the XC3SD1800A FPGA. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Pinout Table

Note: The grayed boxes denote a difference between the XC3SD1800A and the XC3SD3400A devices.

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA**

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L43N_0	K11	I/O
0	IO_L39N_0	K12	I/O
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L12N_0	K16	I/O
0	IP_0	J10	INPUT
0	IO_L43P_0	J11	I/O
0	IO_L39P_0	J12	I/O
0	IP_0	J13	INPUT
0	IO_L25N_0/GCLK5	J14	GCLK
0	IP_0	J15	INPUT
0	IO_L12P_0	J16	I/O
0	IP_0/VREF_0	J17	VREF
0	IO_L47N_0	H9	I/O
0	IO_L46N_0	H10	I/O
0	IO_L35N_0	H12	I/O
0	IP_0	H13	INPUT
0	IO_L16N_0	H15	I/O
0	IO_L08P_0	H17	I/O
0	IP_0	H18	INPUT
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L47P_0	G9	I/O
0	IO_L46P_0	G10	I/O
0	IP_0/VREF_0	G11	VREF
0	IO_L35P_0	G12	I/O
0	IO_L27N_0/GCLK9	G13	GCLK
0	IP_0	G14	INPUT
0	IO_L16P_0	G15	I/O
0	IO_L08N_0	G17	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L01P_0	G20	I/O
0	IO_L48P_0	F7	I/O
0	IO_L52P_0/VREF_0	F8	VREF
0	IO_L31N_0	F12	I/O
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L24N_0	F14	I/O
0	IO_L20P_0	F15	I/O
0	IO_L13P_0	F17	I/O
0	IO_L02N_0	F19	I/O
0	IO_L01N_0	F20	I/O
0	IO_L48N_0	E7	I/O
0	IO_L37P_0	E10	I/O
0	IP_0	E11	INPUT
0	IO_L31P_0	E12	I/O
0	IO_L24P_0	E14	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L13N_0	E17	I/O
0	IP_0	E18	INPUT
0	IO_L10P_0	E21	I/O
0	IO_L44N_0	D6	I/O
0	IP_0/VREF_0	D7	VREF
0	IO_L40N_0	D8	I/O
0	IO_L37N_0	D9	I/O
0	IO_L34N_0	D10	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IP_0	D12	INPUT
0	IO_L30P_0	D13	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_L16N_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_L20N_1/VREF_1	V26	VREF
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_L24N_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O

FG676 Footprint – XC3SD1800A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

82 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

39 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

4 **JTAG:** Dedicated JTAG port pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

77 **GND:** Ground

36 **VCCO:** Output voltage supply for bank.

23 **VCCINT:** Internal core supply voltage (+1.2V).

14 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with triangles inside indicate pin differences from the XC3SD3400A device. Please see the Footprint Migration Differences section for more information.

Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	INPUT ▽	GND	INPUT ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT L04N_3 VREF_3 ▽	INPUT L04P_3 ▽	GND	INPUT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	INPUT L08N_3 ▽	INPUT L08P_3 ▽	I/O L06P_3	TMS	INPUT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	INPUT ▽	I/O L48N_0	VCCO_0	INPUT ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	INPUT ▽	INPUT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT L16N_3 ▽	INPUT L16P_3 ▽	I/O L14P_3	I/O L09N_3	INPUT L12P_3 ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT L12N_3 VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT L54P_3 ▽	INPUT L54N_3 ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	INPUT ▽	I/O L05N_2	I/O L12P_2	INPUT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	INPUT L58P_3 ▽	INPUT L58N_3 VREF_3 ▽	GND	I/O L02N_2 CSO_B	INPUT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	INPUT L62P_3 ▽	INPUT L62N_3 ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	INPUT VREF_2 ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	INPUT ▽	I/O L08P_2	INPUT ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	INPUT ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	INPUT ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	INPUT ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 16: **FG676 Package Footprint for XC3SD1800A FPGA (Top View–Left Half)**

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	A23	GND
GND	GND	A26	GND
VCCAUX	SUSPEND	V20	PWRMGMT
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	TCK	A25	JTAG
VCCAUX	VCCAUX	W26	VCCAUX
VCCAUX	VCCAUX	V9	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	H23	VCCAUX
VCCAUX	VCCAUX	G26	VCCAUX
VCCAUX	VCCAUX	F9	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E20	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	D1	VCCAUX
VCCAUX	VCCAUX	AF2	VCCAUX
VCCAUX	VCCAUX	AB4	VCCAUX
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX
VCCAUX	VCCAUX	AB17	VCCAUX
VCCAUX	VCCAUX	AB22	VCCAUX
VCCAUX	VCCAUX	A24	VCCAUX
VCCINT	VCCINT	Y4	VCCINT
VCCINT	VCCINT	Y8	VCCINT
VCCINT	VCCINT	Y11	VCCINT
VCCINT	VCCINT	Y18	VCCINT
VCCINT	VCCINT	Y19	VCCINT
VCCINT	VCCINT	W18	VCCINT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
VCCINT	VCCINT	U12	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	G18	VCCINT
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	F18	VCCINT
VCCINT	VCCINT	E6	VCCINT
VCCINT	VCCINT	D5	VCCINT
VCCINT	VCCINT	C4	VCCINT
VCCINT	VCCINT	AA8	VCCINT