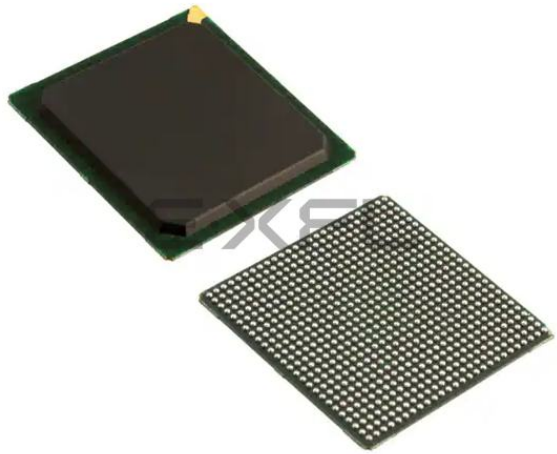

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4fgg676c

XC3SD3400A FPGA

[illegible]

[illegible]

Pinout Table

Note: [illegible]

Table 68: Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	[illegible]	K1	IO
0	[illegible]	K2	IO
0	[illegible]	K4	IO
0	[illegible]	K6	IO
0	[illegible]	J10	VCCO
0	[illegible]	J11	IO
0	[illegible]	J12	IO
0	[illegible]	J13	VCCO
0	[illegible]	J14	IO
0	[illegible]	J15	VCCO
0	[illegible]	J16	IO
0	[illegible]	J17	VREF
0	[illegible]	H1	IO
0	[illegible]	H10	IO
0	[illegible]	H12	IO
0	[illegible]	H13	VCCO
0	[illegible]	H15	IO
0	[illegible]	H17	IO
0	[illegible]	H18	VCCO
0	[illegible]	G1	IO
0	[illegible]	G10	IO
0	[illegible]	G11	VREF
0	[illegible]	G12	IO
0	[illegible]	G13	IO
0	[illegible]	G14	VCCO
0	[illegible]	G15	IO
0	[illegible]	G16	IO
0	[illegible]	G17	IO
0	[illegible]	G18	VCCO
0	[illegible]	F1	IO
0	[illegible]	F2	VREF
0	[illegible]	F3	IO
0	[illegible]	F4	IO
0	[illegible]	F5	IO
0	[illegible]	F7	IO
0	[illegible]	F9	IO
0	[illegible]	F10	IO
0	[illegible]	F11	VCCO
0	[illegible]	F12	IO
0	[illegible]	F13	VCCO
0	[illegible]	E1	IO
0	[illegible]	E2	IO
0	[illegible]	E4	IO
0	[illegible]	E5	VREF
0	[illegible]	E7	IO
0	[illegible]	E8	VCCO
0	[illegible]	E10	IO
0	[illegible]	D1	IO
0	[illegible]	D2	VCCO
0	[illegible]	D3	IO
0	[illegible]	D4	VREF
0	[illegible]	D6	IO
0	[illegible]	D7	IO
0	[illegible]	D8	IO
0	[illegible]	D10	IO

Table 68: Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA (Cont'd)

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	[illegible]	F1	IO
0	[illegible]	B1	VREF
0	[illegible]	E2	IO
0	[illegible]	E3	VREF
0	[illegible]	E4	IO
0	[illegible]	E5	IO
0	[illegible]	E7	IO
0	[illegible]	E9	IO
0	[illegible]	C1	IO
0	[illegible]	E1	IO
0	[illegible]	E2	IO
0	[illegible]	E3	VCCO
0	[illegible]	E4	IO
0	[illegible]	E5	VREF
0	[illegible]	E7	IO
0	[illegible]	E8	VCCO
0	[illegible]	E10	IO
0	[illegible]	C1	IO
0	[illegible]	B1	IO
0	[illegible]	D1	IO
0	[illegible]	C1	IO
0	[illegible]	D1	VREF
0	[illegible]	D2	VCCO
0	[illegible]	D3	IO
0	[illegible]	D4	VREF
0	[illegible]	D6	IO
0	[illegible]	D7	IO
0	[illegible]	D8	IO
0	[illegible]	D10	IO

Table 68: Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA (Cont'd)

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	[illegible]		
0	[illegible]		
0	[illegible]		

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial release.
05/18/07	1.1	Added Bank 3 to Table 3-8, Table 3-9, Table 3-10, Table 3-11, Table 3-12, Table 3-13, Table 3-14, Table 3-15, and Table 3-16. Updated Table 3-17 for UG331 changes. Added Table 3-18 and Table 3-19. Updated Table 3-20 for UG331 changes. Added Table 3-21.
06/18/07	1.2	Updated Table 3-17 for UG331 changes.
07/16/07	2.0	Updated Table 3-17 for UG331 changes. Added Table 3-22.
06/02/08	2.1	Updated Table 3-17 for UG331 changes. Added Table 3-23.
03/11/09	2.2	Updated Table 3-17 for UG331 changes.
10/04/10	3.0	Updated Table 3-17 for UG331 changes.