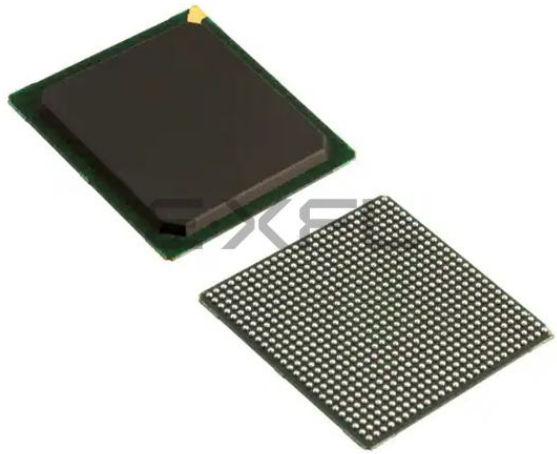

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Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-4fgg676i

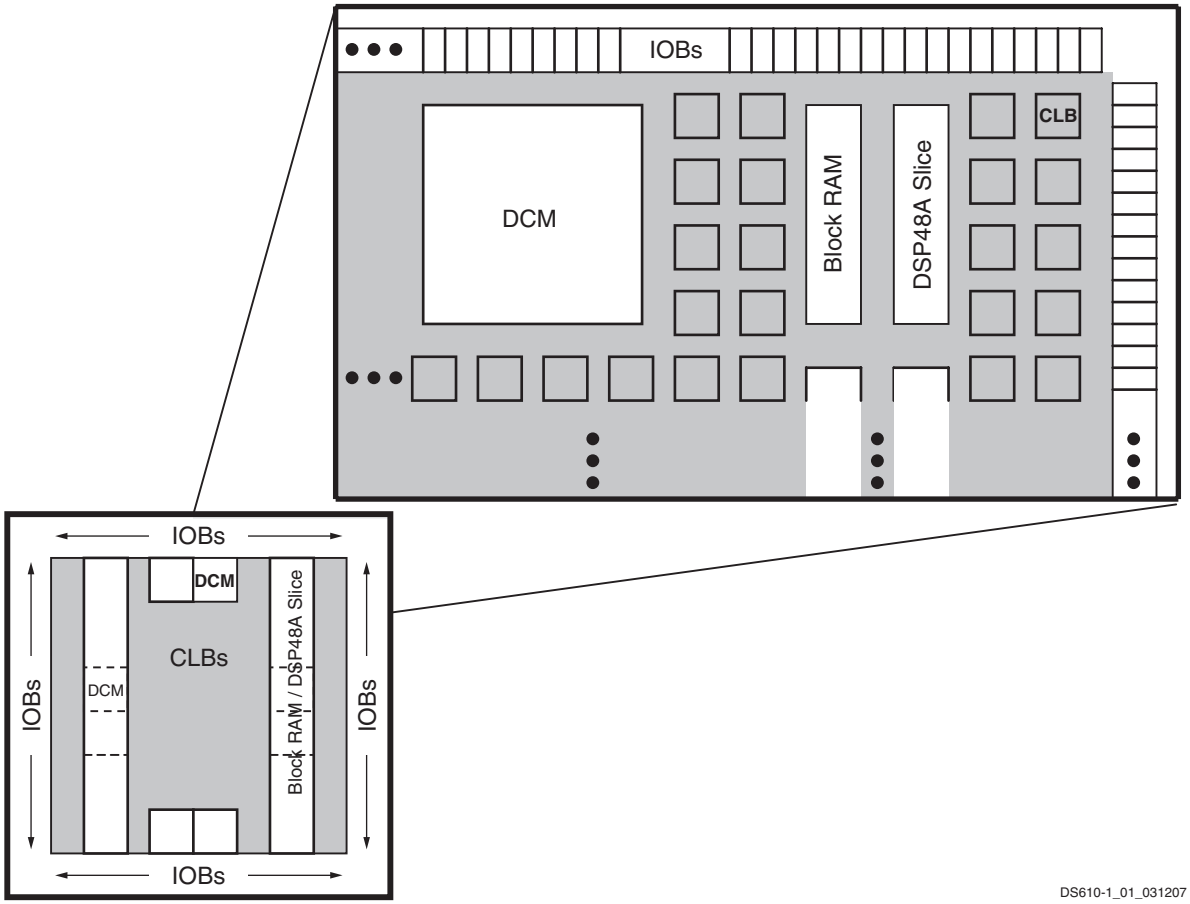
Architectural Overview

The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP™ DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XC3SD1800A has four columns of DSP48As, and the XC3SD3400A has five columns of DSP48As. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3SD1800A and XC3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer Block RAM/DSP48A columns of the 4 or 5 columns in the selected device, as shown in the diagram above.
2. A detailed diagram of the DSP48A can be found in UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide.*

Figure 1: **Spartan-3A DSP Family Architecture**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options; no changes to this module.
06/02/08	2.1	Updated links.
03/11/09	2.2	Added link to DS706 on Extended Spartan-3A family.
10/04/10	3.0	Updated link to sign up for Alerts and updated Notice of Disclaimer.

Notice of Disclaimer

Switching Characteristics

All Spartan-3A DSP FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 15. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs will require updating the Xilinx ISE development software with a future version and/or Service Pack.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 15. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 15: **Spartan-3A DSP v1.32 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3SD1800A			-4, -5
XC3SD3400A			-4, -5

Table 16 provides the recent history of the Spartan-3A DSP FPGA speed files.

Table 16: **Spartan-3A DSP Speed File Version History**

Version	ISE Release	Description
1.32	ISE 10.1.02	Updated DSP timing model to reflect higher performance for some implementations
1.31	ISE 10.1	Added Automotive support
1.30	ISE 9.2.03i	Added absolute minimum values
1.29	ISE 9.2.01i	Production Speed Files for -4 and -5 speed grades
1.28	ISE 9.2i	Minor updates
1.27	ISE 9.1.03i	Advance Speed Files for -4 speed grade

Pin-to-Pin Setup and Hold Times

Table 18: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	2.65	3.11	ns
			XC3SD3400A	2.25	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	2.98	3.39	ns
			XC3SD3400A	2.78	3.08	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	–0.38	–0.38	ns
			XC3SD3400A	–0.26	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	–0.71	–0.71	ns
			XC3SD3400A	–0.65	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 21: **Propagation Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XC3SD1800A	1.79	2.04	ns
				XC3SD3400A	1.65	2.11	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XC3SD1800A	2.23	2.47	ns
			2		2.81	3.06	ns
			3		3.39	3.86	ns
			4		3.89	4.43	ns
			5		3.83	4.39	ns
			6		4.61	5.32	ns
			7		5.40	6.24	ns
			8		5.93	6.86	ns
			1	XC3SD3400A	2.21	2.67	ns
			2		2.71	3.25	ns
			3		3.58	4.04	ns
			4		4.15	4.62	ns
			5		4.03	4.49	ns
			6		4.57	5.31	ns
			7		5.34	6.18	ns
			8		5.84	6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0.00	0.00	ns
SSTL2_II			–0.05	–0.05	ns
SSTL3_I			0.00	0.00	ns
SSTL3_II			0.17	0.17	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	1.16	1.16	ns
LVDS_33	0.46	0.46	ns
BLVDS_25	0.11	0.11	ns
MINI_LVDS_25	0.75	0.75	ns
MINI_LVDS_33	0.40	0.40	ns
LVPECL_25	Inputs Only		
LVPECL_33			
RSDS_25	1.42	1.42	ns
RSDS_33	0.58	0.58	ns
TMDS_33	0.46	0.46	ns
PPDS_25	1.07	1.07	ns
PPDS_33	0.63	0.63	ns
DIFF_HSTL_I_18	0.43	0.43	ns
DIFF_HSTL_II_18	0.41	0.41	ns
DIFF_HSTL_III_18	0.36	0.36	ns
DIFF_HSTL_I	1.01	1.01	ns
DIFF_HSTL_III	0.54	0.54	ns
DIFF_SSTL18_I	0.49	0.49	ns
DIFF_SSTL18_II	0.41	0.41	ns
DIFF_SSTL2_I	0.82	0.82	ns
DIFF_SSTL2_II	0.09	0.09	ns
DIFF_SSTL3_I	1.16	1.16	ns
DIFF_SSTL3_II	0.28	0.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. Note that 16 mA drive is faster than 24 mA drive for the Slow slew rate.

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS12	Slow	2	40	40
		4	–	25
		6	–	18
	Fast	2	31	31
		4	–	13
		6	–	9
	QuietIO	2	55	55
		4	–	36
		6	–	36
PCI33_3			16	16
PCI66_3			–	13
HSTL_I			–	20
HSTL_III			–	8
HSTL_I_18			17	17
HSTL_II_18			–	5
HSTL_III_18			10	8
SSTL18_I			7	15
SSTL18_II			–	9
SSTL2_I			18	18
SSTL2_II			–	9
SSTL3_I			8	10
SSTL3_II			6	7

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)	Package Type	
	CS484, FG676	
	Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Differential Standards (Number of I/O Pairs or Channels)		
LVDS_25	22	–
LVDS_33	27	–
BLVDS_25	4	4
MINI_LVDS_25	22	–
MINI_LVDS_33	27	–
LVPECL_25	Inputs Only	
LVPECL_33	Inputs Only	
RSDS_25	22	–
RSDS_33	27	–
TMDS_33	27	–
PPDS_25	22	–
PPDS_33	27	–
DIFF_HSTL_I_18	8	8
DIFF_HSTL_II_18	–	2
DIFF_HSTL_III_18	5	4
DIFF_HSTL_I	–	10
DIFF_HSTL_III	–	4
DIFF_SSTL18_I	3	7
DIFF_SSTL18_II	–	4
DIFF_SSTL2_I	9	9
DIFF_SSTL2_II	–	4
DIFF_SSTL3_I	4	5
DIFF_SSTL3_II	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Table 35: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

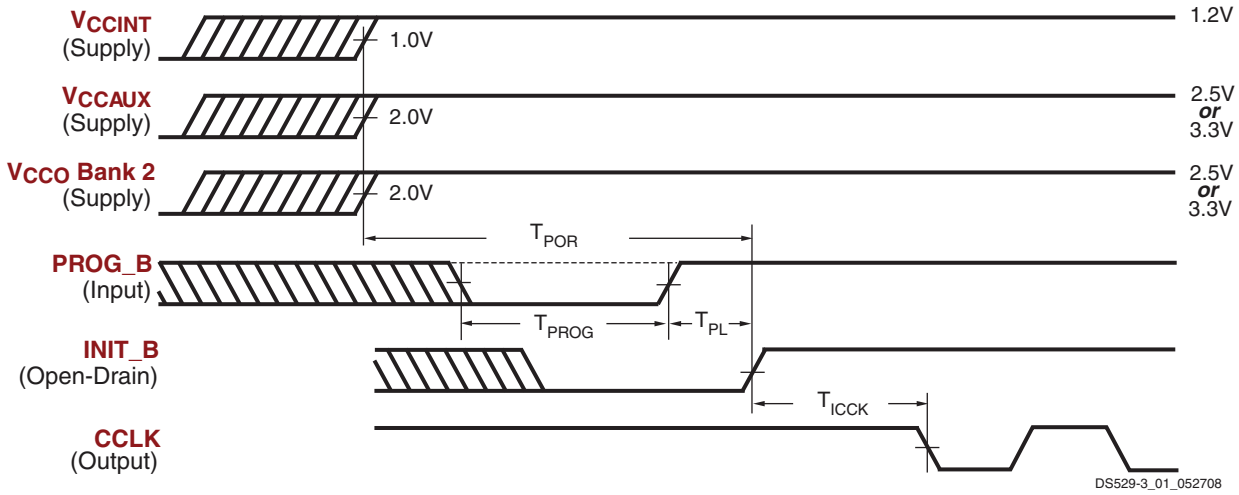
Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Max	Max	
Clock to Out from Output Register Clock to Output Pin							
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.26	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins							
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes	Yes	3.16	3.63	ns
		–	Yes	No	1.94	2.23	ns
Clock to Out from Input Register Clock to Output Pins							
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	6.33	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	7.45	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.37	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	7.33	8.42	ns
Combinatorial Delays from Input Pins to Output Pins							
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	2.78	3.19	ns
		–	Yes	No	4.60	5.28	ns
		–	Yes	Yes	5.65	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	3.49	4.01	ns
		Yes	Yes	No	5.79	6.65	ns
		Yes	Yes	Yes	6.74	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	2.76	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	6.81	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	7.12	8.18	ns
Maximum Frequency							
F_{MAX}	All registers used	Yes	Yes	Yes	287	250	MHz

Notes:

1. To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.
2. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in Table 7.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: **Waveforms for Power-On and the Beginning of Configuration**

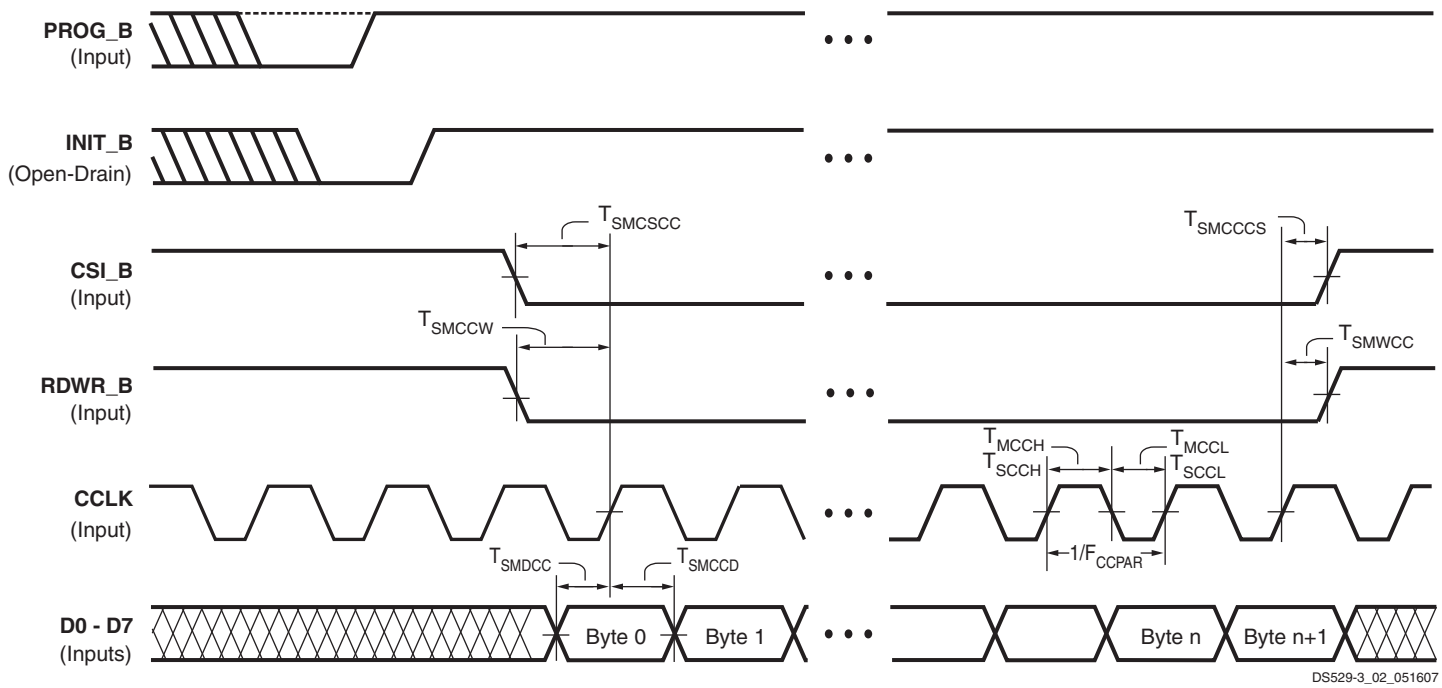
Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 12: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Serial Peripheral Interface (SPI) Configuration Timing

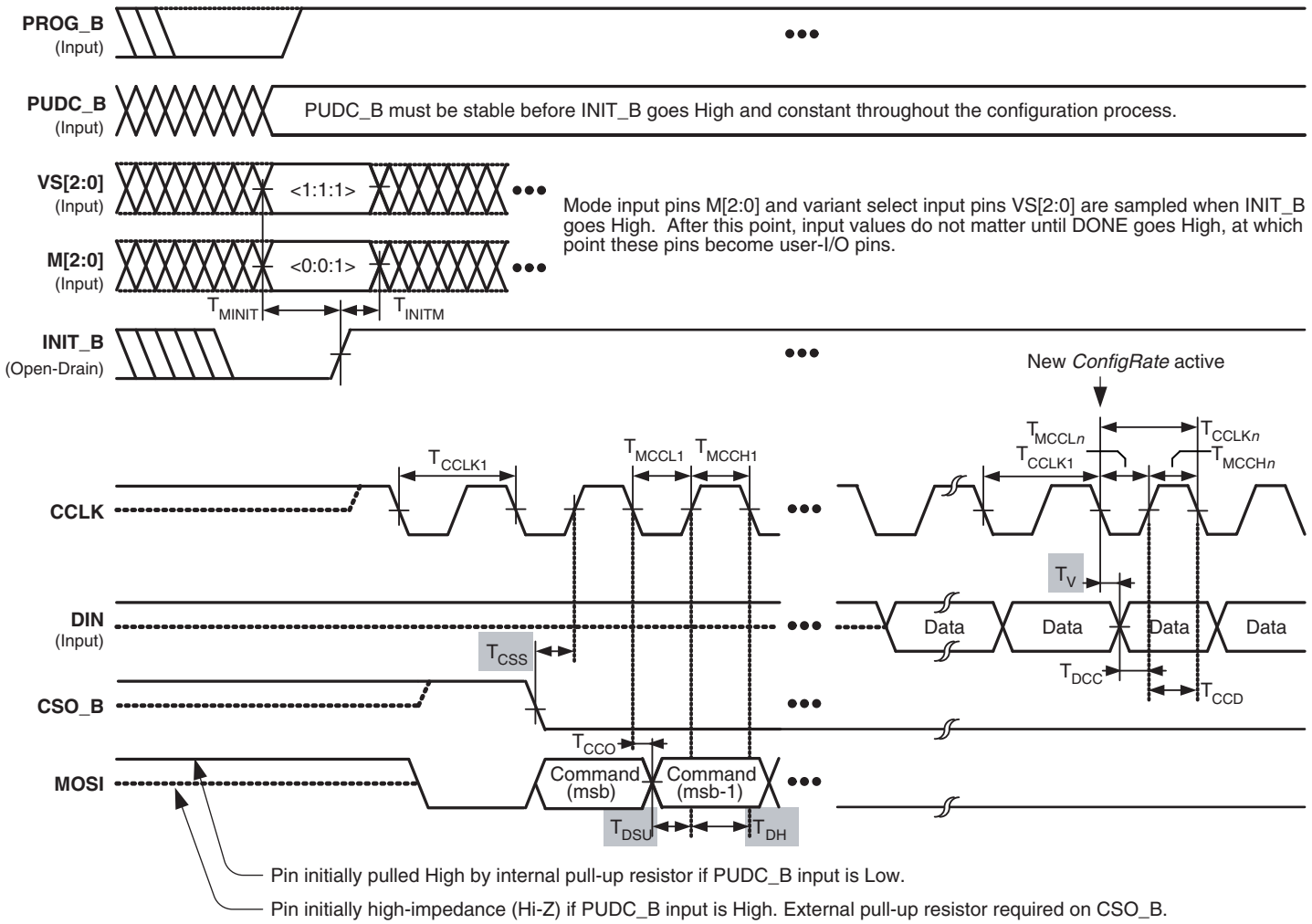


Figure 13: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 52: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on DIN data input before CCLK rising edge	See Table 50		
T_{CCD}	Hold time on DIN data input after CCLK rising edge	See Table 50		

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in UG331: *Spartan-3 Generation FPGA User Guide.*

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs**

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	T14	GND
GND	GND	T15	GND
GND	GND	T19	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U11	GND
GND	GND	U17	GND
GND	GND	W7	GND
GND	GND	W12	GND
GND	GND	W16	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	V19	PWRMGMT
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	DONE	AB21	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TMS	B1	JTAG
VCCAUX	TDO	B22	JTAG
VCCAUX	TDI	D2	JTAG
VCCAUX	VCCAUX	AA2	VCCAUX
VCCAUX	VCCAUX	AA21	VCCAUX
VCCAUX	VCCAUX	B2	VCCAUX
VCCAUX	VCCAUX	B21	VCCAUX
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	G12	VCCAUX
VCCAUX	VCCAUX	G14	VCCAUX
VCCAUX	VCCAUX	J16	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	L16	VCCAUX
VCCAUX	VCCAUX	M7	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N16	VCCAUX
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	T9	VCCAUX
VCCAUX	VCCAUX	T11	VCCAUX
VCCAUX	VCCAUX	T13	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G16	VCCINT
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	H15	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	J14	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	R8	VCCINT
VCCINT	VCCINT	R10	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	T7	VCCINT
VCCINT	VCCINT	T16	VCCINT

CS484 Footprint

Left Half of Package (Top View)

156 **I/O:** Unrestricted, general-purpose user I/O.

41 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

28 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins.

4 **JTAG:** Dedicated JTAG port pins.

84 **GND:** Ground.

24 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	I/O L30N_0	I/O L28N_0	I/O L25N_0	I/O L25P_0	I/O L24N_0 VREF_0	I/O L20P_0 GCLK10	I/O L18P_0 GCLK6	INPUT	I/O L15N_0
B	TMS	VCCAUX	I/O L30P_0	I/O L28P_0	VCCO_0	I/O L24P_0	GND	I/O L20N_0 GCLK11	I/O L18N_0 GCLK7	VCCO_0	I/O L15P_0
C	I/O L02N_3	I/O L02P_3	GND	I/O L29N_0	INPUT	I/O L21P_0	I/O L26P_0	I/O L22P_0	I/O L16P_0	INPUT	INPUT 0 VREF_0
D	INPUT L04P_3	TDI	INPUT L08P_3	INPUT L08N_3	I/O L29P_0	I/O L21N_0	I/O L26N_0	GND	I/O L22N_0	I/O L16N_0	GND
E	INPUT L04N_3 VREF_3	VCCO_3	I/O L09P_3	I/O L09N_3	VCCAUX	INPUT	I/O L31P_0 VREF_0	I/O L27N_0	VCCO_0	INPUT	I/O L19N_0 GCLK9
F	I/O L06N_3	I/O L06P_3	I/O L01P_3	I/O L03P_3	I/O L03N_3	GND	I/O L31N_0 PUDC_B	I/O L27P_0	I/O L23N_0	I/O L19P_0 GCLK8	I/O L17N_0 GCLK5
G	I/O L11P_3	GND	I/O L01N_3	GND	I/O L07P_3	I/O L07N_3	VCCINT	I/O L23P_0	GND	VCCAUX	GND
H	I/O L11N_3	I/O L14P_3	I/O L05P_3	I/O L05N_3	I/O L10P_3	I/O L10N_3	GND	GND	VCCINT	GND	VCCINT
J	I/O L14N_3 VREF_3	VCCO_3	INPUT L16P_3	INPUT L16N_3	VCCO_3	INPUT L12P_3	INPUT L12N_3 VREF_3	VCCINT	GND	VCCINT	GND
K	I/O L19P_3 LHCLK2	I/O L17P_3	I/O L17N_3	I/O L13P_3	I/O L13N_3	I/O L15P_3	VCCAUX	GND	VCCINT	GND	VCCINT
L	I/O L19N_3 IRDY2 LHCLK3	GND	I/O L20P_3 LHCLK4	VCCAUX	I/O L15N_3	I/O L18P_3 LHCLK0	GND	VCCINT	GND	VCCINT	GND
M	I/O L22P_3 VREF_3	I/O L20N_3 LHCLK5	INPUT L23P_3	GND	I/O L18N_3 LHCLK1	I/O L21P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	GND	VCCINT
N	I/O L22N_3	VCCO_3	INPUT L31P_3	INPUT L23N_3	I/O L24N_3	I/O L24P_3	I/O L21N_3 LHCLK7	VCCINT	GND	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT L31N_3	I/O L32P_3 VREF_3	VCCO_3	I/O L26P_3	VCCAUX	GND	VCCINT	GND	VCCINT
R	I/O L28N_3	I/O L28P_3	I/O L34P_3	GND	I/O L32N_3	I/O L26N_3	GND	VCCINT	GND	VCCINT	GND
T	I/O L30P_3	GND	INPUT L27P_3	I/O L34N_3	I/O L29N_3	I/O L29P_3	VCCINT	GND	VCCAUX	GND	VCCAUX
U	I/O L30N_3	I/O L33P_3	INPUT L27N_3	I/O L38P_3	I/O L38N_3	GND	I/O L02N_2 CSO_B	I/O L11N_2	I/O L10N_2	I/O L14N_2 D4	GND
V	I/O L33N_3	VCCO_3	I/O L36N_3	I/O L36P_3	VCCAUX	I/O L02P_2 M2	I/O L11P_2	I/O L06N_2	VCCO_2	I/O L10P_2	I/O L14P_2 D5
W	I/O L35N_3	I/O L37N_3	I/O L37P_3	INPUT 2 VREF_2	I/O L03P_2	I/O L07N_2 VS2	GND	I/O L06P_2	INPUT 2 VREF_2	INPUT	VCCAUX
Y	I/O L35P_3	INPUT L39P_3	GND	I/O L03N_2	I/O L07P_2 RDWR_B	INPUT	INPUT	I/O L13P_2	I/O L13N_2	I/O L15N_2 GCLK13	I/O L15P_2 GCLK12
AA	INPUT L39N_3 VREF_3	VCCAUX	I/O L01P_2 M1	I/O L04N_2	VCCO_2	INPUT	GND	I/O L08N_2	VCCO_2	I/O L12N_2 D6	GND
AB	GND	INPUT 2 VREF_2	I/O L01N_2 M0	I/O L04P_2	I/O L05P_2	I/O L05N_2	I/O L08P_2	I/O L09P_2 VS1	I/O L09N_2 VS0	I/O L12P_2 D7	INPUT 2 VREF_2

Bank 3 (left) **Bank 2** (bottom)

Figure 15: **CS484 Package Footprint (Top View–Left Half)**

Right Half of CS484 Package (Top View)

Figure 16: CS484 Package Footprint (Top View–Right Half)

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IP_2	AF7	INPUT
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

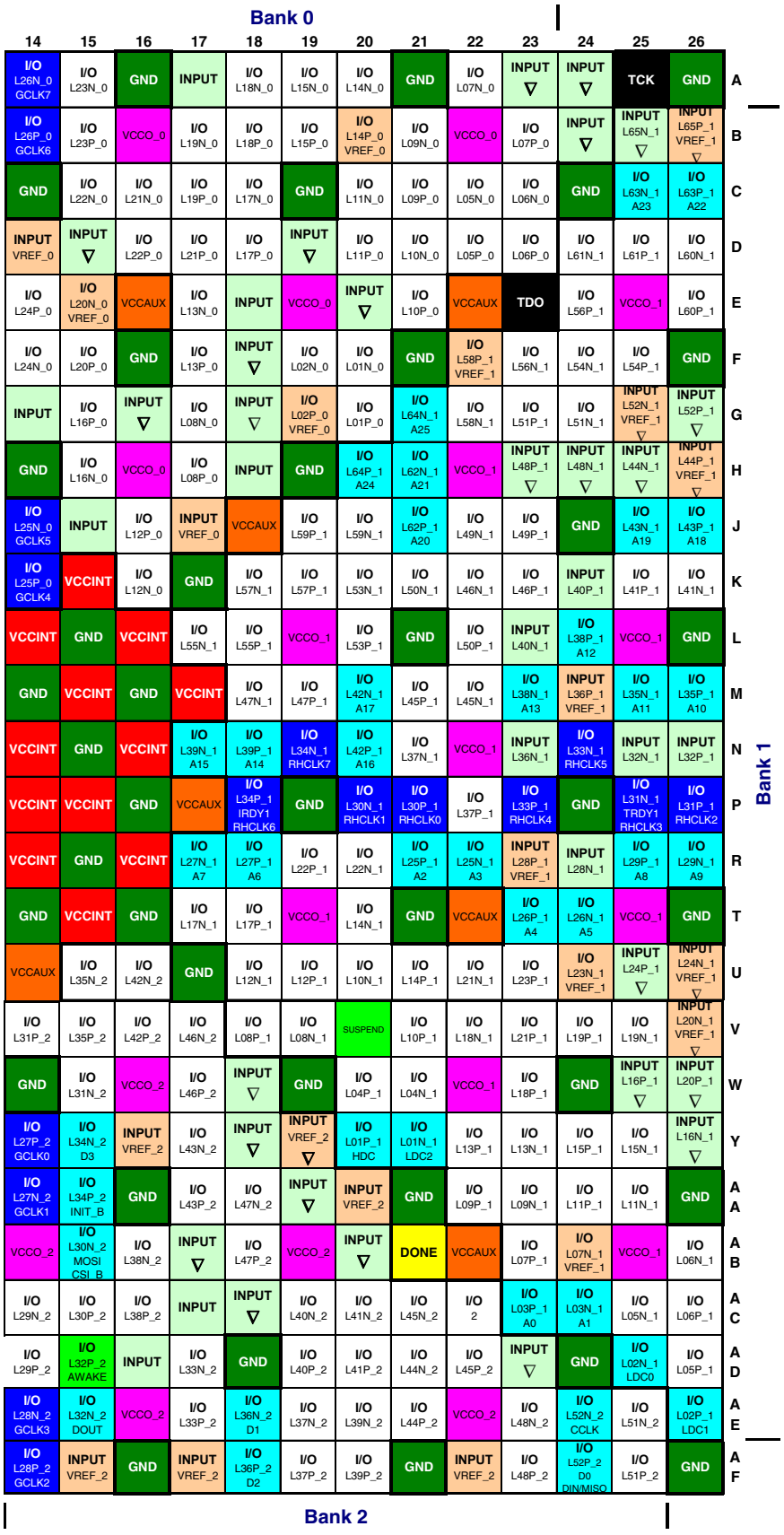
Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O



Right Half of FG676 Package (Top View)

Figure 17: FG676 Package Footprint for XC3SD1800A FPGA (Top View–Right Half)

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_1	H24	INPUT
1	IP_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	G2	GND
GND	GND	G5	GND
GND	GND	G16	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	E9	GND
GND	GND	D2	GND
GND	GND	D15	GND
GND	GND	D19	GND
GND	GND	C3	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	C9	GND
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	B24	GND
GND	GND	B25	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	AD3	GND
GND	GND	AD5	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD23	GND
GND	GND	AD24	GND
GND	GND	AC5	GND
GND	GND	AC7	GND
GND	GND	AC18	GND
GND	GND	AB3	GND
GND	GND	AB10	GND
GND	GND	AB20	GND
GND	GND	AA1	GND
GND	GND	AA4	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA19	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	A1	GND
GND	GND	A5	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND