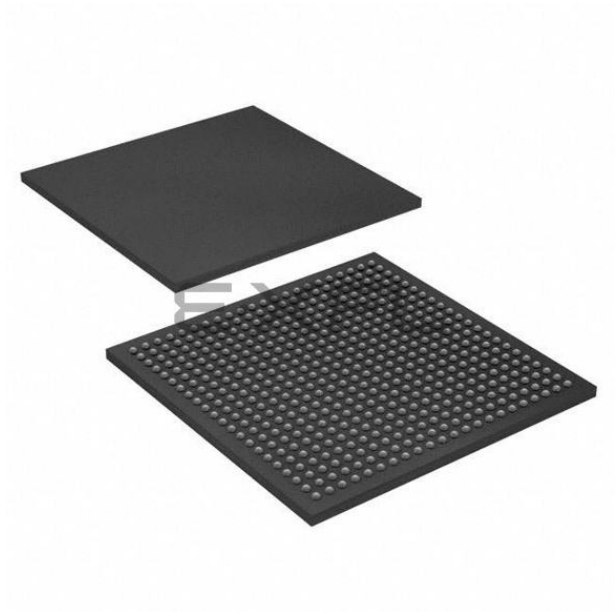
AMD Xilinx - XC3SD3400A-5CSG484C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-5csg484c

Spartan-3A DSP FPGA Family: Introduction and Ordering Information

DS610 (v3.0) October 4, 2010 **Product Specification**

Introduction

The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high- volume, cost-sensitive, high-performance DSP applications. The two-member family offers densities ranging from 1.8 to 3.4 million system gates, as shown in Table 1.

The Spartan-3A DSP family builds on the success of the Spartan-3A FPGA family by increasing the amount of memory per logic and adding XtremeDSP™ DSP48A slices. New features improve system performance and reduce the cost of configuration. These Spartan-3A DSP FPGA enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic and DSP processing industry.

The Spartan-3A DSP FPGAs extend and enhance the Spartan-3A FPGA family. The XC3SD1800A and the XC3SD3400A devices are tailored for DSP applications and have additional block RAM and XtremeDSP DSP48A slices. The XtremeDSP DSP48A slices replace the 18x18 multipliers found in the Spartan-3A devices and are based on the DSP48 blocks found in the Virtex®-4 devices. The block RAMs are also enhanced to run faster by adding an output register. Both the block RAM and DSP48A slices in the Spartan-3A DSP devices run at 250 MHz in the lowest cost, standard -4 speed grade.

Because of their exceptional DSP price/performance ratio, Spartan-3A DSP FPGAs are ideally suited to a wide range of consumer electronics applications, such as broadband access, home networking, display/projection, and digital television.

The Spartan-3A DSP family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance DSP solution for high-volume, cost-conscious applications
- 250 MHz XtremeDSP DSP48A Slices
  - Dedicated 18-bit by 18-bit multiplier
  - Available pipeline stages for enhanced performance of at least 250 MHz in the standard -4 speed grade
  - 48-bit accumulator for multiply-accumulate (MAC) operation
  - Integrated adder for complex multiply or multiply-add operation
  - Integrated 18-bit pre-adder
  - Optional cascaded Multiply or MAC
- Hierarchical SelectRAM™ memory architecture
  - Up to 2268 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 373 Kbits of efficient distributed RAM
  - Registered outputs on the block RAM with operation of at least 280 MHz in the standard -4 speed grade
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Low-power option reduces quiescent current
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 519 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 622+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 333 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI support
- Abundant, flexible logic resources
  - Densities up to 53712 logic cells, including optional shift register
  - Efficient wide multiplexers, wide logic, fast carry logic
  - IEEE 1149.1/1532 JTAG programming/debug port
- Eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- BGA and CSP packaging with Pb-free options
  - Common footprints support easy density migration
- XA Automotive version available

Table 1: **Summary of Spartan-3A DSP FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits(1)	Block RAM Bits(1)	DSP48As	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XC3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

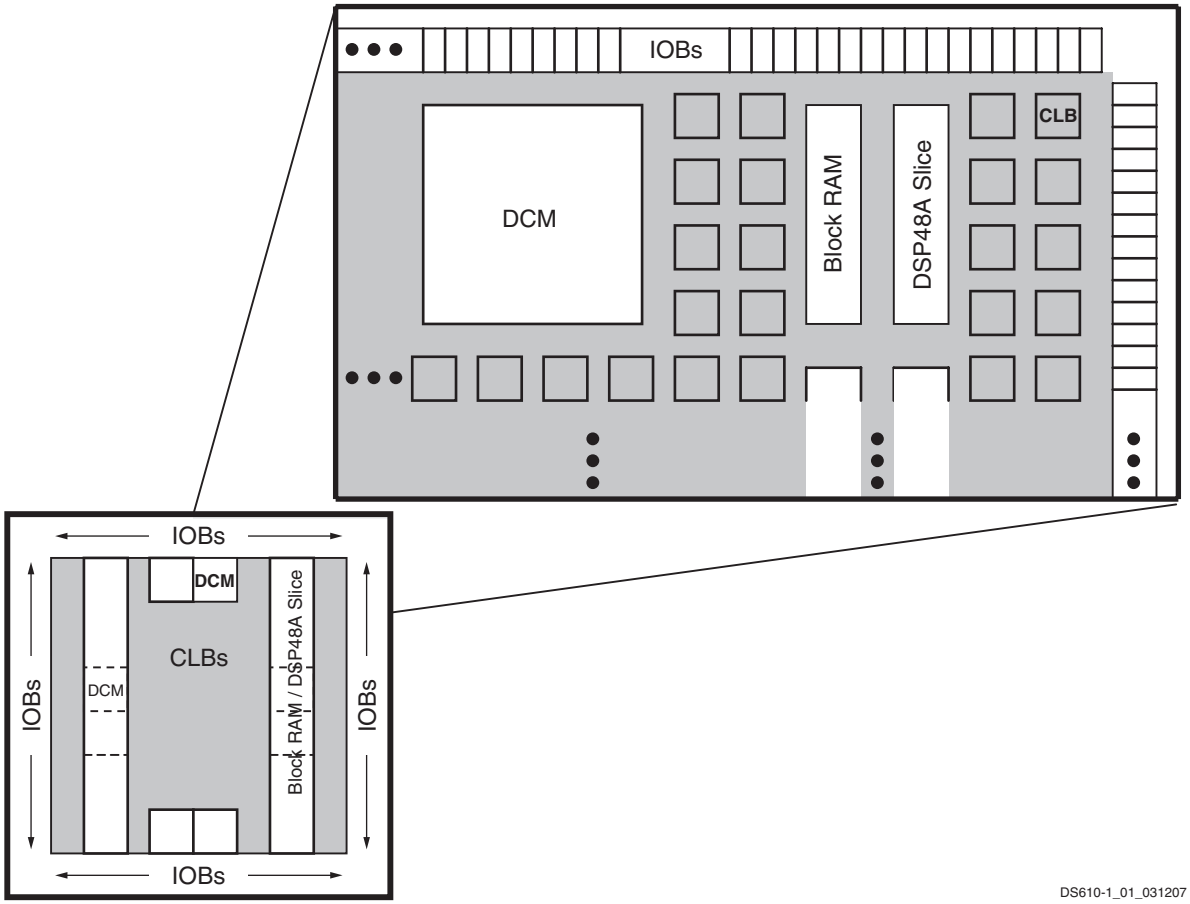
Architectural Overview

The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP™ DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XC3SD1800A has four columns of DSP48As, and the XC3SD3400A has five columns of DSP48As. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3SD1800A and XC3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer Block RAM/DSP48A columns of the 4 or 5 columns in the selected device, as shown in the diagram above.
2. A detailed diagram of the DSP48A can be found in UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide.*

Figure 1: **Spartan-3A DSP Family Architecture**

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 3: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 3: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON} (2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON} (2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Configurable Logic Block (CLB) Timing

Table 29: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0.00	–	0.00	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.00	–	0.00	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Clock Buffer/Multiplexer Switching Characteristics

Table 32: **Clock Distribution Switching Characteristics**

Symbol	Description	Minimum	Maximum		Units
			Speed Grade		
			-5	-4	
T_{GIO}	Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	–	0.22	0.23	ns
T_{GSI}	Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	–	0.56	0.63	ns
F_{BUFG}	Frequency of signals distributed on global buffers (all sides)	0	350	334	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 36 and Table 37) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 38 through Table 41) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 36 and Table 37.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469: *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 36: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	280(3)	5(2)	250(3)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz	40%	60%	40%	60%	–
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	–
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 38.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter (2)(3)(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz < FCLKIN < 15 MHz	All	–	5	–	5	ms
		FCLKIN > 15 MHz		–	600	–	600	µs

Suspend Mode Timing

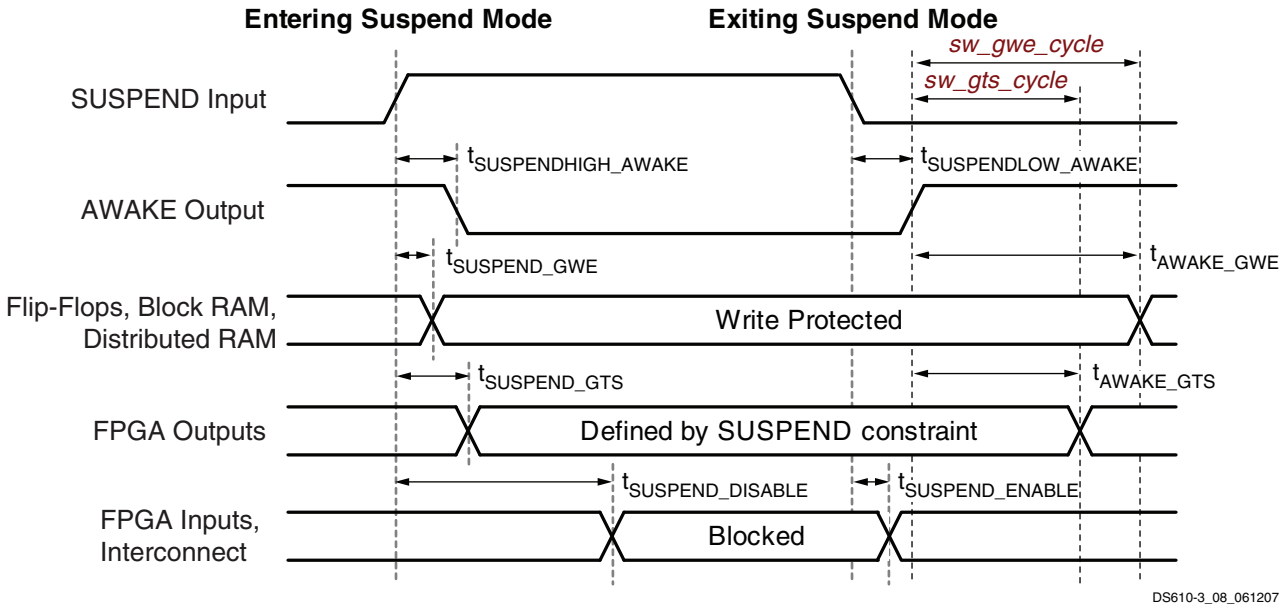


Figure 9: **Suspend Mode Timing**

Table 44: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A DSP Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Configuration Clock (CCLK) Characteristics

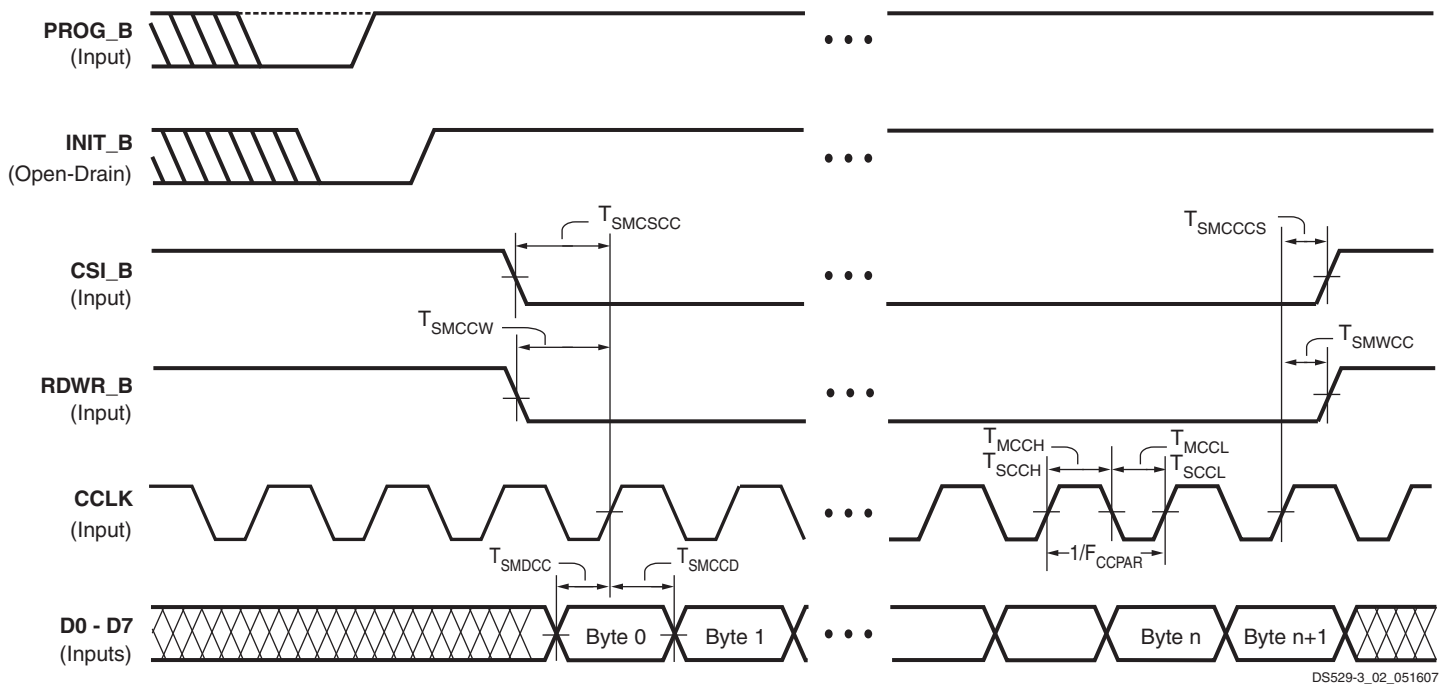
Table 46: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting[1]	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 12: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A DSP FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 62 provides the thermal characteristics for the various Spartan-3A DSP device package offerings. This information is also available using the Thermal Query tool.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 62: **Spartan-3A DSP FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
CS484 CSG484	XC3SD1800A	4.1	6.8	18.0	13.3	12.3	11.5	°C/W
	XC3SD3400A	3.5	5.6	16.9	12.2	11.0	10.4	°C/W
FG676 FGG676	XC3SD1800A	4.7	7.8	15.9	11.6	10.6	10.0	°C/W
	XC3SD3400A	3.8	6.4	14.7	10.5	9.4	8.9	°C/W

CS484: 484-Ball Chip-Scale Ball Grid Array

The 484-ball chip-scale ball grid array, CS484, supports both the XC3SD1800A and XC3SD3400A FPGAs. There are no pinout differences between the two devices.

Table 63 lists all the CS484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 63: **Spartan-3A DSP CS484 Pinout**

Bank	Pin Name	CS484 Ball	Type
0	IO_L30N_0	A3	I/O
0	IO_L28N_0	A4	I/O
0	IO_L25N_0	A5	I/O
0	IO_L25P_0	A6	I/O
0	IO_L24N_0/VREF_0	A7	VREF
0	IO_L20P_0/GCLK10	A8	GCLK
0	IO_L18P_0/GCLK6	A9	GCLK
0	IP_0	A10	INPUT
0	IO_L15N_0	A11	I/O
0	IP_0	A12	INPUT
0	IO_L11P_0	A13	I/O
0	IO_L10P_0	A14	I/O
0	IP_0	A15	INPUT
0	IO_L06P_0/VREF_0	A16	VREF
0	IO_L06N_0	A17	I/O
0	IP_0	A18	INPUT
0	IO_L07N_0	A19	I/O
0	IO_0	A20	I/O
0	IO_L30P_0	B3	I/O
0	IO_L28P_0	B4	I/O
0	IO_L24P_0	B6	I/O
0	IO_L20N_0/GCLK11	B8	GCLK
0	IO_L18N_0/GCLK7	B9	GCLK
0	IO_L15P_0	B11	I/O
0	IO_L11N_0	B13	I/O
0	IO_L10N_0	B15	I/O
0	IO_L03P_0	B17	I/O
0	IO_L02N_0	B19	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L07P_0	B20	I/O
0	IO_L29N_0	C4	I/O
0	IP_0	C5	INPUT
0	IO_L21P_0	C6	I/O
0	IO_L26P_0	C7	I/O
0	IO_L22P_0	C8	I/O
0	IO_L16P_0	C9	I/O
0	IP_0	C10	INPUT
0	IP_0/VREF_0	C11	VREF
0	IO_L14N_0	C12	I/O
0	IO_L14P_0	C13	I/O
0	IP_0	C14	INPUT
0	IO_L12N_0/VREF_0	C15	VREF
0	IO_L08N_0	C16	I/O
0	IO_L03N_0	C17	I/O
0	IO_L02P_0/VREF_0	C18	VREF
0	IO_L01N_0	C19	I/O
0	IO_L29P_0	D5	I/O
0	IO_L21N_0	D6	I/O
0	IO_L26N_0	D7	I/O
0	IO_L22N_0	D9	I/O
0	IO_L16N_0	D10	I/O
0	IO_L09N_0	D13	I/O
0	IO_L12P_0	D14	I/O
0	IO_L08P_0	D15	I/O
0	IP_0	D17	INPUT
0	IP_0	D18	INPUT
0	IO_L01P_0	D19	I/O
0	IP_0	E6	INPUT
0	IO_L31P_0/VREF_0	E7	VREF
0	IO_L27N_0	E8	I/O
0	IP_0	E10	INPUT
0	IO_L19N_0/GCLK9	E11	GCLK
0	IO_L17P_0/GCLK4	E12	GCLK
0	IO_L09P_0	E13	I/O
0	IO_L05P_0	E15	I/O
0	IO_L04P_0	E16	I/O
0	IP_0	E17	INPUT
0	IO_L31N_0/PUDC_B	F7	DUAL
0	IO_L27P_0	F8	I/O
0	IO_L23N_0	F9	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IO_L03N_1/A1	V20	DUAL
1	IP_L08P_1	V22	INPUT
1	IO_L03P_1/A0	W19	DUAL
1	IP_L04N_1/VREF_1	W20	VREF
1	IP_L04P_1	W21	INPUT
1	IO_L06P_1	W22	I/O
1	IO_L02P_1/LDC1	Y21	DUAL
1	IO_L06N_1	Y22	I/O
1	VCCO_1	E21	VCCO
1	VCCO_1	J18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P18	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01P_2/M1	AA3	DUAL
2	IO_L04N_2	AA4	I/O
2	IP_2	AA6	INPUT
2	IO_L08N_2	AA8	I/O
2	IO_L12N_2/D6	AA10	DUAL
2	IO_L16P_2/GCLK14	AA12	GCLK
2	IO_L18N_2/GCLK3	AA14	GCLK
2	IO_L19P_2	AA15	I/O
2	IO_L22P_2/AWAKE	AA17	PWRMGMT
2	IO_L27N_2	AA19	I/O
2	IO_L30P_2	AA20	I/O
2	IP_2/VREF_2	AB2	VREF
2	IO_L01N_2/M0	AB3	DUAL
2	IO_L04P_2	AB4	I/O
2	IO_L05P_2	AB5	I/O
2	IO_L05N_2	AB6	I/O
2	IO_L08P_2	AB7	I/O
2	IO_L09P_2/VS1	AB8	DUAL
2	IO_L09N_2/VS0	AB9	DUAL
2	IO_L12P_2/D7	AB10	DUAL
2	IP_2/VREF_2	AB11	VREF
2	IO_L16N_2/GCLK15	AB12	GCLK
2	IO_L18P_2/GCLK2	AB13	GCLK
2	IO_L19N_2	AB14	I/O
2	IP_2	AB15	INPUT
2	IO_L22N_2/DOUT	AB16	DUAL
2	IO_L23P_2	AB17	I/O
2	IO_L23N_2	AB18	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IO_L27P_2	AB19	I/O
2	IO_L30N_2	AB20	I/O
2	IO_L02N_2/CSO_B	U7	DUAL
2	IO_L11N_2	U8	I/O
2	IO_L10N_2	U9	I/O
2	IO_L14N_2/D4	U10	DUAL
2	IO_L17P_2/GCLK0	U12	GCLK
2	IO_L20P_2	U13	I/O
2	IO_L25P_2	U14	I/O
2	IO_L25N_2	U15	I/O
2	IO_L28P_2	U16	I/O
2	IO_L02P_2/M2	V6	DUAL
2	IO_L11P_2	V7	I/O
2	IO_L06N_2	V8	I/O
2	IO_L10P_2	V10	I/O
2	IO_L14P_2/D5	V11	DUAL
2	IO_L17N_2/GCLK1	V12	GCLK
2	IO_L20N_2/MOSI/CSI_B	V13	DUAL
2	IP_2/VREF_2	V15	VREF
2	IO_L28N_2	V16	I/O
2	IO_L31N_2/CCLK	V17	DUAL
2	IP_2/VREF_2	W4	VREF
2	IO_L03P_2	W5	I/O
2	IO_L07N_2/VS2	W6	DUAL
2	IO_L06P_2	W8	I/O
2	IP_2/VREF_2	W9	VREF
2	IP_2	W10	INPUT
2	IP_2/VREF_2	W13	VREF
2	IO_L21N_2	W14	I/O
2	IO_L24P_2/INIT_B	W15	DUAL
2	IO_L31P_2/D0/DIN/MISO	W17	DUAL
2	IP_2/VREF_2	W18	VREF
2	IO_L03N_2	Y4	I/O
2	IO_L07P_2/RDWR_B	Y5	DUAL
2	IP_2	Y6	INPUT
2	IP_2	Y7	INPUT
2	IO_L13P_2	Y8	I/O
2	IO_L13N_2	Y9	I/O
2	IO_L15N_2/GCLK13	Y10	GCLK
2	IO_L15P_2/GCLK12	Y11	GCLK
2	IP_2	Y12	INPUT
2	IO_L21P_2	Y13	I/O

CS484 Footprint

Left Half of Package (Top View)

156 **I/O:** Unrestricted, general-purpose user I/O.

41 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

28 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins.

4 **JTAG:** Dedicated JTAG port pins.

84 **GND:** Ground.

24 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	I/O L30N_0	I/O L28N_0	I/O L25N_0	I/O L25P_0	I/O L24N_0 VREF_0	I/O L20P_0 GCLK10	I/O L18P_0 GCLK6	INPUT	I/O L15N_0
B	TMS	VCCAUX	I/O L30P_0	I/O L28P_0	VCCO_0	I/O L24P_0	GND	I/O L20N_0 GCLK11	I/O L18N_0 GCLK7	VCCO_0	I/O L15P_0
C	I/O L02N_3	I/O L02P_3	GND	I/O L29N_0	INPUT	I/O L21P_0	I/O L26P_0	I/O L22P_0	I/O L16P_0	INPUT	INPUT 0 VREF_0
D	INPUT L04P_3	TDI	INPUT L08P_3	INPUT L08N_3	I/O L29P_0	I/O L21N_0	I/O L26N_0	GND	I/O L22N_0	I/O L16N_0	GND
E	INPUT L04N_3 VREF_3	VCCO_3	I/O L09P_3	I/O L09N_3	VCCAUX	INPUT	I/O L31P_0 VREF_0	I/O L27N_0	VCCO_0	INPUT	I/O L19N_0 GCLK9
F	I/O L06N_3	I/O L06P_3	I/O L01P_3	I/O L03P_3	I/O L03N_3	GND	I/O L31N_0 PUDC_B	I/O L27P_0	I/O L23N_0	I/O L19P_0 GCLK8	I/O L17N_0 GCLK5
G	I/O L11P_3	GND	I/O L01N_3	GND	I/O L07P_3	I/O L07N_3	VCCINT	I/O L23P_0	GND	VCCAUX	GND
H	I/O L11N_3	I/O L14P_3	I/O L05P_3	I/O L05N_3	I/O L10P_3	I/O L10N_3	GND	GND	VCCINT	GND	VCCINT
J	I/O L14N_3 VREF_3	VCCO_3	INPUT L16P_3	INPUT L16N_3	VCCO_3	INPUT L12P_3	INPUT L12N_3 VREF_3	VCCINT	GND	VCCINT	GND
K	I/O L19P_3 LHCLK2	I/O L17P_3	I/O L17N_3	I/O L13P_3	I/O L13N_3	I/O L15P_3	VCCAUX	GND	VCCINT	GND	VCCINT
L	I/O L19N_3 IRDY2 LHCLK3	GND	I/O L20P_3 LHCLK4	VCCAUX	I/O L15N_3	I/O L18P_3 LHCLK0	GND	VCCINT	GND	VCCINT	GND
M	I/O L22P_3 VREF_3	I/O L20N_3 LHCLK5	INPUT L23P_3	GND	I/O L18N_3 LHCLK1	I/O L21P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	GND	VCCINT
N	I/O L22N_3	VCCO_3	INPUT L31P_3	INPUT L23N_3	I/O L24N_3	I/O L24P_3	I/O L21N_3 LHCLK7	VCCINT	GND	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT L31N_3	I/O L32P_3 VREF_3	VCCO_3	I/O L26P_3	VCCAUX	GND	VCCINT	GND	VCCINT
R	I/O L28N_3	I/O L28P_3	I/O L34P_3	GND	I/O L32N_3	I/O L26N_3	GND	VCCINT	GND	VCCINT	GND
T	I/O L30P_3	GND	INPUT L27P_3	I/O L34N_3	I/O L29N_3	I/O L29P_3	VCCINT	GND	VCCAUX	GND	VCCAUX
U	I/O L30N_3	I/O L33P_3	INPUT L27N_3	I/O L38P_3	I/O L38N_3	GND	I/O L02N_2 CSO_B	I/O L11N_2	I/O L10N_2	I/O L14N_2 D4	GND
V	I/O L33N_3	VCCO_3	I/O L36N_3	I/O L36P_3	VCCAUX	I/O L02P_2 M2	I/O L11P_2	I/O L06N_2	VCCO_2	I/O L10P_2	I/O L14P_2 D5
W	I/O L35N_3	I/O L37N_3	I/O L37P_3	INPUT 2 VREF_2	I/O L03P_2	I/O L07N_2 VS2	GND	I/O L06P_2	INPUT 2 VREF_2	INPUT	VCCAUX
Y	I/O L35P_3	INPUT L39P_3	GND	I/O L03N_2	I/O L07P_2 RDWR_B	INPUT	INPUT	I/O L13P_2	I/O L13N_2	I/O L15N_2 GCLK13	I/O L15P_2 GCLK12
AA	INPUT L39N_3 VREF_3	VCCAUX	I/O L01P_2 M1	I/O L04N_2	VCCO_2	INPUT	GND	I/O L08N_2	VCCO_2	I/O L12N_2 D6	GND
AB	GND	INPUT 2 VREF_2	I/O L01N_2 M0	I/O L04P_2	I/O L05P_2	I/O L05N_2	I/O L08P_2	I/O L09P_2 VS1	I/O L09N_2 VS0	I/O L12P_2 D7	INPUT 2 VREF_2

Bank 3 (left) **Bank 2** (bottom)

Figure 15: **CS484 Package Footprint (Top View–Left Half)**

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_3/VREF_3	C1	VREF
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_3/VREF_3	AA5	VREF
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	C2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	W25	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	U25	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	G2	GND
GND	GND	G5	GND
GND	GND	G16	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	E9	GND
GND	GND	D2	GND
GND	GND	D15	GND
GND	GND	D19	GND
GND	GND	C3	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	C9	GND
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	B24	GND
GND	GND	B25	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	AD3	GND
GND	GND	AD5	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD23	GND
GND	GND	AD24	GND
GND	GND	AC5	GND
GND	GND	AC7	GND
GND	GND	AC18	GND
GND	GND	AB3	GND
GND	GND	AB10	GND
GND	GND	AB20	GND
GND	GND	AA1	GND
GND	GND	AA4	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA19	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	A1	GND
GND	GND	A5	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND

User I/Os by Bank

Table 69 indicates how the available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 69: **User I/Os Per Bank for the XC3SD3400A in the FG676 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	111	82	11	1	9	8
Right	1	123	67	8	30	10	8
Bottom	2	112	68	6	21	9	8
Left	3	123	97	9	0	9	8
TOTAL		**469**	**314**	**34**	**52**	**37**	**32**

Notes:

1. 26 VREF are on INPUT pins.

FG676 Footprint – XC3SD3400A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

34 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

37 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

4 **JTAG:** Dedicated JTAG port pins.

100 **GND:** Ground

40 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with question marks inside indicate pin differences from the XC3SD1800A device. Please see the Footprint Migration Differences section for more information.

	Bank 0												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	GND ▽	GND	VCCO_0 ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT VREF_3 ▽	VCCO_3 ▽	GND	VCCINT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	VCCAUX ▽	GND ▽	I/O L06P_3	TMS	VCCINT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VCCINT ▽	I/O L48N_0	VCCO_0	GND ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	VCCAUX ▽	VCCINT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT ▽	GND ▽	I/O L14P_3	I/O L09N_3	GND ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT ▽	VCCINT ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	VCCINT ▽	I/O L05N_2	I/O L12P_2	VCCINT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	GND ▽	INPUT VREF_3 ▽	GND	I/O L02N_2 CSO_B	VCCINT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	GND ▽	VCCAUX ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	GND ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	GND ▽	I/O L08P_2	GND ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	GND ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	VCCAUX ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	VCCO_2 ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Left Half)**