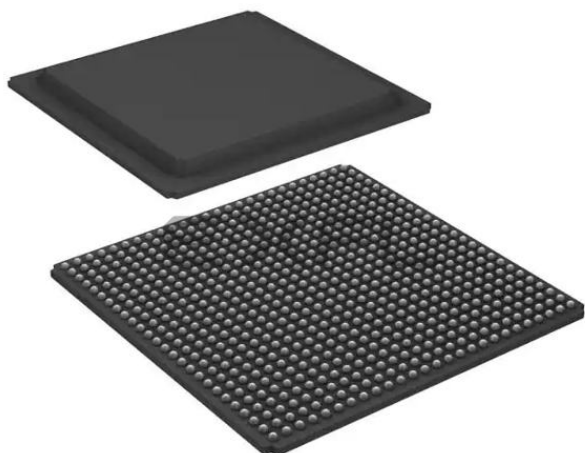




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-5fg676c

Spartan-3A DSP FPGA Design Documentation

The functionality of the Spartan®-3A DSP FPGA family is described in the following documents. The topics covered in each guide are listed.

- [DS706](#): *Extended Spartan-3A Family Overview*
 - [UG331](#): *Spartan-3 Generation FPGA User Guide*
 - Clocking Resources
 - Digital Clock Managers (DCMs)
 - Block RAM
 - Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
 - I/O Resources
 - Programmable Interconnect
 - ISE® Software Design Tools
 - IP Cores
 - Embedded Processing and Control Solutions
 - Pin Types and Package Overview
 - Package Drawings
 - Powering FPGAs
 - Power Management
 - [UG332](#): *Spartan-3 Generation Configuration User Guide*
 - Configuration Overview
 - Configuration Pins and Behavior
 - Bitstream Sizes
 - Detailed Descriptions by Mode
 - Master Serial Mode using Xilinx Platform Flash PROM
 - Master SPI Mode using Commodity SPI Serial Flash PROM
 - Master BPI Mode using Commodity Parallel NOR Flash PROM
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
 - ISE iMPACT Programming Examples
 - MultiBoot Reconfiguration
 - Design Authentication using Device DNA
 - [UG431](#): *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*
 - XtremeDSP DSP48A Slices
 - XtremeDSP DSP48A Pre-Adder
- For specific hardware examples, please see the Spartan-3A DSP FPGA Starter Kit board web pages.
- **XtremeDSP Starter Platform—Spartan-3A DSP 1800A Edition**
<http://www.xilinx.com/products/devkits/HW-SD1800A-DSP-SB-UNI-G.htm>
 - **XtremeDSP Starter Kit—Spartan-3A DSP 1800A Edition**
<http://www.xilinx.com/products/devkits/DO-SD1800A-DSP-SK-UNI-G.htm>
 - **XtremeDSP Video Starter Kit—Spartan-3A DSP Edition**
<http://www.xilinx.com/products/devkits/DO-S3ADSP-VIDEO-SK-UNI-G.htm>
 - **Embedded Development HW/SW Kit—Spartan-3A DSP S3D1800A MicroBlaze Processor Edition**
<http://www.xilinx.com/products/devkits/DO-SD1800A-EDK-DK-UNI-G.htm>
- Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.
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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options; no changes to this module.
06/02/08	2.1	Updated links.
03/11/09	2.2	Added link to DS706 on Extended Spartan-3A family.
10/04/10	3.0	Updated link to sign up for Alerts and updated Notice of Disclaimer .

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Power Supply Specifications

Table 4: Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the [UG331](#) chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the [UG331](#) chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

General DC Characteristics for I/O Pins

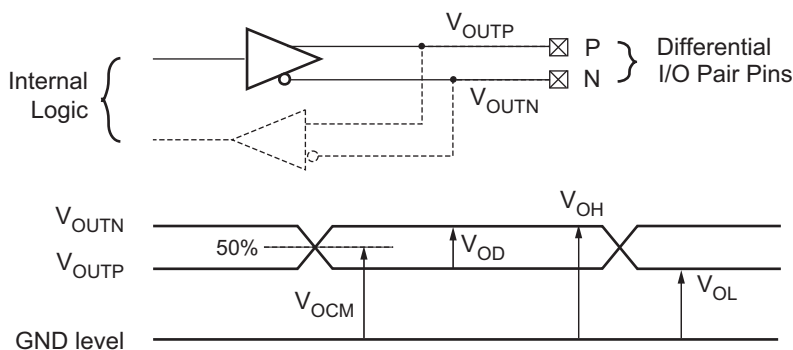
Table 8: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins ⁽¹⁾

Symbol	Description	Test Conditions		Min	Typ	Max	Units
$I_L^{(2)}$	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered	Driver is in a high-impedance state, $V_{IN} = 0V$ or V_{CCO} max, sample-tested		-10	—	+10	μA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		-10	—	+10	μA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add $I_{HS} + I_{RPU}$			μA
$I_{RPU}^{(3)}$	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by V_{CCAUX} .	$V_{IN} = GND$	V_{CCO} or $V_{CCAUX} = 3.0V$ to $3.6V$	-151	-315	-710	μA
			V_{CCO} or $V_{CCAUX} = 2.3V$ to $2.7V$	-82	-182	-437	μA
			$V_{CCO} = 1.7V$ to $1.9V$	-36	-88	-226	μA
			$V_{CCO} = 1.4V$ to $1.6V$	-22	-56	-148	μA
			$V_{CCO} = 1.14V$ to $1.26V$	-11	-31	-83	μA
$R_{PU}^{(3)}$	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	$V_{IN} = GND$	$V_{CCO} = 3.0V$ to $3.6V$	5.1	11.4	23.9	$k\Omega$
			$V_{CCO} = 2.3V$ to $2.7V$	6.2	14.8	33.1	$k\Omega$
			$V_{CCO} = 1.7V$ to $1.9V$	8.4	21.6	52.6	$k\Omega$
			$V_{CCO} = 1.4V$ to $1.6V$	10.8	28.4	74.0	$k\Omega$
			$V_{CCO} = 1.14V$ to $1.26V$	15.3	41.1	119.4	$k\Omega$
$I_{RPD}^{(3)}$	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	$V_{CCAUX} = 3.0V$ to $3.6V$	167	346	659	μA
			$V_{CCAUX} = 2.25V$ to $2.75V$	100	225	457	μA
$R_{PD}^{(3)}$	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{CCAUX} = 3.0V$ to $3.6V$	$V_{IN} = 3.0V$ to $3.6V$	5.5	10.4	20.8	$k\Omega$
			$V_{IN} = 2.3V$ to $2.7V$	4.1	7.8	15.7	$k\Omega$
			$V_{IN} = 1.7V$ to $1.9V$	3.0	5.7	11.1	$k\Omega$
			$V_{IN} = 1.4V$ to $1.6V$	2.7	5.1	9.6	$k\Omega$
			$V_{IN} = 1.14V$ to $1.26V$	2.4	4.5	8.1	$k\Omega$
		$V_{CCAUX} = 2.25V$ to $2.75V$	$V_{IN} = 3.0V$ to $3.6V$	7.9	16.0	35.0	$k\Omega$
			$V_{IN} = 2.3V$ to $2.7V$	5.9	12.0	26.3	$k\Omega$
			$V_{IN} = 1.7V$ to $1.9V$	4.2	8.5	18.6	$k\Omega$
			$V_{IN} = 1.4V$ to $1.6V$	3.6	7.2	15.7	$k\Omega$
			$V_{IN} = 1.14V$ to $1.26V$	3.0	6.0	12.5	$k\Omega$
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		-10	—	+10	μA
C_{IN}	Input capacitance	—		—	—	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	$V_{CCO} = 3.3V \pm 10\%$	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		$V_{CCO} = 2.5V \pm 10\%$	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	—	Ω

Notes:

- The numbers in this table are based on the conditions set forth in Table 7.
- For single-ended signals that are placed on a differential-capable I/O, V_{IN} of $-0.2V$ to $-0.5V$ is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in [UG331](#), *Spartan-3 Generation FPGA User Guide*.
- This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Differential Output Pairs



$$V_{OCM} = \text{Output common mode voltage} = \frac{V_{OUTP} + V_{OUTN}}{2}$$

$$V_{OD} = \text{Output differential voltage} = |V_{OUTP} - V_{OUTN}|$$

$$V_{OH} = \text{Output voltage indicating a High logic level}$$

$$V_{OL} = \text{Output voltage indicating a Low logic level}$$

DS312-3_03_090510

Figure 4: Differential Output Voltages

Table 13: DC Characteristics of User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	—	1.375	—	—
LVDS_33	247	350	454	1.125	—	1.375	—	—
BLVDS_25	240	350	460	—	1.30	—	—	—
MINI_LVDS_25	300	—	600	1.0	—	1.4	—	—
MINI_LVDS_33	300	—	600	1.0	—	1.4	—	—
RSDS_25	100	—	400	1.0	—	1.4	—	—
RSDS_33	100	—	400	1.0	—	1.4	—	—
TMDS_33	400	—	800	$V_{CCO} - 0.405$	—	$V_{CCO} - 0.190$	—	—
PPDS_25	100	—	400	0.5	0.8	1.4	—	—
PPDS_33	100	—	400	0.5	0.8	1.4	—	—
DIFF_HSTL_I_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_I	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_SSTL18_I	—	—	—	—	—	—	$V_{TT} + 0.475$	$V_{TT} - 0.475$
DIFF_SSTL18_II	—	—	—	—	—	—	$V_{TT} + 0.603$	$V_{TT} - 0.603$
DIFF_SSTL2_I	—	—	—	—	—	—	$V_{TT} + 0.61$	$V_{TT} - 0.61$
DIFF_SSTL2_II	—	—	—	—	—	—	$V_{TT} + 0.81$	$V_{TT} - 0.81$
DIFF_SSTL3_I	—	—	—	—	—	—	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL3_II	—	—	—	—	—	—	$V_{TT} + 0.8$	$V_{TT} - 0.8$

Notes:

- The numbers in this table are based on the conditions set forth in Table 7 and Table 12.
- See "External Termination Requirements for Differential I/O."
- Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100 Ω across the N and P pins of the differential signal pair.
- At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when $V_{CCO}=2.5V$, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when $V_{CCO} = 3.3V$

Table 21: Propagation Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	0	XC3SD1800A	1.79	2.04	ns
				XC3SD3400A	1.65	2.11	ns
T _{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	1	XC3SD1800A	2.23	2.47	ns
			2		2.81	3.06	ns
			3		3.39	3.86	ns
			4		3.89	4.43	ns
			5		3.83	4.39	ns
			6		4.61	5.32	ns
			7		5.40	6.24	ns
			8		5.93	6.86	ns
			1	XC3SD3400A	2.21	2.67	ns
			2		2.71	3.25	ns
			3		3.58	4.04	ns
			4		4.15	4.62	ns
			5		4.03	4.49	ns
			6		4.57	5.31	ns
			7		5.34	6.18	ns
			8		5.84	6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 7](#) and [Table 10](#).
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from [Table 22](#).

Input Timing Adjustments

Table 22: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0.00	0.00	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 22: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

- The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
- These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Timing Adjustments

Table 25: Output Timing Adjustments for IOB

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74 ⁽³⁾	2.74 ⁽³⁾	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 25: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVC MOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55 ⁽³⁾	2.55 ⁽³⁾	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 25: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVC MOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26 ⁽³⁾	2.26 ⁽³⁾	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0.00	0.00	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 25: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVC MOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVC MOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Table 28: Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V)

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Single-Ended Standards				
LVTTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 28: Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) (Cont'd)

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	—	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	—	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	—	10

Table 28: Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) (Cont'd)

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	—	11
		24	—	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	—	3
		24	—	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	—	36
		24	—	8

Table 28: Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) (Cont'd)

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	—	13
		16	—	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	—	4
		16	—	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	—	36
		16	—	24
LVCMOS15	Slow	2	55	55
		4	31	31
		6	18	18
		8	—	15
		12	—	10
	Fast	2	25	25
		4	10	10
		6	6	6
		8	—	4
		12	—	3
	QuietIO	2	70	70
		4	40	40
		6	31	31
		8	—	31
		12	—	20

Clock Buffer/Multiplexer Switching Characteristics

Table 32: Clock Distribution Switching Characteristics

Symbol	Description	Minimum	Maximum		Units
			Speed Grade		
			-5	-4	
T _{GIO}	Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	–	0.22	0.23	ns
T _{GSI}	Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	–	0.56	0.63	ns
F _{BUFG}	Frequency of signals distributed on global buffers (all sides)	0	350	334	MHz

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 7](#).

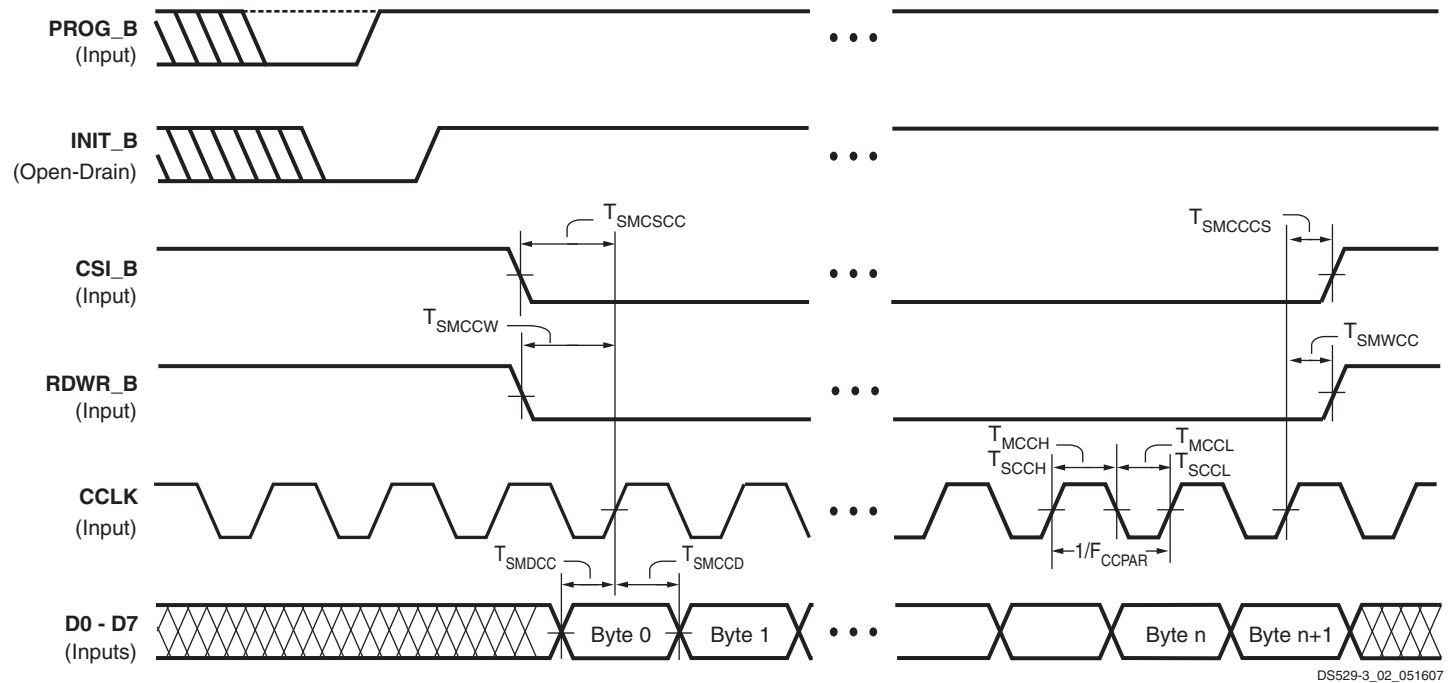
Table 39: Switching Characteristics for the DFS

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_FX ⁽²⁾	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	311	MHz
Output Clock Jitter ⁽³⁾⁽⁴⁾								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN ≤ 20 MHz	All	Typ	Max	Typ	Max	ps
				Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle ⁽⁵⁾⁽⁶⁾								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment ⁽⁶⁾								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps
Lock Time								
LOCK_FX ⁽²⁾⁽³⁾	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F _{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F _{CLKIN} > 15 MHz		–	450	–	450	μs

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 7 and Table 38.
- DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
- For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of “±[1% of CLKFX period + 200]”. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See [UG332](#), Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 12: Waveforms for Slave Parallel Configuration

Table 51: Timing for the Slave Parallel Configuration Mode

Symbol	Description	All Speed Grades		Units	
		Min	Max		
Setup Times					
T _{SMDCC} ⁽²⁾	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	7	—	ns	
T _{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin	7	—	ns	
T _{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin	17	—	ns	
Hold Times					
T _{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	1	—	ns	
T _{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin	0	—	ns	
T _{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin	0	—	ns	
Clock Timing					
T _{CCH}	The High pulse width at the CCLK input pin		5	—	ns
T _{CCL}	The Low pulse width at the CCLK input pin		5	—	ns
F _{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 7](#).
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in [UG331: Spartan-3 Generation FPGA User Guide](#).

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in [Table 57](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: Types of Pins on Spartan-3A DSP FPGAs

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: Spartan-3 Generation Configuration User Guide for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Electronic versions of the package pinout tables and foot-prints are available for download from the Xilinx® website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Package Overview

Table 60 shows the two low-cost, space-saving production package styles for the Spartan-3A DSP family.

Table 60: Spartan-3A DSP Family Package Options

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass ⁽¹⁾ (g)
CS484 / CSG484	484	Chip-Scale Ball Grid Array (CS)	309	0.8	19 x 19	1.80	1.4
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	519	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is $\pm 10\%$.

Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see [UG112: Device Package User Guide](#).

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the [Xilinx web site](#) for each package.

Table 61: Xilinx Package Documentation

Package	Drawing	MDDS
CS484	Package Drawing	PK230_CS484
CSG484		PK231_CSG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

Table 63: Spartan-3A DSP CS484 Pinout (Cont'd)

Bank	Pin Name	CS484 Ball	Type
2	IP_2/VREF_2	Y14	VREF
2	IO_L24N_2/D3	Y15	DUAL
2	IO_L29N_2	Y16	I/O
2	IO_L29P_2	Y17	I/O
2	IO_L26P_2/D2	Y18	DUAL
2	IO_L26N_2/D1	Y19	DUAL
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
2	VCCO_2	V9	VCCO
2	VCCO_2	V14	VCCO
3	IP_L39N_3/VREF_3	AA1	VREF
3	IO_L02N_3	C1	I/O
3	IO_L02P_3	C2	I/O
3	IP_L04P_3	D1	INPUT
3	IP_L08P_3	D3	INPUT
3	IP_L08N_3	D4	INPUT
3	IP_L04N_3/VREF_3	E1	VREF
3	IO_L09P_3	E3	I/O
3	IO_L09N_3	E4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L01P_3	F3	I/O
3	IO_L03P_3	F4	I/O
3	IO_L03N_3	F5	I/O
3	IO_L11P_3	G1	I/O
3	IO_L01N_3	G3	I/O
3	IO_L07P_3	G5	I/O
3	IO_L07N_3	G6	I/O
3	IO_L11N_3	H1	I/O
3	IO_L14P_3	H2	I/O
3	IO_L05P_3	H3	I/O
3	IO_L05N_3	H4	I/O
3	IO_L10P_3	H5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L14N_3/VREF_3	J1	VREF
3	IP_L16P_3	J3	INPUT
3	IP_L16N_3	J4	INPUT
3	IP_L12P_3	J6	INPUT
3	IP_L12N_3/VREF_3	J7	VREF
3	IO_L19P_3/LHCLK2	K1	LHCLK

Table 63: Spartan-3A DSP CS484 Pinout (Cont'd)

Bank	Pin Name	CS484 Ball	Type
3	IO_L17P_3	K2	I/O
3	IO_L17N_3	K3	I/O
3	IO_L13P_3	K4	I/O
3	IO_L13N_3	K5	I/O
3	IO_L15P_3	K6	I/O
3	IO_L19N_3/IRDY2/LHCLK3	L1	LHCLK
3	IO_L20P_3/LHCLK4	L3	LHCLK
3	IO_L15N_3	L5	I/O
3	IO_L18P_3/LHCLK0	L6	LHCLK
3	IO_L22P_3/VREF_3	M1	VREF
3	IO_L20N_3/LHCLK5	M2	LHCLK
3	IP_L23P_3	M3	INPUT
3	IO_L18N_3/LHCLK1	M5	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	M6	LHCLK
3	IO_L22N_3	N1	I/O
3	IP_L31P_3	N3	INPUT
3	IP_L23N_3	N4	INPUT
3	IO_L24N_3	N5	I/O
3	IO_L24P_3	N6	I/O
3	IO_L21N_3/LHCLK7	N7	LHCLK
3	IO_L25P_3	P1	I/O
3	IO_L25N_3	P2	I/O
3	IP_L31N_3	P3	INPUT
3	IO_L32P_3/VREF_3	P4	VREF
3	IO_L26P_3	P6	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	R2	I/O
3	IO_L34P_3	R3	I/O
3	IO_L32N_3	R5	I/O
3	IO_L26N_3	R6	I/O
3	IO_L30P_3	T1	I/O
3	IP_L27P_3	T3	INPUT
3	IO_L34N_3	T4	I/O
3	IO_L29N_3	T5	I/O
3	IO_L29P_3	T6	I/O
3	IO_L30N_3	U1	I/O
3	IO_L33P_3	U2	I/O
3	IP_L27N_3	U3	INPUT
3	IO_L38P_3	U4	I/O
3	IO_L38N_3	U5	I/O
3	IO_L33N_3	V1	I/O
3	IO_L36N_3	V3	I/O

Table 66: Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA (Cont'd)

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO

Table 66: Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA (Cont'd)

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O

Bank 0																	Bank 1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
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Right Half of FG676
Package (Top View)

Figure 17: FG676 Package Footprint for XC3SD1800A FPGA (Top View–Right Half)

User I/Os by Bank

Table 69 indicates how the available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 69: User I/Os Per Bank for the XC3SD3400A in the FG676 Package

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK
Top	0	111	82	11	1	9	8
Right	1	123	67	8	30	10	8
Bottom	2	112	68	6	21	9	8
Left	3	123	97	9	0	9	8
TOTAL		469	314	34	52	37	32

Notes:

1. 26 VREF are on INPUT pins.