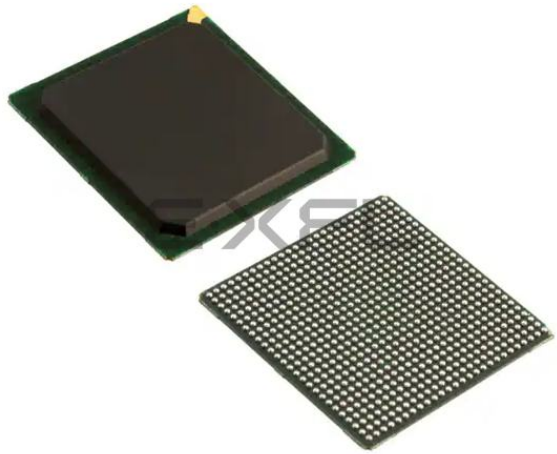

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Details	
Product Status	Active
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	469
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3sd3400a-5fgg676c

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 3: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 3: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

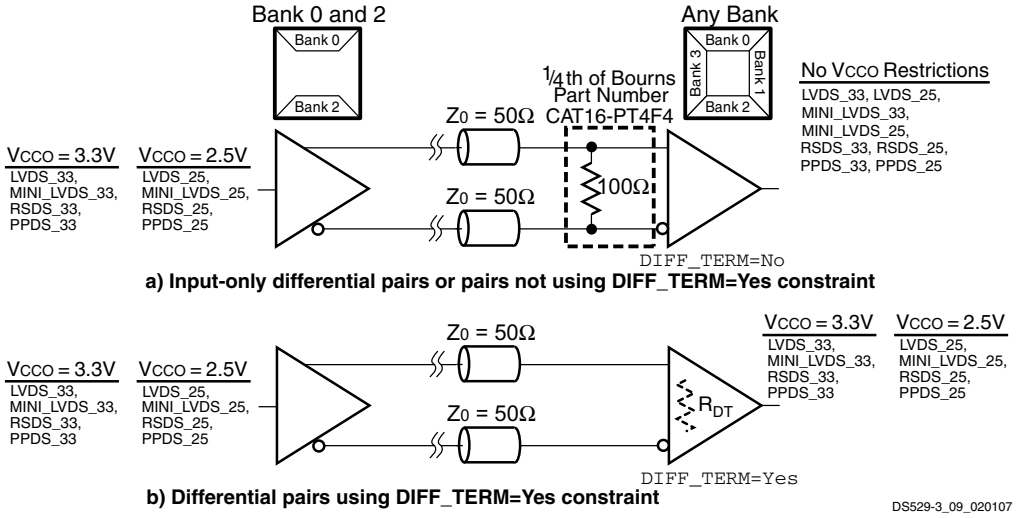

Figure 5: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

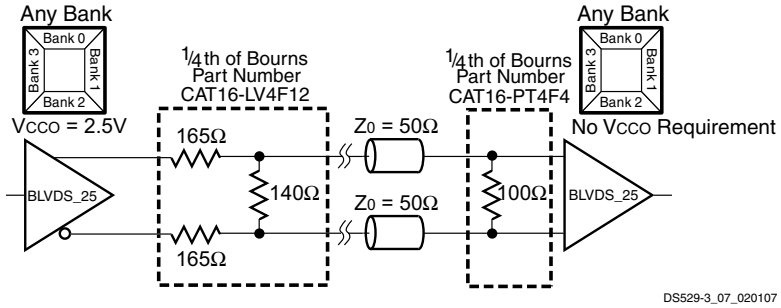

Figure 6: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

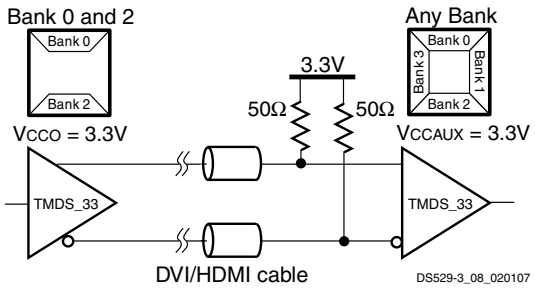

Figure 7: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 14: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A DSP FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 15. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs will require updating the Xilinx ISE development software with a future version and/or Service Pack.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 15. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 15: **Spartan-3A DSP v1.32 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3SD1800A			-4, -5
XC3SD3400A			-4, -5

Table 16 provides the recent history of the Spartan-3A DSP FPGA speed files.

Table 16: **Spartan-3A DSP Speed File Version History**

Version	ISE Release	Description
1.32	ISE 10.1.02	Updated DSP timing model to reflect higher performance for some implementations
1.31	ISE 10.1	Added Automotive support
1.30	ISE 9.2.03i	Added absolute minimum values
1.29	ISE 9.2.01i	Production Speed Files for -4 and -5 speed grades
1.28	ISE 9.2i	Minor updates
1.27	ISE 9.1.03i	Advance Speed Files for -4 speed grade

Output Propagation Times

Table 23: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON} (2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON} (2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

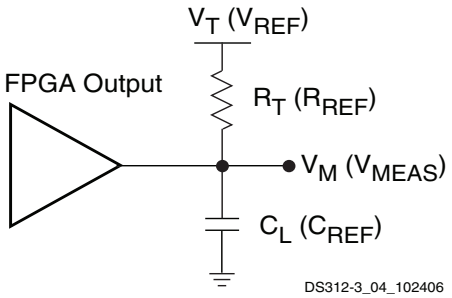
1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 8. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 8: **Output Test Setup**

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs[2]		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 26 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 8. Use parameter values V_T, R_T, and V_M from Table 26. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 25) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 27 and Table 28 provide the essential SSO guidelines. For each device/package combination, Table 27 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 28 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 28 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 27 and Table 28 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 27 x Table 28

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

Table 27: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*	
	CS484	FG676
XC3SD1800A	6	9
XC3SD3400A	6	10

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V)**

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Block RAM Timing

Table 33: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
$T_{RCKO\_DOA\_NC}$	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.38	–	2.80	ns
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)	–	1.24	–	1.45	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.40	–	0.46	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.29	–	0.33	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.51	–	0.60	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	0.64	–	0.75	–	ns
T_{RCCK_REGCE}	Setup time for the CE input before the active transition at the CLK input of the block RAM	0.34	–	0.40	–	ns
T_{RCCK_RST}	Setup time for the RST input before the active transition at the CLK input of the block RAM	0.22	–	0.25	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_REGCE}	Hold time on the CE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_RST}	Hold time on the RST input after the active transition at the CLK input	0.09	–	0.10	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 37: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

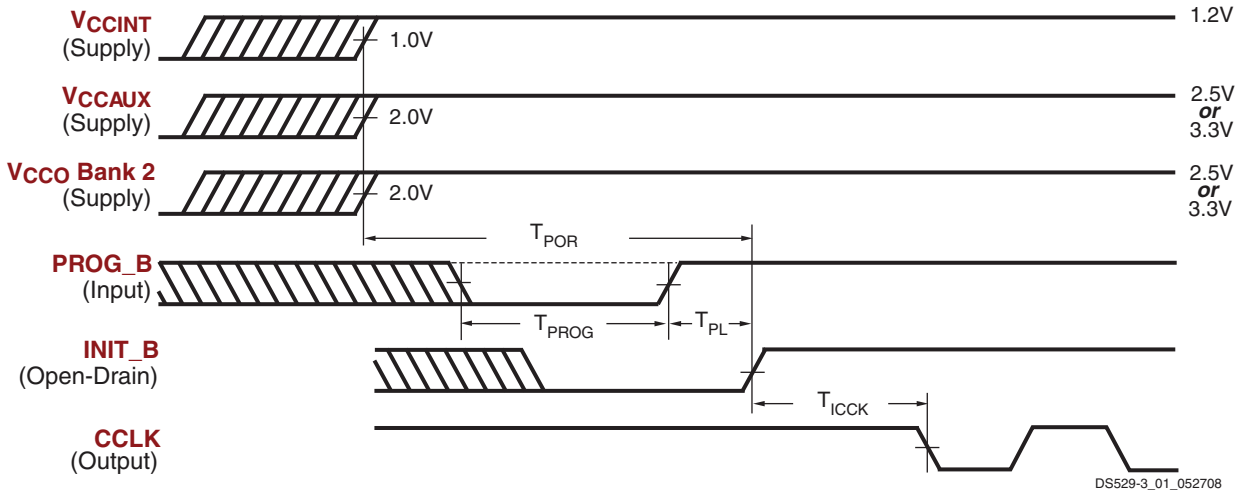
Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.2	333(5)	0.2	333(5)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.
5. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL} T_{SCCH}	CCLK Low and High time	5	∞	ns

Electronic versions of the package pinout tables and foot- prints are available for download from the Xilinx® website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Package Overview

Table 60 shows the two low-cost, space-saving production package styles for the Spartan-3A DSP family.

Table 60: **Spartan-3A DSP Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass(1) (g)
CS484 / CSG484	484	Chip-Scale Ball Grid Array (CS)	309	0.8	19 x 19	1.80	1.4
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	519	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
CS484	Package Drawing	PK230_CS484
CSG484		PK231_CSG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L19P_0/GCLK8	F10	GCLK
0	IO_L17N_0/GCLK5	F11	GCLK
0	IP_0	F12	INPUT
0	IO_L13N_0	F13	I/O
0	IO_L13P_0	F14	I/O
0	IO_L05N_0	F15	I/O
0	IO_L04N_0	F16	I/O
0	IO_L23P_0	G8	I/O
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E9	VCCO
0	VCCO_0	E14	VCCO
1	IO_L02N_1/LDC0	AA22	DUAL
1	IP_L39N_1	C21	INPUT
1	IP_L39P_1/VREF_1	C22	VREF
1	IO_L36P_1/A20	D20	DUAL
1	IO_L37P_1/A22	D21	DUAL
1	IO_L37N_1/A23	D22	DUAL
1	IO_L36N_1/A21	E19	DUAL
1	IO_L35N_1	E20	I/O
1	IO_L33N_1	E22	I/O
1	IO_L38N_1/A25	F18	DUAL
1	IO_L38P_1/A24	F19	DUAL
1	IO_L30N_1/A19	F20	DUAL
1	IO_L35P_1	F21	I/O
1	IO_L33P_1	F22	I/O
1	IO_L34P_1	G17	I/O
1	IO_L34N_1	G18	I/O
1	IO_L30P_1/A18	G19	DUAL
1	IP_L31N_1	G20	INPUT
1	IO_L28N_1	G22	I/O
1	IO_L26P_1/A14	H17	DUAL
1	IO_L26N_1/A15	H18	DUAL
1	IO_L32N_1	H20	I/O
1	IP_L31P_1/VREF_1	H21	VREF
1	IO_L28P_1	H22	I/O
1	IO_L29N_1/A17	J17	DUAL
1	IO_L32P_1	J19	I/O
1	IO_L25N_1/A13	J20	DUAL
1	IP_L27P_1	J21	INPUT

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IP_L27N_1	J22	INPUT
1	IO_L29P_1/A16	K16	DUAL
1	IP_L23N_1	K17	INPUT
1	IO_L24N_1	K18	I/O
1	IO_L24P_1	K19	I/O
1	IO_L25P_1/A12	K20	DUAL
1	IO_L22N_1/A11	K22	DUAL
1	IO_L21N_1/RHCLK7	L17	RHCLK
1	IP_L23P_1/VREF_1	L18	VREF
1	IO_L20N_1/RHCLK5	L20	RHCLK
1	IO_L20P_1/RHCLK4	L21	RHCLK
1	IO_L22P_1/A10	L22	DUAL
1	IO_L18N_1/RHCLK1	M17	RHCLK
1	IO_L21P_1/IRDY1/RHCLK6	M18	RHCLK
1	IO_L19N_1/TRDY1/RHCLK3	M20	RHCLK
1	IO_L17N_1/A9	M22	DUAL
1	IO_L13P_1/A2	N17	DUAL
1	IO_L18P_1/RHCLK0	N18	RHCLK
1	IO_L15N_1/A7	N19	DUAL
1	IO_L15P_1/A6	N20	DUAL
1	IO_L19P_1/RHCLK2	N21	RHCLK
1	IO_L17P_1/A8	N22	DUAL
1	IO_L13N_1/A3	P16	DUAL
1	IP_L12N_1/VREF_1	P17	VREF
1	IO_L10P_1	P19	I/O
1	IP_L16N_1	P20	INPUT
1	IO_L14N_1/A5	P22	DUAL
1	IP_L12P_1	R17	INPUT
1	IO_L10N_1	R18	I/O
1	IO_L07P_1	R19	I/O
1	IO_L07N_1	R20	I/O
1	IP_L16P_1/VREF_1	R21	VREF
1	IO_L14P_1/A4	R22	DUAL
1	IO_L05N_1	T17	I/O
1	IO_L05P_1	T18	I/O
1	IO_L09N_1	T20	I/O
1	IO_L11N_1/VREF_1	T22	VREF
1	IO_L01P_1/HDC	U18	DUAL
1	IO_L01N_1/LDC2	U19	DUAL
1	IO_L09P_1	U20	I/O
1	IP_L08N_1/VREF_1	U21	VREF
1	IO_L11P_1	U22	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
3	IO_L36P_3	V4	I/O
3	IO_L35N_3	W1	I/O
3	IO_L37N_3	W2	I/O
3	IO_L37P_3	W3	I/O
3	IO_L35P_3	Y1	I/O
3	IP_L39P_3	Y2	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J5	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA7	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B7	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND
GND	GND	D8	GND
GND	GND	D11	GND
GND	GND	D16	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G4	GND
GND	GND	G9	GND
GND	GND	G11	GND
GND	GND	G13	GND
GND	GND	G15	GND
GND	GND	G21	GND
GND	GND	H7	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	H12	GND
GND	GND	H14	GND
GND	GND	H16	GND

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	H19	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J15	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K14	GND
GND	GND	L2	GND
GND	GND	L7	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L19	GND
GND	GND	M4	GND
GND	GND	M8	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	M21	GND
GND	GND	N9	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	N15	GND
GND	GND	P8	GND
GND	GND	P10	GND
GND	GND	P12	GND
GND	GND	P14	GND
GND	GND	R4	GND
GND	GND	R7	GND
GND	GND	R9	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	R16	GND
GND	GND	T2	GND
GND	GND	T8	GND
GND	GND	T10	GND
GND	GND	T12	GND

Right Half of CS484 Package (Top View)

Figure 16: CS484 Package Footprint (Top View–Right Half)

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_3/VREF_3	C1	VREF
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_3/VREF_3	AA5	VREF
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	C2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	W25	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	U25	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND

Right Half of FG676 Package (Top View)

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Right Half)**

Footprint Migration Differences

There are multiple migration footprint differences between the XC3SD1800A and the XC3SD3400A in the FG676 package. These migration footprint differences are shown in Table 70. Migration from the XC3S1400A Spartan-3A device in the FG676 package to a Spartan-3A DSP device in the FG676 package is also possible. The XC3S1800A pin migration differences have been added to Table 70 for designs migrating between these devices.

Table 70: **FG676 Footprint Migration Differences**

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
G16	IP_0	0	IP_0	0	GND	GND	G16
G18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	G18
F9	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	F9
F10	IP_0	0	IP_0	0	VCCINT	VCCINT	F10
F18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	F18
E6	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	E6
E9	N.C.	N.C.	IP_0	0	GND	GND	E9
E20	IP_0	0	IP_0	0	VCCAUX	VCCAUX	E20
D5	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	D5
D15	IP_0	0	IP_0	0	GND	GND	D15
D19	IP_0	0	IP_0	0	GND	GND	D19
C4	IP_0	0	IP_0	0	VCCINT	VCCINT	C4
B24	N.C.	N.C.	IP_0	0	GND	GND	B24
A5	IP_0	0	IP_0	0	GND	GND	A5
A7	IP_0	0	IP_0	0	VCCO_0	0	A7
A23	IP_0	0	IP_0	0	GND	GND	A23
A24	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	A24
Y26	IP_L16N_1	1	IP_L16N_1	1	IP_1	1	Y26
W25	IP_L16P_1	1	IP_L16P_1	1	GND	GND	W25
W26	IP_L20P_1	1	IP_L20P_1	1	VCCAUX	VCCAUX	W26
V26	IP_L20N_1/ VREF_1	1	IP_L20N_1/ VREF_1	1	IP_1/VREF_1	1	V26
U25	IP_L24P_1	1	IP_L24P_1	1	GND	GND	U25
U26	IP_L24N_1/ VREF_1	1	IP_L24N_1/ VREF_1	1	IP_1/VREF_1	1	U26
H23	IP_L48P_1	1	IP_L48P_1	1	VCCAUX	VCCAUX	H23
H24	IP_L48N_1	1	IP_L48N_1	1	IP_1	1	H24
H25	IP_L44N_1	1	IP_L44N_1	1	VCCO_1	1	H25
H26	IP_L44P_1/ VREF_1	1	IP_L44P_1/ VREF_1	1	IP_1/VREF_1	1	H26
G25	IP_L52N_1/ VREF_1	1	IP_L52N_1/ VREF_1	1	IP_1/VREF_1	1	G25
G26	IP_L52P_1	1	IP_L52P_1	1	VCCAUX	VCCAUX	G26
B25	IP_L65N_1	1	IP_L65N_1	1	GND	GND	B25
B26	IP_L65P_1/ VREF_1	1	IP_L65P_1/ VREF_1	1	IP_1/VREF_1	1	B26

Table 70: **FG676 Footprint Migration Differences *(Cont'd)***

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
Y8	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	Y8
Y11	IP_2	2	IP_2	2	VCCINT	VCCINT	Y11
Y18	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	Y18
Y19	N.C.	N.C.	IP_2/VREF_2	2	VCCINT	VCCINT	Y19
W18	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	W18
AF2	IP_2	2	IP_2	2	VCCAUX	VCCAUX	AF2
AF7	IP_2	2	IP_2	2	VCCO_2	2	AF7
AD5	N.C.	N.C.	IP_2	2	GND	GND	AD5
AD23	N.C.	N.C.	IP_2	2	GND	GND	AD23
AC5	N.C.	N.C.	IP_2	2	GND	GND	AC5
AC7	IP_2	2	IP_2	2	GND	GND	AC7
AC18	IP_2	2	IP_2	2	GND	GND	AC18
AB10	IP_2/VREF_2	2	IP_2/VREF_2	2	GND	GND	AB10
AB17	IP_2	2	IP_2	2	VCCAUX	VCCAUX	AB17
AB20	IP_2	2	IP_2	2	GND	GND	AB20
AA8	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	AA8
AA19	IP_2	2	IP_2	2	GND	GND	AA19
AC22	N.C.	N.C.	IO_2	2	IO_2	2	AC22
Y3	IP_L54P_3	3	IP_L54P_3	3	IP_3	3	Y3
Y4	IP_L54N_3	3	IP_L54N_3	3	VCCINT	VCCINT	Y4
H4	IP_L12N_3/ VREF_3	3	IP_L12N_3/ VREF_3	3	IP_3/VREF_3	3	H4
G1	IP_L16N_3	3	IP_L16N_3	3	IP_3	3	G1
G2	IP_L16P_3	3	IP_L16P_3	3	GND	GND	G2
G5	IP_L12P_3	3	IP_L12P_3	3	GND	GND	G5
D1	IP_L08N_3	3	IP_L08N_3	3	VCCAUX	VCCAUX	D1
D2	IP_L08P_3	3	IP_L08P_3	3	GND	GND	D2
C1	IP_L04N_3/ VREF_3	3	IP_L04N_3/ VREF_3	3	IP_3/VREF_3	3	C1
C2	IP_L04P_3	3	IP_L04P_3	3	VCCO_3	3	C2
AB3	IP_L62P_3	3	IP_L62P_3	3	GND	GND	AB3
AB4	IP_L62N_3	3	IP_L62N_3	3	VCCAUX	VCCAUX	AB4
AA4	IP_L58P_3	3	IP_L58P_3	3	GND	GND	AA4
AA5	IP_L58N_3/ VREF_3	3	IP_L58N_3/ VREF_3	3	IP_3/VREF_3	3	AA5

Migration Recommendations

There are multiple pinout differences between the XC3SD1800A and the XC3SD3400A FPGAs in the FG676 package. Please note the differences between the two devices from Table 70 and take the necessary precautions.