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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K × 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f458-i-p

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4.10 Access Bank

The Access Bank is an architectural enhancement that is very useful for C compiler code optimization. The techniques used by the C compiler are also useful for programs written in assembly.

This data memory region can be used for:

- · Intermediate computational values
- · Local variables of subroutines
- · Faster context saving/switching of variables
- · Common variables
- Faster evaluation/control of SFRs (no banking)

The Access Bank is comprised of the upper 160 bytes in Bank 15 (SFRs) and the lower 96 bytes in Bank 0. These two sections will be referred to as Access Bank High and Access Bank Low, respectively. Figure 4-6 indicates the Access Bank areas.

A bit in the instruction word specifies if the operation is to occur in the bank specified by the BSR register or in the Access Bank.

When forced in the Access Bank (a = 0), the last address in Access Bank Low is followed by the first address in Access Bank High. Access Bank High maps most of the Special Function Registers so that these registers can be accessed without any software overhead.

4.11 Bank Select Register (BSR)

The need for a large general purpose memory space dictates a RAM banking scheme. The data memory is partitioned into sixteen banks. When using direct addressing, the BSR should be configured for the desired bank.

BSR<3:0> holds the upper 4 bits of the 12-bit RAM address. The BSR<7:4> bits will always read '0's and writes will have no effect.

A MOVLB instruction has been provided in the instruction set to assist in selecting banks.

If the currently selected bank is not implemented, any read will return all '0's and all writes are ignored. The Status register bits will be set/cleared as appropriate for the instruction performed.

Each Bank extends up to FFh (256 bytes). All data memory is implemented as static RAM.

A MOVFF instruction ignores the BSR since the 12-bit addresses are embedded into the instruction word.

Section 4.12 "Indirect Addressing, INDF and FSR Registers" provides a description of indirect addressing, which allows linear addressing of the entire RAM space.



FIGURE 4-7: DIRECT ADDRESSING

9.5 PORTE, TRISE and LATE Registers

Note:	This	port	is	only	available	on	the
	PIC18	3F448	and	PIC1	8F458.		

PORTE is a 3-bit wide, bidirectional port. PORTE has three pins (RE0/AN5/RD, RE1/AN6/WR/C10UT and RE2/AN7/CS/C20UT) which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

Read-modify-write operations on the LATE register, read and write the latched output value for PORTE.

The corresponding Data Direction register for the port is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

The TRISE register also controls the operation of the Parallel Slave Port through the control bits in the upper half of the register. These are shown in Register 9-1.

When the Parallel Slave Port is active, the PORTE pins function as its control inputs. For additional details, refer to **Section 10.0 "Parallel Slave Port**".

PORTE pins are also multiplexed with inputs for the A/D converter and outputs for the analog comparators. When selected as an analog input, these pins will read as '0's. Direction bits TRISE<2:0> control the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

EXAMP	PLE 9-5:	INITIALIZING PORTE
CLRF	PORTE	; Initialize PORTE by
		; clearing output
		; data latches
CLRF	LATE	; Alternate method
		; to clear output
		; data latches
MOVLW	03h	; Value used to
		; initialize data
		; direction
MOVWF	TRISE	; Set RE1:RE0 as inputs
		; RE2 as an output
		; (RE4=0 - PSPMODE Off)



FIGURE 9-10: PORTE BLOCK DIAGRAM

Name	Bit#	Buffer Type	Function
RE0/AN5/RD	bit 0	ST/TTL ⁽¹⁾	Input/output port pin, analog input or read control input in Parallel Slave Port mode.
RE1/AN6/WR/C1OUT	bit 1	ST/TTL ⁽¹⁾	Input/output port pin, analog input, write control input in Parallel Slave Port mode or Comparator 1 output.
RE2/AN7/CS/C2OUT	bit 2	ST/TTL ⁽¹⁾	Input/output port pin, analog input, chip select control input in Parallel Slave Port mode or Comparator 2 output.

TABLE 9-9: PORTE FUNCTIONS

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 9-10:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TRISE	IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
PORTE	—	—	_	—	—	Read POF Write POF	RTE pin/ RTE Data L	atch	xxx	uuu
LATE	—	—		—	—	Read POF Write POF	RTE Data L RTE Data L	atch/ atch	xxx	uuu
ADCON1	ADFM	ADCS2	_	—	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

14.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers: TMR3H and TMR3L)
- Readable and writable (both registers)
- · Internal or external clock select
- Interrupt-on-overflow from FFFFh to 0000h
- Reset from CCP1/ECCP1 module trigger

Figure 14-1 is a simplified block diagram of the Timer3 module.

Register 14-1 shows the Timer3 Control register. This register controls the operating mode of the Timer3 module and sets the CCP1 and ECCP1 clock source.

Register 12-1 shows the Timer1 Control register. This register controls the operating mode of the Timer1 module, as well as contains the Timer1 Oscillator Enable bit (T1OSCEN) which can be a clock source for Timer3.

Timer3 is disabled on POR. Note:

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3ECCP1	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

bit 7	RD16: 16-bit Read/Write 1 = Enables register read 0 = Enables register read	Mode Enable bit I/write of Timer3 in or I/write of Timer3 in tw	ne 16-bit operation vo 8-bit operations	
bit 6,3	T3ECCP1:T3CCP1: Time 1x = Timer3 is the clock = 01 = Timer3 is the clock = Timer1 is the clock = 00 = Timer1 is the clock =	er3 and Timer1 to CC source for compare/c source for compare/c source for compare/c source for compare/c	P1/ECCP1 Enable bits apture CCP1 and ECCF apture of ECCP1, apture of CCP1 apture CCP1 and ECCF	P1 modules
bit 5-4	T3CKPS1:T3CKPS0 : Tir 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value	ner3 Input Clock Pres	scale Select bits	
bit 2	T3SYNC: Timer3 Externa(Not usable if the systemWhen TMR3CS = 1:1 = Do not synchronize e0 = Synchronize externalWhen TMR3CS = 0:This bit is ignored. Timera	al Clock Input Synchr clock comes from Til xternal clock input clock input 3 uses the internal clo	onization Control bit mer1/Timer3.) ock when TMR3CS = 0.	
bit 1	TMR3CS: Timer3 Clock 3 1 = External clock input fro 0 = Internal clock (Fosc/-	Source Select bit m Timer1 oscillator or 4)	T1CKI (on the rising edge	after the first falling edge)
bit 0	TMR3ON: Timer3 On bit 1 = Enables Timer3 0 = Stops Timer3			
	Legend:			
	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
	-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown





16.5.3.1 Direction Change in Full-Bridge Mode

In the Full-Bridge Output mode, the EPWM1M1 bit in the ECCP1CON register allows the user to control the forward/reverse direction. When the application firmware changes this direction control bit, the ECCP1 module will assume the new direction on the next PWM cycle. The current PWM cycle still continues, however, the non-modulated outputs, P1A and P1C signals, will transition to the new direction Tosc, 4 Tosc or 16 Tosc earlier (for T2CKRS<1:0> = 00, 01 or 1x, respectively) before the end of the period. During this transition cycle, the modulated outputs, P1B and P1D, will go to the inactive state (Figure 16-7).

Note that in the Full-Bridge Output mode, the ECCP module does not provide any dead-band delay. In general, since only one output is modulated at all times, dead-band delay is not required. However, there is a situation where a dead-band delay might be required. This situation occurs when all of the following conditions are true:

- 1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- 2. The turn-off time of the power switch, including the power device and driver circuit, is greater than turn-on time.

Figure 16-8 shows an example where the PWM direction changes from forward to reverse at a near 100% duty cycle. At time t1, the outputs P1A and P1D become inactive, while output P1C becomes active. In this example, since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current flows through power devices QB and QD (see Figure 16-6) for the duration of 't'. The same phenomenon will occur to power devices QA and QC for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, one of the following requirements must be met:

- 1. Avoid changing PWM output direction at or near 100% duty cycle.
- 2. Use switch drivers that compensate the slow turn off of the power devices. The total turn-off time (t_{off}) of the power device and the driver must be less than the turn-on time (t_{on}) .

17.4.3.2 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and the SDA line is held low (ACK).

When the address byte overflow condition exists, then the no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON1<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPCON2<0> = 1), RC3/SCK/SCL will be held low (clock stretch) following each data transfer. The clock must be released by setting bit CKP (SSPCON1<4>). See **Section 17.4.4** "**Clock Stretching**" for more detail.

17.4.3.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and pin RC3/SCK/SCL is held low regardless of SEN (see Section 17.4.4 "Clock Stretching" for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then, pin RC3/ SCK/SCL should be enabled by setting bit CKP (SSPCON1<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 17-9).

The \overline{ACK} pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not \overline{ACK}), then the data transfer is complete. In this case, when the \overline{ACK} is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDA line was low (\overline{ACK}), the next transmit data must be loaded into the SSPBUF register. Again, pin RC3/SCK/SCL must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.



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IADEL	- 10 4.	DAGE						(Biiaii	- •)			
BAUD	Fosc =	40 MHz	SPBRG	33	MHz	SPBRG	25	MHz	SPBRG	20	ИНz	SPBRG
(Kbps)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	2.40	-0.07	214	2.40	-0.15	162	2.40	+0.16	129
9.6	9.62	+0.16	64	9.55	-0.54	53	9.53	-0.76	40	9.47	-1.36	32
19.2	18.94	-1.36	32	19.10	-0.54	26	19.53	+1.73	19	19.53	+1.73	15
76.8	78.13	+1.73	7	73.66	-4.09	6	78.13	+1.73	4	78.13	+1.73	3
96	89.29	-6.99	6	103.13	+7.42	4	97.66	+1.73	3	104.17	+8.51	2
300	312.50	+4.17	1	257.81	-14.06	1	NA	-	-	312.50	+4.17	0
500	625	+25.00	0	NA	-	-	NA	-	-	NA	-	-
HIGH	625	-	0	515.63	-	0	390.63	-	0	312.50	-	0
LOW	2.44	-	255	2.01	-	255	1.53	-	255	1.22	-	255
BAUD	Fosc =	16 MHz	SPBRG	10	MHz	SPBRG	7.1590	09 MHz	SPBRG	5.068	B MHz	SPBRG
RATE		%	value		%	value		%	value		%	value
(Kbps)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.20	+0.16	207	1.20	+0.16	129	1.20	+0.23	92	1.20	0	65
2.4	2.40	+0.16	103	2.40	+0.16	64	2.38	-0.83	46	2.40	0	32
9.6	9.62	+0.16	25	9.77	+1.73	15	9.32	-2.90	11	9.90	+3.13	7
19.2	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5	19.80	+3.13	3
76.8	83.33	+8.51	2	78.13	+1.73	1	111.86	+45.65	0	79.20	+3.13	0
96	83.33	-13.19	2	78.13	-18.62	1	NA	-	-	NA	-	-
300	250	-16.67	0	156.25	-47.92	0	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	250	-	0	156.25	-	0	111.86	-	0	79.20	-	0
LOW	0.98	-	255	0.61	-	255	0.44	-	255	0.31	-	255
BAUD	Fosc	= 4 MHz	CDBDC	3.5795	545 MHz	CDBDC	1	MHz	CDDDC	32.76	8 kHz	CDDDC
RATE		0/	value		0/	value		0/	value		9/	value
(Kbps)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)	KBAUD	ERROR	(decimal)
0.3	0.30	-0.16	207	0.30	+0.23	185	0.30	+0.16	51	0.26	-14.67	1
1.2	1.20	+1.67	51	1.19	-0.83	46	1.20	+0.16	12	NA	-	-
2.4	2.40	+1.67	25	2.43	+1.32	22	2.23	-6.99	6	NA	-	-
9.6	8.93	-6.99	6	9.32	-2.90	5	7.81	-18.62	1	NA	-	-
19.2	20.83	+8.51	2	18.64	-2.90	2	15.63	-18.62	0	NA	-	-
76.8	62.50	-18.62	0	55.93	-27.17	0	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-

0

255

15.63

0.06

-

-

-

-

0

255

0.51

0.002

BAUD BATES FOR ASYNCHRONOUS MODE (BRGH = 0) TABLE 18-4:

0

255

55.93

0.22

-

-

HIGH

LOW

62.50

0.24

0

255

_

TADLE 10-10. THE MISTERIS ASSOCIATED WITH STRUCTUOUS SEAVE TRANSMISSION	TABLE 18-10:	REGISTERS	ASSOCIATED	WITH SYNC	CHRONOUS	SLAVE 1	RANSMISSION
---	--------------	-----------	------------	-----------	----------	---------	-------------

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	1111 1111	1111 1111
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000u
TXREG	USART Trai	nsmit Registe	er						0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate 0	Generator Re	gister						0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: These registers or register bits are not implemented on the PIC18F248 and PIC18F258 and read as '0's.

TABLE 18-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	1111 1111	1111 1111
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000u
RCREG	USART Receive Register									0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	Generator Re		0000 0000	0000 0000					

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception.

Note 1: These registers or register bits are not implemented on the PIC18F248 and PIC18F258 and read as '0's.

19.2.3 CAN RECEIVE BUFFER REGISTERS

This section shows the Receive Buffer registers with their associated control registers.

REGISTER 19-12:	RXB0CON: RECEIVE BUFFER 0 CONTROL REGISTER										
	R/C-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R-0	R-0			
	RXFUL ⁽¹⁾	RXM1 ⁽¹⁾	RXM0 ⁽¹⁾	—	RXRTRRO	RXB0DBEN	JTOFF	FILHIT0			
	bit 7 bit 0										
bit 7	RXFUL: Re	eceive Full	Status bit ⁽¹⁾								
	1 = Receiv 0 = Receiv	e buffer con e buffer is d	ntains a rece open to rece	eived mess eive a new r	age nessage						
	Note:	This bit is is read.	set by the C	AN module	and must be	cleared by so	ftware afte	r the buffer			
bit 6-5	RXM1:RXM	MO: Receive	e Buffer Mo	de bits ⁽¹⁾							
	 11 = Receive all messages (including those with errors) 10 = Receive only valid messages with extended identifier 01 = Receive only valid messages with standard identifier 00 = Receive all valid messages 										
bit 4	Unimplem	ented: Rea	ad as '0'								
bit 3	RXRTRRO	: Receive I	Remote Trai	nsfer Reque	est Read-Only	y bit					
	1 = Remote 0 = No rem	e transfer re note transfe	equest r request								
bit 2	RXB0DBE	N: Receive	Buffer 0 Do	ouble-Buffer	Enable bit						
	1 = Receiv 0 = No Rec	e Buffer 0 o ceive Buffer	overflow will 0 overflow	write to Re to Receive	ceive Buffer ⁻ Buffer 1	1					
bit 1	JTOFF: Ju	mp Table C	Offset bit (rea	ad-only cop	y of RXB0DB	EN)					
	1 = Allows 0 = Allows	jump table jump table	offset betwe offset betwe	een 6 and 7 een 1 and 0							
	Note:	This bit all	ows same f	ilter jump ta	ble for both F	XB0CON and	RXB1CO	Ν.			
bit 0	FILHITO: F	ilter Hit bit									
	This bit indicates which acceptance filter enabled the message reception into Receive Buffer 0. 1 = Acceptance Filter 1 (RXF1) 0 = Acceptance Filter 0 (RXF0)										
	Note 1:	Bits RXFU	IL, RXM1 ar	nd RXM0 of	RXB0CON a	are not mirrore	d in RXB10	CON.			
	Legend:										

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

PIC18FXX8

REGISTER 19-23: RXFnEIDH: RECEIVE ACCEPTANCE FILTER n EXTENDED IDENTIFIER, HIGH BYTE REGISTERS

	R/W-x							
	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bi	t 7							bit 0

bit 7-0

EID15:EID8: Extended Identifier Filter bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 19-24: RXFnEIDL: RECEIVE ACCEPTANCE FILTER n EXTENDED IDENTIFIER, LOW BYTE REGISTERS

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 EID7:EID0: Extended Identifier Filter bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 19-25: RXMnSIDH: RECEIVE ACCEPTANCE MASK n STANDARD IDENTIFIER MASK, HIGH BYTE REGISTERS

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 SID10:SID3: Standard Identifier Mask bits or Extended Identifier Mask bits EID28:EID21

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

22.0 COMPARATOR VOLTAGE REFERENCE MODULE

Note:	The compa	arator	r voltage reference is only				
	available	on	the	PIC18F448	and		
	PIC18F45	8.					

This module is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The CVRCON register controls the operation of the reference, as shown in Register 22-1. The block diagram is shown in Figure 22-1.

The comparator and reference supply voltage can come from either VDD and Vss, or the external VREF+ and VREF-, that are multiplexed with RA3 and RA2. The comparator reference supply voltage is controlled by the CVRSS bit.

22.1 Configuring the Comparator Voltage Reference

The comparator voltage reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the comparator voltage reference are as follows.

EQUATION 22-1:

If CVRR = 1: $CVREF = (CVR < 3:0 > /24) \times CVRSRC$ where: CVRSS = 1, CVRSRC = (VREF+) - (VREF-)CVRSS = 0, CVRSRC = AVDD - AVSS

EQUATION 22-2:

If CVRR = 0: $CVREF = (CVRSRC \times 1/4) + (CVR < 3:0 > /32) \times CVRSRC$ where: CVRSS = 1, CVRSRC = (VREF+) - (VREF-)CVRSS = 0, CVRSRC = AVDD - AVSS

The settling time of the Comparator Voltage Reference must be considered when changing the RA0/AN0/ CVREF output (see Table 27-4 in **Section 27.2** "**DC Characteristics**").

REGISTER 22-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0			
	bit 7							bit 0			
bit 7	CVREN: C	omparator V	oltage Refe	erence Enab	le bit						
	1 = CVREF	circuit powe	red on								
	0 = CVREF	circuit powe	red down								
bit 6	CVROE: C	omparator \	REF Output	Enable bit							
	1 = CVREF 0 = CVREF	voltage leve voltage is d	l is also out	put on the F	A0/AN0/CV A0/AN0/CVF	REF pin REF pin					
bit 5	CVRR: Comparator VREF Range Selection bit										
	1 = 0.00 C	VRSRC to 0.6	25 CVRSRC	with CVRSF	RC/24 step si	ze					
	0 = 0.25 C	VRSRC to 0.7	19 CVRSRC	with CVRSF	RC/32 step si	ze					
bit 4	CVRSS: C	omparator V	REF Source	Selection b	it						
	1 = Compa 0 = Compa	rator referen rator referen	nce source, nce source,	CVRSRC = (CVRSRC = \	VREF+) – (VI /DD – VSS	REF-)					
bit 3-0	CVR<3:0>	: Comparato	or VREF Valu	e Selection	$0 \le CVR3:C$	VR0 ≤ 15 b	its				
	<u>When CVF</u> CVREF = (0	<u>R = 1:</u> 20083:CVR0	/24) • (CVR:	SRC)							
	When CVF	R = 0:	, . ,								
	CVREF = 1/	4 • (CVRSR	c) + (CVR3:	CVR0/32) •	(CVRSRC)						
	Legend:										
	R = Reada	ble bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'			
	-n = Value	at POR	'1' = Bi	it is set	'0' = Bit is	scleared	x = Bit is u	nknown			

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					•			,			
	U-0	U-0	U-0	U-0	R/C-1	R/C-1	R/C-1	R/C-1			
	—	—	_	—	CP3 ⁽¹⁾	CP2 ⁽¹⁾	CP1	CP0			
	bit 7							bit 0			
bit 7-4 bit 3	Unimpleme CP3: Code 1 = Block 3	nted: Read Protection b (006000-00	as '0' it (1) 7FFFh) not c	code-protecte	ed						
bit 2	0 = Block 3 (006000-007FFFh) code-protected CP2: Code Protection bit ⁽¹⁾										
	1 = Block 2 0 = Block 2	(004000-00) (004000-00)	5FFFh) not c 5FFFh) code	code-protecte e-protected	ed						
bit 1	CP1: Code 1 = Block 1 0 = Block 1	Protection b (002000-003 (002000-003	it 3FFFh) not c 3FFFh) code	code-protecte e-protected	ed						
bit 0	CP0: Code 1 = Block 0 0 = Block 0	Protection b (000200-00 (000200-00	it 1FFFh) not c 1FFFh) code	code-protecte	ed						
	Note 1:	Unimplemer	nted in PIC18	8FX48 device	es; maintair	n this bit set	t.				

REGISTER 24-5: CONFIG5L: CONFIGURATION REGISTER 5 LOW (BYTE ADDRESS 300008h)

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value when device	ce is unprogrammed	u = Unchanged from programmed state

REGISTER 24-6: CONFIG5H: CONFIGURATION REGISTER 5 HIGH (BYTE ADDRESS 300009h)

	R/C-1	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
	CPD	CPB	_	—	—	—	—	—
	bit 7							bit 0
bit 7	CPD: Data	EEPROM	Code Protec	tion bit				
	1 = Data E	EPROM no	t code-prote	cted				
	0 = Data E	EPROM co	de-protected	ł				
bit 6	CPB: Boot	Block Code	Protection	bit				
	1 = Boot Block (000000-0001FFh) not code-protected							
	0 = Boot B	lock (00000	0-0001FFh)	code-protect	cted			
bit 5-0	Unimplemented: Read as '0'							
	Legend:							
	R = Reada	ble bit	C = Clear	able bit	U = Unin	nplemented	bit, read as	'0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

24.2 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKI pin. That means that the WDT will run, even if the clock on the OSC1/CLKI and OSC2/CLKO/RA6 pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device Reset (Watchdog Timer Reset). If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer wake-up). The TO bit in the RCON register will be cleared upon a WDT time-out.

The Watchdog Timer is enabled/disabled by a device configuration bit. If the WDT is enabled, software execution may not disable this function. When the WDTEN configuration bit is cleared, the SWDTEN bit enables/disables the operation of the WDT. The WDT time-out period values may be found in **Section 27.0** "**Electrical Characteristics**" under parameter #31. Values for the WDT postscaler may be assigned using the configuration bits.

Note: The CLRWDT and SLEEP instructions clear the WDT and the postscaler if assigned to the WDT and prevent it from timing out and generating a device Reset condition.

Note: When a CLRWDT instruction is executed and the postscaler is assigned to the WDT, the postscaler count will be cleared but the postscaler assignment is not changed.

24.2.1 CONTROL REGISTER

Register 24-13 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to override the WDT enable configuration bit only when the configuration bit has disabled the WDT.

REGISTER 24-13: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN
bit 7							bit 0

bit 7-1 Unimplemented: Read as '0'

1 = Watchdog Timer is on

0 = Watchdog Timer is turned off if the WDTEN configuration bit in the Configuration register = 0

Legend:

Legena.	
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	-n = Value at POR

bit 0 SWDTEN: Software Controlled Watchdog Timer Enable bit

25.0 INSTRUCTION SET SUMMARY

The PIC18 instruction set adds many enhancements to the previous PICmicro instruction sets, while maintaining an easy migration from these PICmicro instruction sets.

Most instructions are a single program memory word (16 bits) but there are three instructions that require two program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

The PIC18 instruction set summary in Table 25-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 25-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

- 1. The file register (specified by 'f')
- 2. The destination of the result (specified by 'd')
- 3. The accessed memory (specified by 'a')

The file register designator 'f' specifies which file register is to be used by the instruction.

The destination designator 'd' specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

- 1. The file register (specified by 'f')
- 2. The bit in the file register (specified by 'b')
- 3. The accessed memory (specified by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator 'f' represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by 'k')
- The desired FSR register to load the literal value into (specified by 'f')
- No operand required (specified by '—')

The **control** instructions may use some of the following operands:

- A program memory address (specified by 'n')
- The mode of the CALL or RETURN instructions (specified by 's')
- The mode of the table read and table write instructions (specified by 'm')
- No operand required (specified by '—')

All instructions are a single word, except for three double-word instructions. These three instructions were made double-word instructions so that all the required information is available in these 32 bits. In the second word, the 4 MSbs are '1's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s. Two-word branch instructions (if true) would take 3 μ s.

Figure 25-1 shows the general formats that the instructions can have.

All examples use the format 'nnh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

The Instruction Set Summary, shown in Table 25-2, lists the instructions recognized by the Microchip MPASM[™] Assembler.

Section 25.2 "Instruction Set" provides a description of each instruction.

25.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified and the result is stored according to either the instruction or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a "CLRF PORTB" instruction will read PORTB, clear all the data bits, then write the result back to PORTB. This example would have the unintended result that the condition that sets the RBIF flag would be cleared.

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BNOV Branch if Not Overflow								
Synta	ax:	[<i>label</i>] BN	[<i>label</i>] BNOV n					
Oper	ands:	-128 ≤ n ≤ 1	-128 ≤ n ≤ 127					
Oper	ation:	if Overflow I (PC) + 2 + 2	if Overflow bit is '0' (PC) + 2 + 2n \rightarrow PC					
Statu	is Affected:	None	None					
Enco	oding:	1110	0101 r	ınnn	nnnn			
Desc	ription:	If the Overfil program will The 2's com added to the incremented tion, the new PC + 2 + 2r two-cycle in	If the Overflow bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruc- tion, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.					
Word	ls:	1						
Cycle	es:	1(2)						
Q Cycle Activity: If Jump:								
	Q1	Q2	Q3		Q4			
	Decode	Read literal 'n'	Process Data	Wri	te to PC			
	No operation	No operation	No operation	ор	No eration			
lf No	o Jump:							
	Q1	Q2	Q3		Q4			
	Decode	Read literal 'n'	Process Data	ор	No eration			
Example: HERE BNOV Jump								
Before Instruction PC = address (HERE)								
After Instruction If Overflow = 0; PC = address (Jump) If Overflow = 1; PC = address (HERE + 2)								

BNZ		Branch if Not Zero					
Synta	ax:	[<i>label</i>] BNZ n					
Oper	ands:	-128 ≤ n ≤ 1	27				
Oper	ation:	if Zero bit is (PC) + 2 + 2	'₀' 2n → PC				
Statu	s Affected:	None					
Enco	ding:	1110	0001	nnnn	nnnn		
Desc	ription:	If the Zero bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruc- tion, the new address will be PC + 2 + 2n. This instruction is then a					
Word	s:	1					
Cycles:		1(2)					
Q C If Ju	ycle Activity: mp:						
	Q1	Q2	Q3	3	Q4		
	Decode	Read literal 'n'	Proce Data	ess N a	Write to PC		
	No operation	No operation	No operation		No operation		
If No	Jump:						
	Q1	Q2	Q3	3	Q4		
	Decode	Read literal 'n'	Proce Data	ess a	No operation		
		L			•		
<u>Exan</u>	<u>iple:</u>	HERE	BNZ	Jump			
Before Instruction		tion = ad	dress (F	HERE)			
	If Zero PC	= 0; = ad	dress (;	Tummo)			





APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (June 2001)

Original data sheet for the PIC18FXX8 family.

Revision B (May 2002)

Updated information on CAN module, device memory and register maps, I/O ports and Enhanced CCP.

Revision C (January 2003)

This revision includes the DC and AC Characteristics Graphs and Tables (see Section 28.0 "DC and AC Characteristics Graphs and Tables"), Section 27.0 "Electrical Characteristics" have been updated and CAN certification information has been added.

Revision D (September 2004)

Data Sheet Errata (DS80134 and DS80161) issues have been addressed and corrected along with minor corrections to the data sheet text.

Revision E (October 2006)

Packaging diagrams updated.

TABLE B-1: DEVICE DIFFERENCES

Features		PIC18F248	PIC18F258	PIC18F448	PIC18F458
Internal	Bytes	16K	32K	16K	32K
Program Memory	# of Single-Word Instructions	8192	16384	8192	16384
Data Memory	(Bytes)	768	1536	768	1536
I/O Ports		Ports A, B, C	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C, D, E
Enhanced Capture/Compare/PWM Modules		—	_	1	1
Parallel Slave Port		No	No	Yes	Yes
10-bit Analog-to-Digital Converter		5 input channels	5 input channels	8 input channels	8 input channels
Analog Comparators		No	No	2	2
Analog Comparators VREF Output		N/A	N/A	Yes	Yes
Packages		28-pin SPDIP 28-pin SOIC	28-pin SPDIP 28-pin SOIC	40-pin PDIP 44-pin PLCC 44-pin TQFP	40-pin PDIP 44-pin PLCC 44-pin TQFP

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.



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