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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d7308hsc

List of Figures

List of Tables

Features

Table 1 shows the features of the Z86D73.

Table 1. Features

Device	OTP (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86D73	32	236	31	2.0 V–3.6 V

Note: *General purpose

- Low power consumption–40 mW (typical)
- Three standby modes
  - Stop—2 µA (typical)
  - Halt—0.8 mA (typical)
  - Low voltage
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low-voltage detection with flag
- Programmable watch-dog/power-on reset circuits
- Two independent comparators with programmable interrupt polarity
- Mask selectable pull-up transistors on ports 0, 1, 2, 3
- Programmable mask options
  - Oscillator selection: RC oscillator versus crystal or other clock source

- Oscillator operational mode: normal high-frequency operation enabled or 32-KHz operation enabled
- Port 0: 0–3 pull-ups
- Port 0: 4–7 pull-ups
- Port 1: 0–3 pull-ups
- Port 1: 4–7 pull-ups
- Port 2: 0–7 pull-ups
- Port 3: pull-ups
- Port 0: 0–3 mouse mode: normal mode (.5V_{DD} input threshold) versus mouse mode (.4V_{DD} input threshold)

Note: The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at V_{CC}=3 V and 450 KΩ ±50% at V_{CC}=2 V.

General Description

The Z86D73 is an OTP-based member of the MCU family of IR (infrared) microcontrollers. With 237 bytes of general-purpose RAM and 32 KB of ROM, ZiLOG's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86D73 architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86D73 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (see Figure 2).

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ Read/Write (Output, Write Low)

The R/$\overline{W}$ signal is Low when the CCP is writing to the external program or data memory.

R/$\overline{RL}$ (Input)

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble), depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode (if selected as an address output), along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ through P3M bits D4 and D3 (see Figure 10).

A ROM mask option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This option allows direct interface to mouse/trackball IR sensors.

Port 1 (P17–P10)

Port 1 (see Figure 11) is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (AS) and Data Strobe (DS) lines and by the Read/Write (R/W) and Data Memory (DM) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, AS, DS, and R/W, allowing the Z86D73 to share common resources in multiprocessor and DMA applications. Port 1 can also be configured for standard port output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

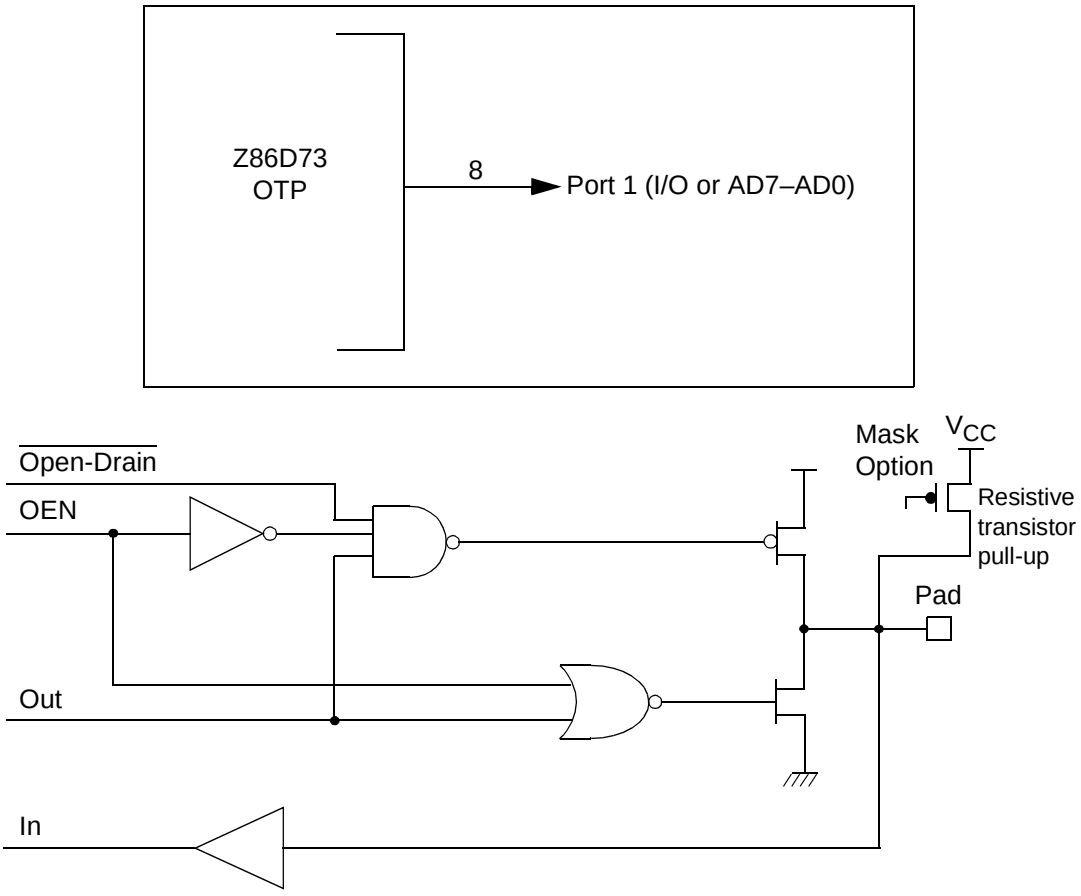


Figure 11. Port 1 Configuration

Stack

The Z86D73 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed

Table 10. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

Table 12. CTR(D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Initial_T16_Out/ Falling_Edge	-------0			**Transmit Mode**
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If the result is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/ Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the Ping-Pong mode or in independent normal operation mode. Setting this field to “Normal Operation Mode” terminates the “Ping-Pong Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This

Table 13. CTR2 (D)02h: Counter/Timer16 Control Register (Continued)

Field	Bit Position		Value	Description
T16 _Clock	---43---	R/W	00 01 10 11	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0 1	Disable Data Capture Int. Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Timeout Int. Enable Timeout Int.
P35_Out	-------0	R/W	0* 1	P35 as Port Output T16 Output on P35

Note:
*Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In Transmit Mode, when set to 0, the counter reloads the initial value when the terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 50.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2 Stop-Mode Recovery Register 2

Table 14 lists and briefly describes the fields for this register.

Table 14. SMR2(F)0Dh: Stop-Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0†	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Port pins configured as outputs are ignored as a SMR recovery source.
† Indicates the value upon Power-On Reset

T8 Demodulation Mode

Program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 24 and Figure 25).

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86D73 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 16.

Table 16. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

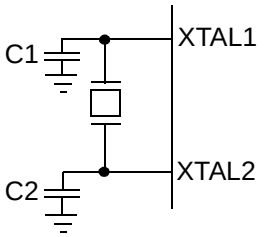
Notes: F = Falling Edge; R = Rising Edge
***In stop mode, the comparators are turned off.

Clock

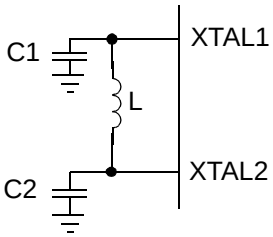
The Z86D73 on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The Z86D73 on-chip oscillator can be driven with a low-cost RC network or other suitable external clock source.

For 32-kHz crystal operation, an external feedback (Rf) and a serial resistor (Rd) are required. See Figure 32.

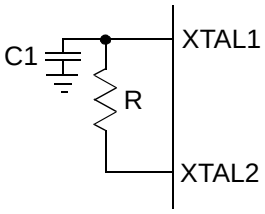
The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 32).



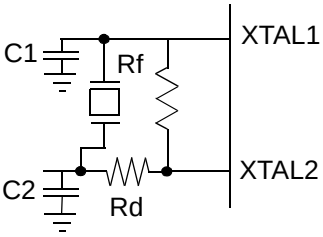
Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz



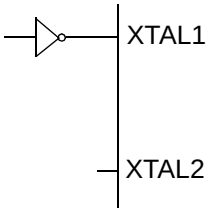
LC
C1, C2 = 22 pF
L = 130 µH *
f = 3 MHz *



RC
@ 3V VCC (TYP)
C1 = 33 pF *
R = 1K *



32 kHz XTAL
C1 = 20 pF, C = 33 pF
Rd = 56 - 470K
Rf = 10 M



External Clock

* Preliminary value including pin parasitics

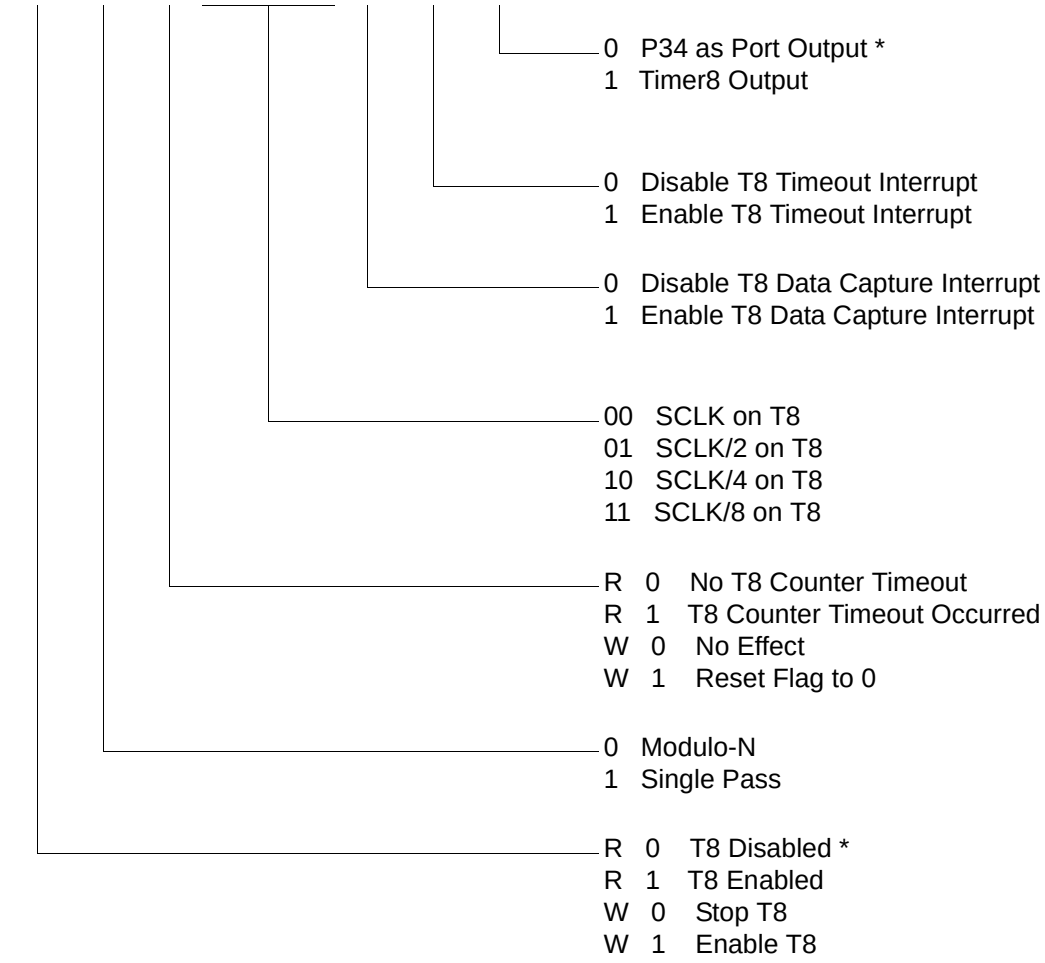
Figure 32. Oscillator Configuration

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are shown in Figure 40 through Figure 43.

CTR0 (0D) 0H

D7	D6	D5	D4	D3	D2	D1	D0



* Default setting after reset

Figure 40. TC8 Control Register ((0D) OH: Read/Write Except Where Noted)

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are shown in Figure 44 through Figure 57.

SMR (0F) 0B

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0 OFF *
1 ON

Reserved (Must be 0)

Stop-Mode Recovery Source
000 POR Only *
001 Reserved
010 P31
011 P32
100 P33
101 P27
110 P2 NOR 0–3
111 P2 NOR 0–7

Stop Delay
0 OFF
1 ON *

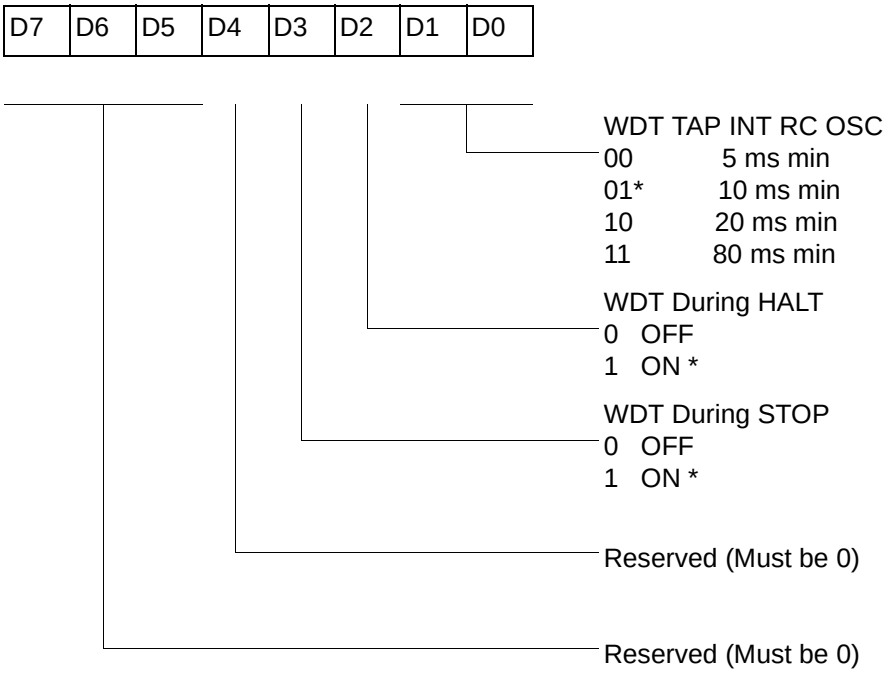
Stop Recovery Level * * *
0 Low *
1 High

Stop Flag
0 POR *
1 Stop Recovery * *

* Default setting after reset
* * Default setting after reset and stop-mode recovery
* * * At the XOR gate input

Figure 44. Stop-Mode Recovery Register ((0F) 0Bh: D6–D0=Write Only, D7=Read Only)

WDTMR (0F) 0F



* Default setting after reset

Figure 46. Watch-Dog Timer Register ((0F) 0Fh: Write Only)

R249 IPR

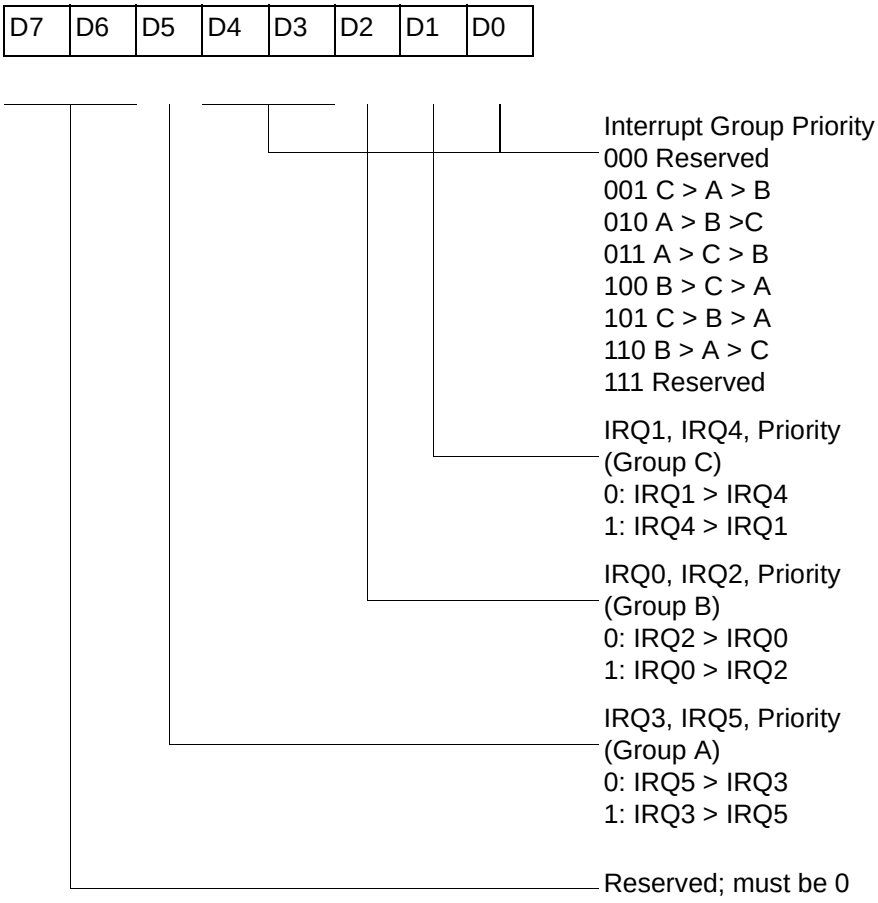


Figure 51. Interrupt Priority Register (F9h: Write Only)

R252 Flags

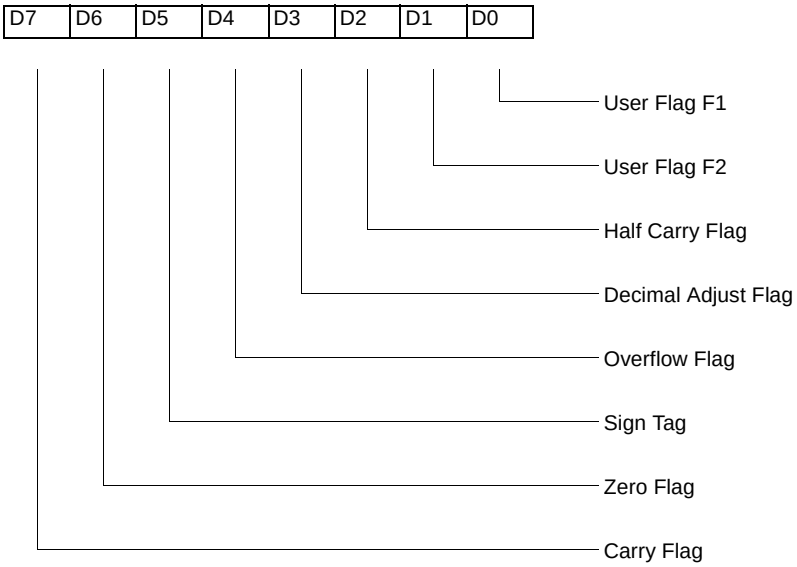
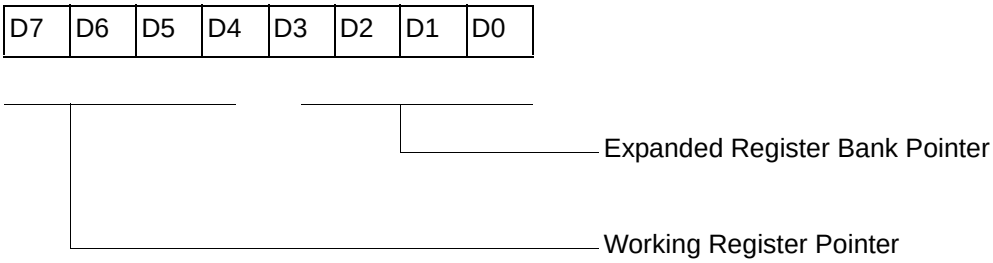


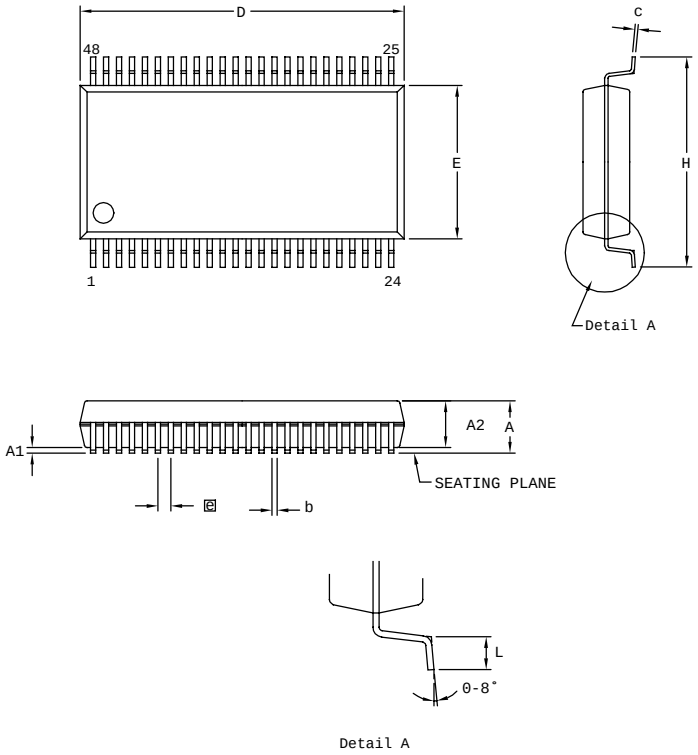
Figure 54. Flag Register (FCh: Read/Write)

R253 RP



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDh: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 61. 48-Pin SSOP Package Design

Note: Please check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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