



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                             |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Obsolete                                                                                                                    |
| Core Processor             | Z8                                                                                                                          |
| Core Size                  | 8-Bit                                                                                                                       |
| Speed                      | 8MHz                                                                                                                        |
| Connectivity               | -                                                                                                                           |
| Peripherals                | Brown-out Detect/Reset, LVD, POR, WDT                                                                                       |
| Number of I/O              | 31                                                                                                                          |
| Program Memory Size        | 32KB (32K x 8)                                                                                                              |
| Program Memory Type        | OTP                                                                                                                         |
| EEPROM Size                | -                                                                                                                           |
| RAM Size                   | 236 x 8                                                                                                                     |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V                                                                                                                   |
| Data Converters            | -                                                                                                                           |
| Oscillator Type            | Internal                                                                                                                    |
| Operating Temperature      | 0°C ~ 70°C (TA)                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                               |
| Package / Case             | 44-LCC (J-Lead)                                                                                                             |
| Supplier Device Package    | -                                                                                                                           |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/zilog/z86d7308vsc">https://www.e-xfl.com/product-detail/zilog/z86d7308vsc</a> |



# Table of Contents

|                                               |    |
|-----------------------------------------------|----|
| Features                                      | 1  |
| General Description                           | 2  |
| Pin Description                               | 5  |
| Absolute Maximum Ratings                      | 9  |
| Standard Test Conditions                      | 10 |
| Capacitance                                   | 10 |
| DC Characteristics                            | 11 |
| AC Characteristics                            | 13 |
| Pin Functions                                 | 18 |
| DS (Output, Active Low)                       | 18 |
| AS (Output, Active Low)                       | 18 |
| XTAL1 Crystal 1 (Time-Based Input)            | 19 |
| XTAL2 Crystal 2 (Time-Based Output)           | 19 |
| R/W Read/Write (Output, Write Low)            | 19 |
| R/RL (Input)                                  | 19 |
| Port 0 (P07–P00)                              | 19 |
| Port 1 (P17–P10)                              | 21 |
| Port 2 (P27–P20)                              | 22 |
| Port 3 (P37–P31)                              | 23 |
| RESET (Input, Active Low)                     | 26 |
| Functional Description                        | 26 |
| Program Memory                                | 26 |
| RAM                                           | 26 |
| Expanded Register File                        | 28 |
| Register File                                 | 31 |
| Stack                                         | 32 |
| Register Description                          | 33 |
| Counter/Timer Functional Blocks               | 42 |
| Expanded Register File Control Registers (0D) | 68 |
| Expanded Register File Control Registers (0F) | 72 |
| Package Information                           | 82 |
| Ordering Information                          | 85 |
| Precharacterization Product                   | 86 |



# List of Figures

|                                                                  |    |
|------------------------------------------------------------------|----|
| Figure 1. Counter/Timers Diagram .....                           | 3  |
| Figure 2. Functional Block Diagram .....                         | 4  |
| Figure 3. 40-Pin DIP Pin Assignment .....                        | 5  |
| Figure 4. 44-Pin QFP Pin Assignment .....                        | 6  |
| Figure 5. 44-Pin PLCC Assignment .....                           | 6  |
| Figure 6. 48-Pin SSOP Assignment .....                           | 7  |
| Figure 7. Test Load Diagram .....                                | 10 |
| Figure 8. External I/O or Memory Read/Write Timing .....         | 13 |
| Figure 9. Additional Timing .....                                | 16 |
| Figure 10. Port 0 Configuration .....                            | 20 |
| Figure 11. Port 1 Configuration .....                            | 21 |
| Figure 12. Port 2 Configuration .....                            | 22 |
| Figure 13. Port 3 Configuration .....                            | 23 |
| Figure 14. Port 3 Counter/Timer Output Configuration .....       | 25 |
| Figure 15. Program Memory Map (32K OTP) .....                    | 27 |
| Figure 16. Expanded Register File Architecture .....             | 29 |
| Figure 17. Register Pointer .....                                | 30 |
| Figure 18. Register Pointer—Detail .....                         | 31 |
| Figure 19. Glitch Filter Circuitry .....                         | 42 |
| Figure 20. Transmit Mode Flowchart .....                         | 43 |
| Figure 21. 8-Bit Counter/Timer Circuits .....                    | 44 |
| Figure 22. T8_OUT in Single-Pass Mode .....                      | 45 |
| Figure 23. T8_OUT in Modulo-N Mode .....                         | 45 |
| Figure 24. Demodulation Mode Count Capture Flowchart .....       | 47 |
| Figure 25. Demodulation Mode Flowchart .....                     | 48 |
| Figure 26. 16-Bit Counter/Timer Circuits .....                   | 49 |
| Figure 27. T16_OUT in Single-Pass Mode .....                     | 50 |
| Figure 28. T16_OUT in Modulo-N Mode .....                        | 50 |
| Figure 29. Ping-Pong Mode .....                                  | 52 |
| Figure 30. Output Circuit .....                                  | 52 |
| Figure 31. Interrupt Block Diagram .....                         | 54 |
| Figure 32. Oscillator Configuration .....                        | 56 |
| Figure 33. Port Configuration Register (PCON) (Write Only) ..... | 58 |
| Figure 34. Stop-Mode Recovery Register .....                     | 59 |



|                                                                                            |    |
|--------------------------------------------------------------------------------------------|----|
| Figure 35. SCLK Circuit .....                                                              | 60 |
| Figure 36. Stop-Mode Recovery Source .....                                                 | 61 |
| Figure 37. Stop-Mode Recovery Register 2 ((0F) DH: D2–D4,<br>D6 Write Only) .....          | 63 |
| Figure 38. Watch-Dog Timer Mode Register (Write Only) .....                                | 64 |
| Figure 39. Resets and WDT .....                                                            | 66 |
| Figure 40. TC8 Control Register ((0D) OH: Read/Write<br>Except Where Noted) .....          | 68 |
| Figure 41. T8 and T16 Common Control Functions ((0D) 1h: Read/Write) ...                   | 69 |
| Figure 42. T16 Control Register ((0D) 2h: Read/Write<br>Except Where Noted) .....          | 70 |
| Figure 43. Low-Voltage Detection .....                                                     | 71 |
| Figure 44. Stop-Mode Recovery Register ((0F) 0Bh: D6–D0=Write Only,<br>D7=Read Only) ..... | 72 |
| Figure 45. Stop-Mode Recovery Register 2 ((0F) 0Dh: D2–D4,<br>D6 Write Only) .....         | 73 |
| Figure 46. Watch-Dog Timer Register ((0F) 0Fh: Write Only) .....                           | 74 |
| Figure 47. Port Configuration Register (PCON) ((0F) 0h: Write Only) .....                  | 75 |
| Figure 48. Port 2 Mode Register (F6h: Write Only) .....                                    | 75 |
| Figure 49. Port 3 Mode Register (F7h: Write Only) .....                                    | 76 |
| Figure 50. Port 0 and 1 Mode Register (F8h: Write Only) .....                              | 77 |
| Figure 51. Interrupt Priority Register (F9h: Write Only) .....                             | 78 |
| Figure 52. Interrupt Request Register (FAh: Read/Write) .....                              | 79 |
| Figure 53. Interrupt Mask Register (FBh: Read/Write) .....                                 | 79 |
| Figure 54. Flag Register (FCh: Read/Write) .....                                           | 80 |
| Figure 55. Register Pointer (FDh: Read/Write) .....                                        | 80 |
| Figure 56. Stack Pointer High (FEh: Read/Write) .....                                      | 81 |
| Figure 57. Stack Pointer Low (FFh: Read/Write) .....                                       | 81 |
| Figure 58. 40-Pin DIP Package Diagram .....                                                | 82 |
| Figure 59. 44-Pin PLCC Package Diagram .....                                               | 82 |
| Figure 60. 44-Pin QFP Package Design .....                                                 | 83 |
| Figure 61. 48-Pin SSOP Package Design .....                                                | 84 |



# *List of Tables*

|           |                                                                 |    |
|-----------|-----------------------------------------------------------------|----|
| Table 1.  | Features .....                                                  | 1  |
| Table 2.  | Power Connections .....                                         | 3  |
| Table 3.  | Pin Identification .....                                        | 7  |
| Table 4.  | Absolute Maximum Ratings .....                                  | 9  |
| Table 5.  | Capacitance .....                                               | 10 |
| Table 6.  | DC Characteristics .....                                        | 11 |
| Table 7.  | External I/O or Memory Read and Write Timing (Preliminary) .... | 14 |
| Table 8.  | Additional Timing .....                                         | 17 |
| Table 9.  | Pin Assignments .....                                           | 24 |
| Table 10. | Expanded Register Group D .....                                 | 32 |
| Table 11. | CTR0 (D)00 Counter/Timer8 Control Register .....                | 35 |
| Table 12. | CTR(D)01h T8 and T16 Common Functions .....                     | 37 |
| Table 13. | CTR2 (D)02h: Counter/Timer16 Control Register .....             | 39 |
| Table 14. | SMR2(F)0Dh: Stop-Mode Recovery Register 2* .....                | 41 |
| Table 15. | Interrupt Types, Sources, and Vectors .....                     | 55 |
| Table 16. | IRQ Register* .....                                             | 55 |
| Table 17. | Stop-Mode Recovery Source .....                                 | 62 |
| Table 18. | WDT Time Select* .....                                          | 65 |
| Table 19. | Mask Selectable Options .....                                   | 67 |
| Table 20. | Z86D73 Ordering Information .....                               | 85 |



- Oscillator operational mode: normal high-frequency operation enabled or 32-KHz operation enabled
- Port 0: 0–3 pull-ups
- Port 0: 4–7 pull-ups
- Port 1: 0–3 pull-ups
- Port 1: 4–7 pull-ups
- Port 2: 0–7 pull-ups
- Port 3: pull-ups
- Port 0: 0–3 mouse mode: normal mode ( $.5V_{DD}$  input threshold) versus mouse mode ( $.4V_{DD}$  input threshold)

► **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of  $200\text{ K}\Omega \pm 50\%$  at  $V_{CC}=3\text{ V}$  and  $450\text{ K}\Omega \pm 50\%$  at  $V_{CC}=2\text{ V}$ .

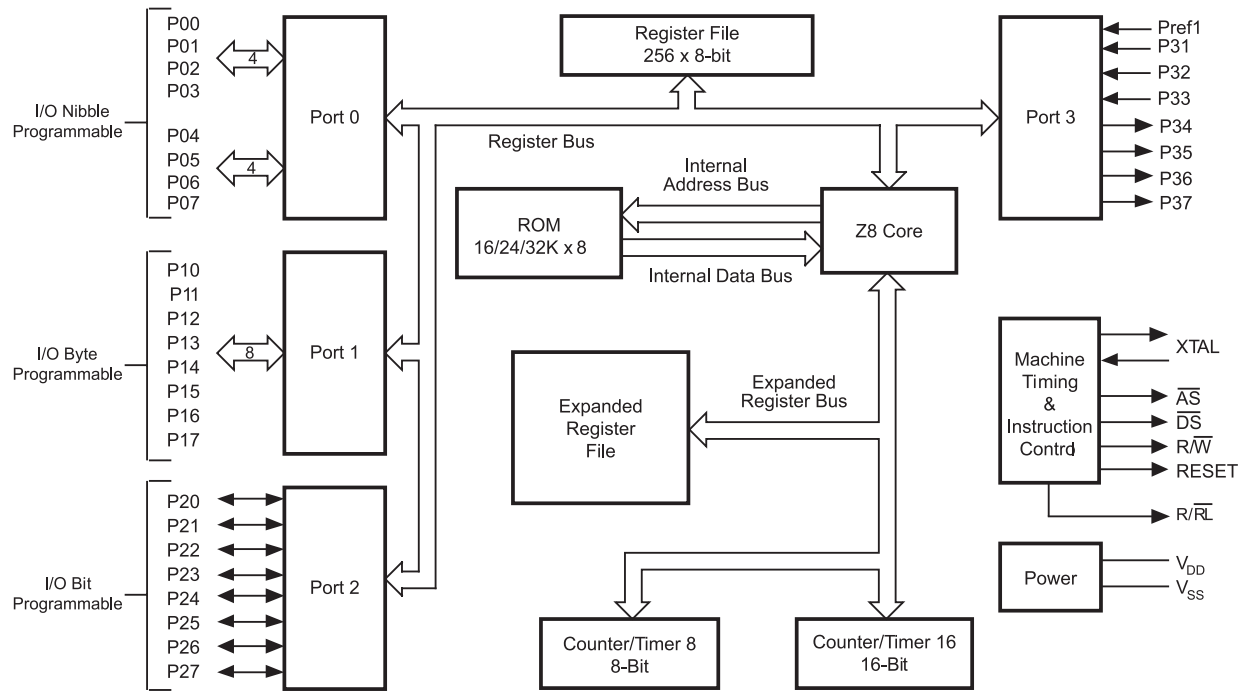
## General Description

The Z86D73 is an OTP-based member of the MCU family of IR (infrared) micro-controllers. With 237 bytes of general-purpose RAM and 32 KB of ROM, ZiLOG's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86D73 architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86D73 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (see Figure 2).



**Figure 2. Functional Block Diagram**

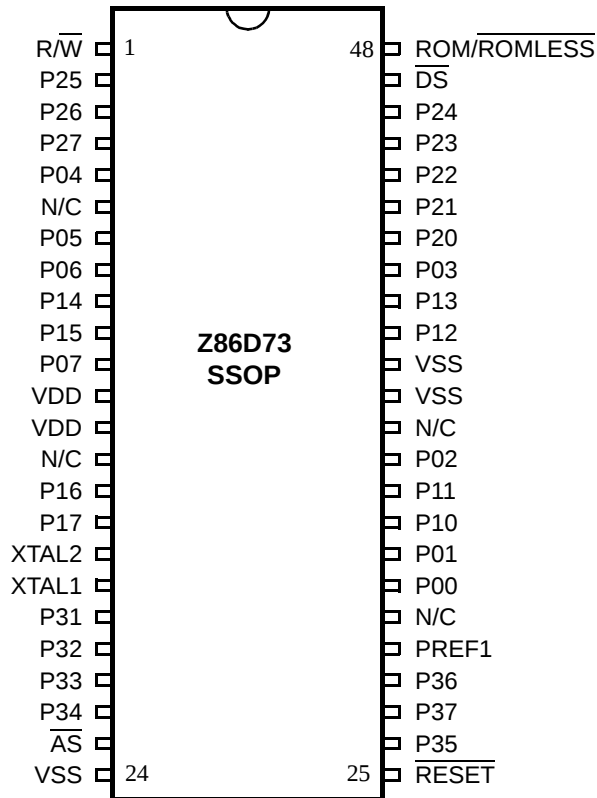


Figure 6. 48-Pin SSOP Assignment

Table 3. Pin Identification

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin QFP # | 48-Pin SSOP # | Symbol |
|--------------|---------------|--------------|---------------|--------|
| 26           | 40            | 23           | 31            | P00    |
| 27           | 41            | 24           | 32            | P01    |
| 30           | 44            | 27           | 35            | P02    |
| 34           | 5             | 32           | 41            | P03    |
| 5            | 17            | 44           | 5             | P04    |
| 6            | 18            | 1            | 7             | P05    |
| 7            | 19            | 2            | 8             | P06    |
| 10           | 22            | 5            | 11            | P07    |
| 28           | 42            | 25           | 33            | P10    |



Table 3. Pin Identification (Continued)

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin QFP # | 48-Pin SSOP # | Symbol             |
|--------------|---------------|--------------|---------------|--------------------|
| 29           | 43            | 26           | 34            | P11                |
| 32           | 3             | 30           | 39            | P12                |
| 33           | 4             | 31           | 40            | P13                |
| 8            | 20            | 3            | 9             | P14                |
| 9            | 21            | 4            | 10            | P15                |
| 12           | 25            | 8            | 15            | P16                |
| 13           | 26            | 9            | 16            | P17                |
| 35           | 6             | 33           | 42            | P20                |
| 36           | 7             | 34           | 43            | P21                |
| 37           | 8             | 35           | 44            | P22                |
| 38           | 9             | 36           | 45            | P23                |
| 39           | 10            | 37           | 46            | P24                |
| 2            | 14            | 41           | 2             | P25                |
| 3            | 15            | 42           | 3             | P26                |
| 4            | 16            | 43           | 4             | P27                |
| 16           | 29            | 12           | 19            | P31                |
| 17           | 30            | 13           | 20            | P32                |
| 18           | 31            | 14           | 21            | P33                |
| 19           | 32            | 15           | 22            | P34                |
| 22           | 36            | 19           | 26            | P35                |
| 24           | 38            | 21           | 28            | P36                |
| 23           | 37            | 20           | 27            | P37                |
| 20           | 33            | 16           | 23            | $\overline{AS}$    |
| 40           | 11            | 38           | 47            | $\overline{DS}$    |
| 1            | 13            | 40           | 1             | R/W                |
| 21           | 35            | 18           | 25            | $\overline{RESET}$ |
| 15           | 28            | 11           | 18            | XTAL1              |
| 14           | 27            | 10           | 17            | XTAL2              |
| 11           | 23, 24        | 6, 7         | 12, 13        | V <sub>DD</sub>    |



Table 3. Pin Identification (Continued)

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin QFP # | 48-Pin SSOP # | Symbol          |
|--------------|---------------|--------------|---------------|-----------------|
| 31           | 1, 2, 34      | 17, 28, 29   | 24, 37, 38    | V <sub>SS</sub> |
| 25           | 39            | 22           | 29            | Pref1           |
|              | 12            | 39           | 48            | R/RL            |

## Absolute Maximum Ratings

Stresses greater than those listed in Table 4 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 4. Absolute Maximum Ratings

| Symbol           | Description                | Min  | Max   | Units |
|------------------|----------------------------|------|-------|-------|
| V <sub>CC</sub>  | Supply Voltage (*)         | −0.3 | +7.0  | V     |
| T <sub>STG</sub> | Storage Temperature        | −65° | +150° | C     |
| T <sub>A</sub>   | Oper. Ambient Temperature. |      | †     | C     |

**Notes:**

\*Voltage on all pins with respect to GND.

†See Ordering Information on page 85.

## Port 1 (P17–P10)

Port 1 (see Figure 11) is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus<sup>®</sup>-compatible memory interface. The operations of Port 1 are supported by the Address Strobe ( $\overline{AS}$ ) and Data Strobe ( $\overline{DS}$ ) lines and by the Read/Write (R/W) and Data Memory (DM) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0,  $\overline{AS}$ ,  $\overline{DS}$ , and R/W, allowing the Z86D73 to share common resources in multiprocessor and DMA applications. Port 1 can also be configured for standard port output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

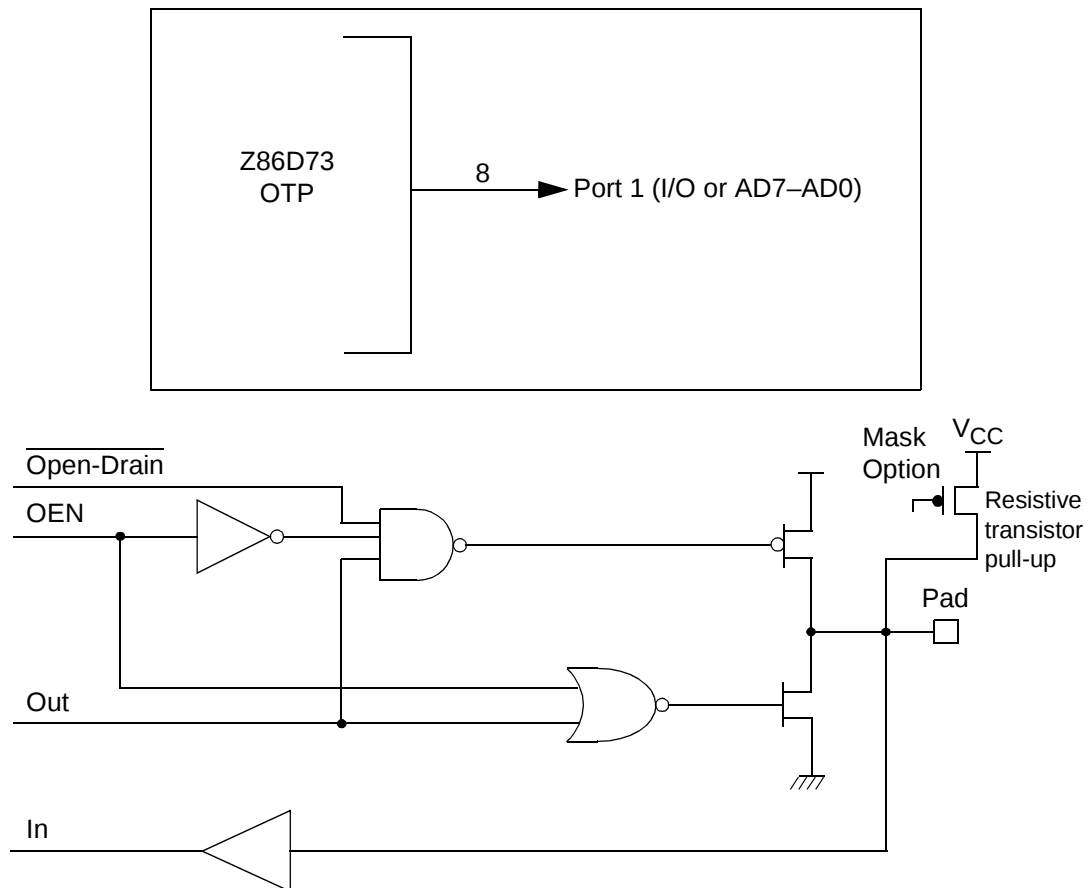


Figure 11. Port 1 Configuration



## Register Description

### LVD(D)0Ch Low-Voltage Detection Register

- **Note:** The LVD flag will be valid after enabling the detection for 20  $\mu$ S (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

| Field | Bit Position | Description           |                              |
|-------|--------------|-----------------------|------------------------------|
| LVD   | 765432--     | Reserved<br>No Effect |                              |
|       | -----1-      | R                     | 1<br>0*                      |
|       |              |                       | LV flag set<br>LV flag reset |
|       | -----0       | R/W                   | 1<br>0*                      |
|       |              |                       | Enable LVD<br>Disable LVD    |

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### HI8(D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register is used to hold the number of counts when the input signal is 1.

| Field         | Bit Position | Description |                            |
|---------------|--------------|-------------|----------------------------|
| T8_Capture_HI | 76543210     | R<br>W      | Captured Data<br>No Effect |

### L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register is used to hold the number of counts when the input signal is 0.

| Field         | Bit Position | Description |                            |
|---------------|--------------|-------------|----------------------------|
| T8_Capture_L0 | 76543210     | R<br>W      | Captured Data<br>No Effect |

**HI16(D)09h**

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

| Field          | Bit Position | Description                    |
|----------------|--------------|--------------------------------|
| T16_Capture_HI | 76543210     | R Captured Data<br>W No Effect |

**L016(D)08h**

This register holds the captured data from the output of the 16-bit Counter/Timer16. this register holds the LS-Byte of the data.

| Field          | Bit Position | Description                    |
|----------------|--------------|--------------------------------|
| T16_Capture_LO | 76543210     | R Captured Data<br>W No Effect |

**TC16H(D)07h Counter/Timer2 MS-Byte Hold Register**

| Field       | Bit Position | Description |
|-------------|--------------|-------------|
| T16_Data_HI | 76543210     | R/W Data    |

**TC16L(D)06h Counter/Timer2 LS-Byte Hold Register**

| Field       | Bit Position | Description |
|-------------|--------------|-------------|
| T16_Data_LO | 76543210     | R/W Data    |

**TC8H(D)05h Counter/Timer8 High Hold Register**

| Field       | Bit Position | Description |
|-------------|--------------|-------------|
| T8_Level_HI | 76543210     | R/W Data    |



### TC8L(D)04h Counter/Timer8 Low Hold Register

| Field       | Bit Position | Description |
|-------------|--------------|-------------|
| T8_Level_LO | 76543210     | R/W Data    |

### CTR0 Counter/Timer8 Control Register

Table 11 lists and briefly describes the fields for this register.

**Table 11. CTR0 (D)00 Counter/Timer8 Control Register**

| Field            | Bit Position |     | Value | Description               |
|------------------|--------------|-----|-------|---------------------------|
| T8_Enable        | 7-----       | R   | 0*    | Counter Disabled          |
|                  |              |     | 1     | Counter Enabled           |
|                  |              | W   | 0     | Stop Counter              |
|                  |              |     | 1     | Enable Counter            |
| Single/Modulo-N  | -6-----      | R/W | 0     | Modulo-N                  |
|                  |              |     | 1     | Single Pass               |
| Time_Out         | --5-----     | R   | 0     | No Counter Time-Out       |
|                  |              |     | 1     | Counter Time-Out Occurred |
|                  |              | W   | 0     | No Effect                 |
|                  |              |     | 1     | Reset Flag to 0           |
| T8_Clock         | ---43---     | R/W | 0 0   | SCLK                      |
|                  |              |     | 0 1   | SCLK/2                    |
|                  |              |     | 1 0   | SCLK/4                    |
|                  |              |     | 1 1   | SCLK/8                    |
| Capture_INT_MASK | -----2--     | R/W | 0     | Disable Data Capture Int. |
|                  |              |     | 1     | Enable Data Capture Int.  |
| Counter_INT_Mask | -----1-      | R/W | 0     | Disable Time-Out Int.     |
|                  |              |     | 1     | Enable Time-Out Int.      |
| P34_Out          | -----0       | R/W | 0*    | P34 as Port Output        |
|                  |              |     | 1     | T8 Output on P34          |

**Note:**

\*Indicates the value upon Power-On Reset.

### T8 Enable

This field enables T8 when set (written) to 1.



### Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Therefore, reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



**Note:** Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

### Example

When the status of bit 5 is 1, a timer reset condition occurs.

### T8 Clock

This bit defines the frequency of the input signal to T8.

### Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

**Counter\_INT\_Mask**

Set this bit to allow an interrupt when T16 times out.

**P35\_Out**

This bit defines whether P35 is used as a normal output pin or T16 output.

**SMR2 Stop-Mode Recovery Register 2**

Table 14 lists and briefly describes the fields for this register.

**Table 14. SMR2(F)0Dh: Stop-Mode Recovery Register 2\***

| Field          | Bit Position  |   | Value            | Description                  |
|----------------|---------------|---|------------------|------------------------------|
| Reserved       | 7 - - - - -   |   | 0                | Reserved (Must be 0)         |
| Recovery Level | - 6 - - - - - | W | 0 <sup>†</sup>   | Low                          |
|                |               |   | 1                | High                         |
| Reserved       | - - 5 - - - - |   | 0                | Reserved (Must be 0)         |
| Source         | - - - 432 - - | W | 000 <sup>†</sup> | A. POR Only                  |
|                |               |   | 001              | B. NAND of P23–P20           |
|                |               |   | 010              | C. NAND of P27–P20           |
|                |               |   | 011              | D. NOR of P33–P31            |
|                |               |   | 100              | E. NAND of P33–P31           |
|                |               |   | 101              | F. NOR of P33–P31, P00, P07  |
|                |               |   | 110              | G. NAND of P33–P31, P00, P07 |
|                |               |   | 111              | H. NAND of P33–P31, P22–P20  |
| Reserved       | - - - - - 10  |   | 00               | Reserved (Must be 0)         |

**Notes:**

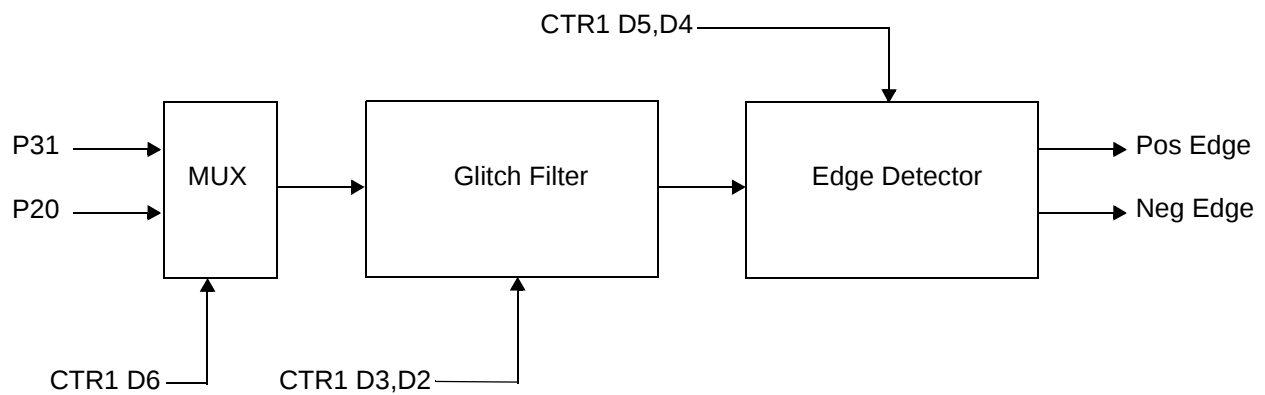
\* Port pins configured as outputs are ignored as a SMR recovery source.

<sup>†</sup> Indicates the value upon Power-On Reset

## Counter/Timer Functional Blocks

### Input Circuit

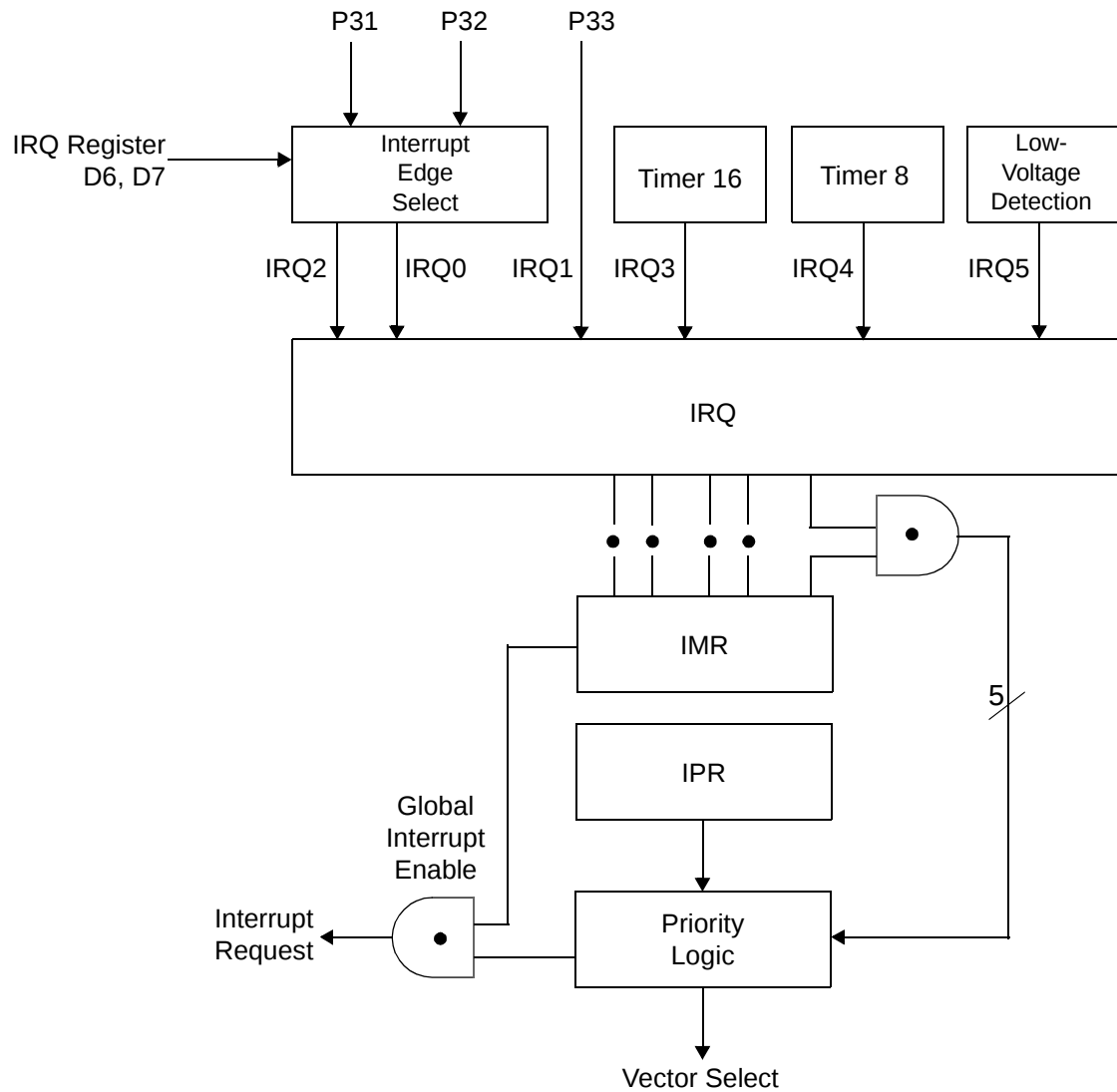
The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 19).



**Figure 19. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1; if it is 1, T8\_OUT is 0. See Figure 20.

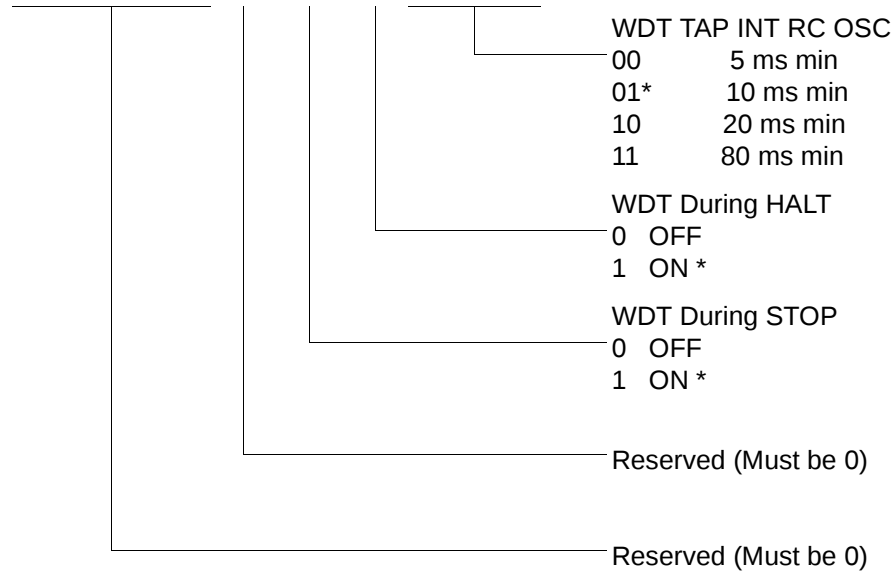


**Figure 31. Interrupt Block Diagram**



WDTMR (0F) 0F

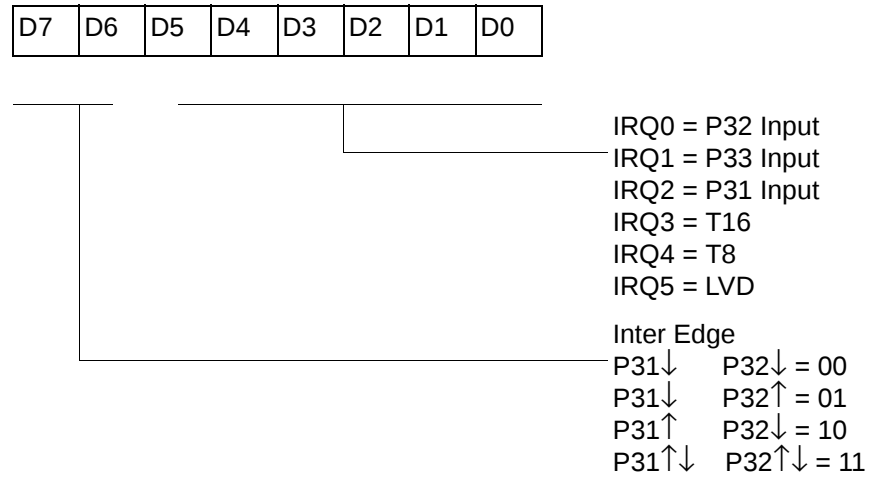
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



\* Default setting after reset

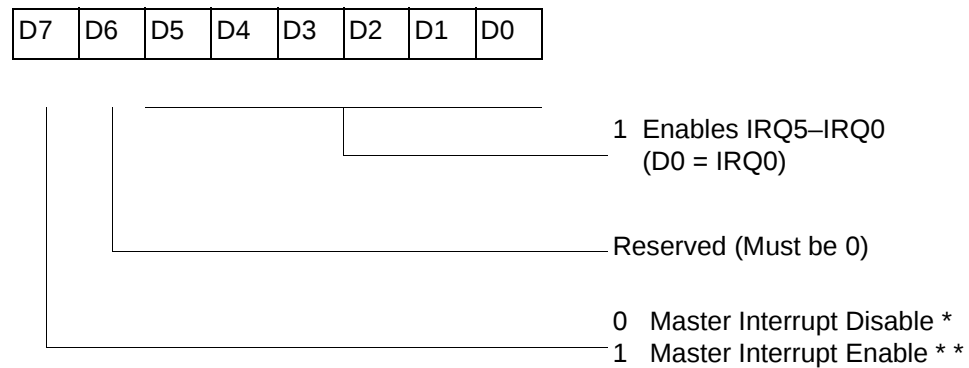
**Figure 46. Watch-Dog Timer Register ((0F) 0Fh: Write Only)**

### R250 IRQ



**Figure 52. Interrupt Request Register (FAh: Read/Write)**

### R251 IMR



\* Default setting after reset

\*\* Only by using E1, D1 instruction; D1 is required before changing the IMR register

**Figure 53. Interrupt Mask Register (FBh: Read/Write)**



## Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

ZiLOG, Inc.

532 Race Street

San Jose, CA 95126-3432

Telephone: (408) 558-8500

FAX: 408 558-8300

Internet: [HTTP://WWW.ZILOG.COM](http://www.ZiLOG.com)