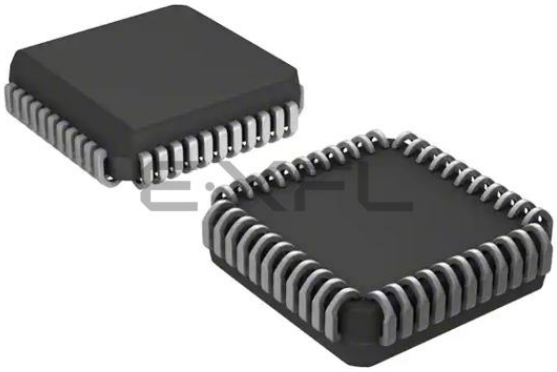

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d7308vsc00tr

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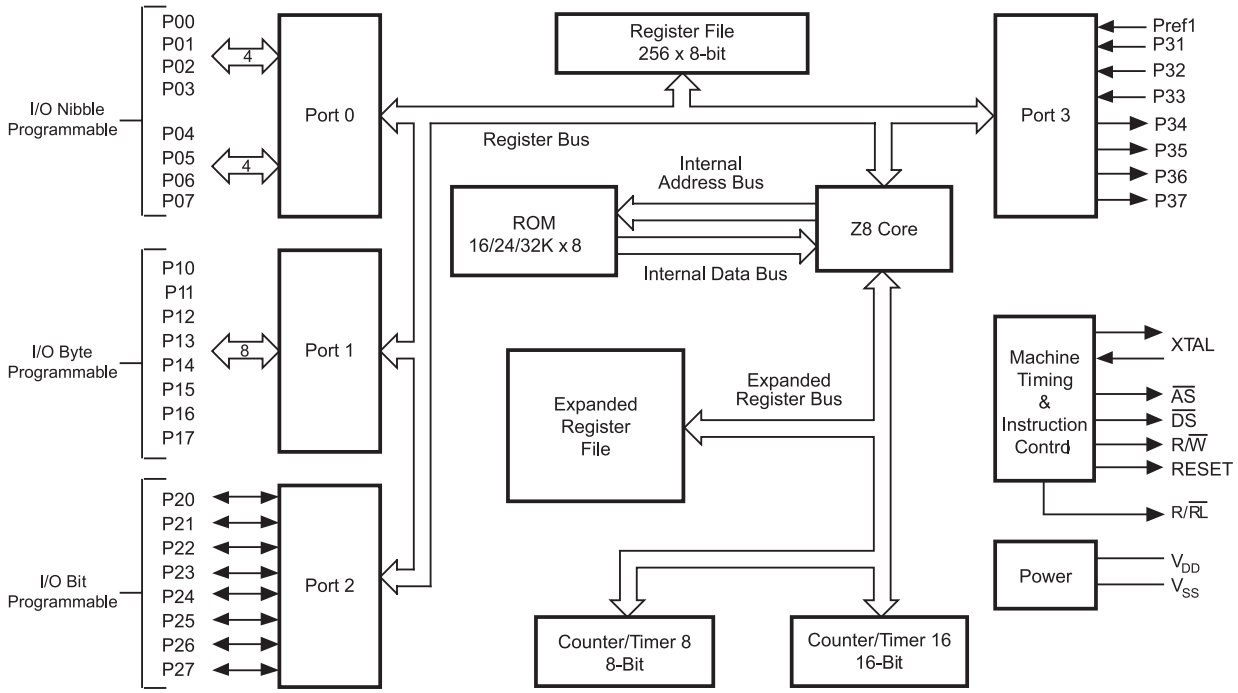


Figure 2. Functional Block Diagram

Table 3. Pin Identification (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	48-Pin SSOP #	Symbol
31	1, 2, 34	17, 28, 29	24, 37, 38	V_{SS}
25	39	22	29	Pref1
	12	39	48	R/$\overline{RL}$

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature.		†	C

Notes:
***** Voltage on all pins with respect to GND.
† See Ordering Information on page 85.

Table 6. DC Characteristics (Continued)

		T_A = 0°C to +70°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
I_{OL}	Output Leakage	2.0 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
		3.6 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
I_{CC}	Supply Current	2.0 V		10	mA	at 8.0 MHz	1, 2
		3.6 V		15	mA	at 8.0 MHz	1, 2
		2.0 V		250	µA	at 32 kHz	1, 2, 3
		3.6 V		850	µA	at 32 kHz	1, 2, 3
I_{CC1}	Standby Current (HALT Mode)	2.0 V		3	mA	V_{IN} = 0 V, V_{CC} at 8.0 MHz	1, 2
		3.6 V		5	mA	Same as above	1, 2
		2.0 V		2	mA	Clock Divide-by-16 at 8.0 MHz	1, 2
		3.6 V		4	mA	Same as above	1, 2
I_{CC2}	Standby Current (STOP Mode)	2.0 V		8	µA	V_{IN} = 0 V, V_{CC} WDT is not Running	4, 5
	Note: WDT, Comparators, Low Voltage Detection, and ADC (if applicable are disabled. The IC might draw more current if any of the above peripherals is enabled.	3.6 V		10	µA	Same as above	4, 5
		2.0 V		500	µA	V_{IN} = 0 V, V_{CC} WDT is Running	4, 5
		3.6 V		800	µA	Same as above	4, 5
I_{CC2}	Standby Current (Low Voltage)			25	µA	$V_{CC} < V_{BO}$	6
					µA		
T_{POR}	Power-On Reset	2.0 V	12	75	ms		
		3.6 V	5	20	ms		
V_{BO}	V_{CC} Low Voltage Protection			2.15	V	8 MHz max Ext. CLK Freq.	7
V_{LVD}	Vcc Low Voltage Detection			V_{BO} + 0.4	V	$V_{LVD} = V_{BO}$ + 0.4	8

Notes:

*All outputs excluding P00, P01, P36, and P37.

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. 32-kHz clock driver input.
4. The V_{BO} increases as the temperature decreases, except inputs at V_{CC}.
5. Oscillator stopped.
6. Oscillator stops when V_{CC} falls below V_{LV} limit.
7. V_{BO} increases as the temperature decreases.
8. Variance is 300 mV.

Table 7. External I/O or Memory Read and Write Timing (Preliminary) (Continued)

				T_A = 0 °C to +70 °C 8.0 MHz*			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
17	TdAS(DS)	$\overline{AS}$ Rising to $\overline{DS}$ Falling Delay	2.0 V 3.6 V	100 100		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Falling Delay	2.0 V 3.6 V	55 55		ns ns	2
19	TdDS(DM)	$\overline{DS}$ Rise to $\overline{DM}$ Valid Delay	2.0 V 3.6 V	70 70		ns ns	
20	ThDS(A)	$\overline{DS}$ Rise to Address Valid Hold Time	2.0 V 3.6 V	70 70		ns	

Notes:
1.When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
* Standard Test Load: All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

Figure 9 and Table 8 describe additional timing characteristics.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

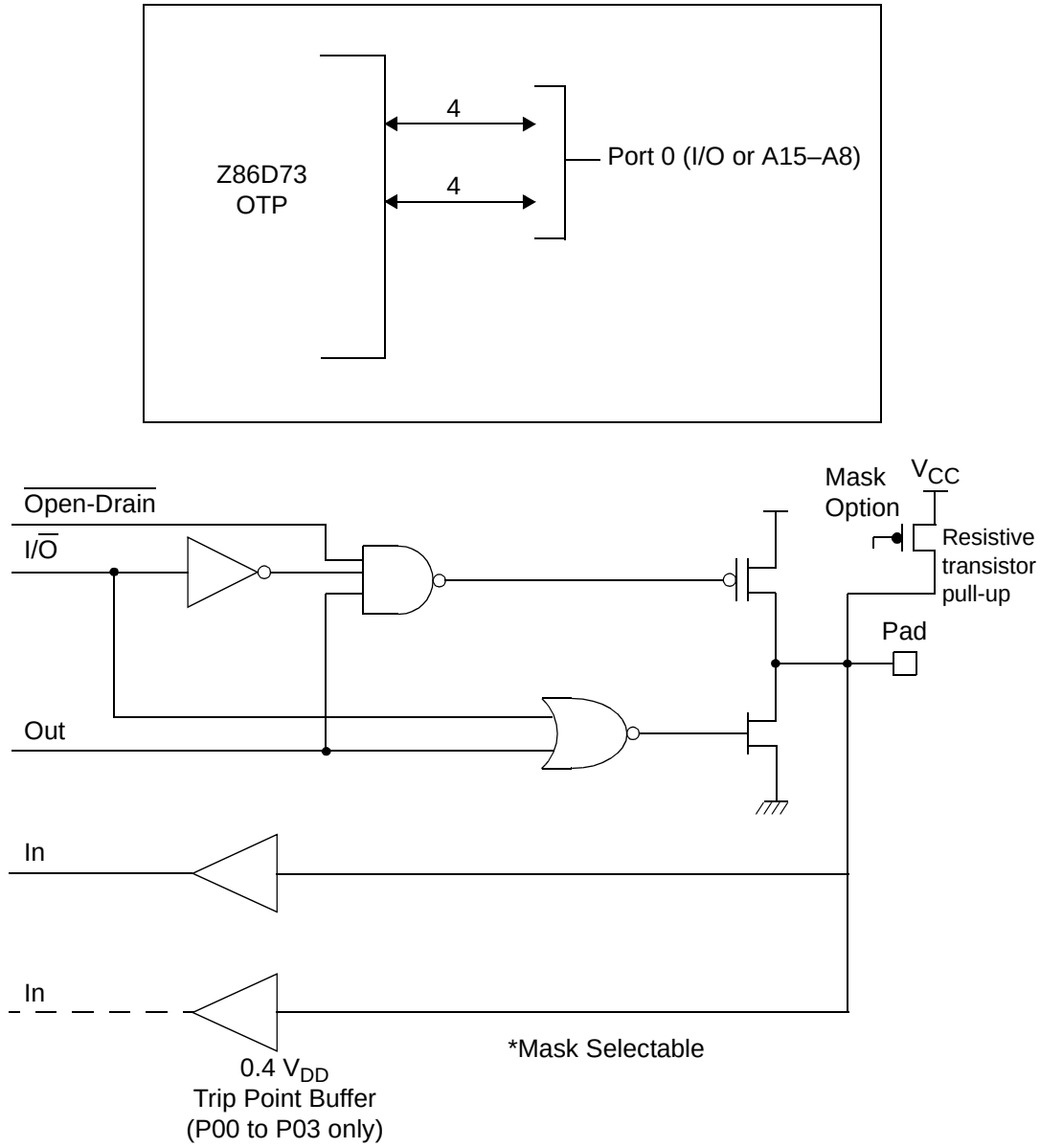


Figure 10. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 11) is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (AS) and Data Strobe (DS) lines and by the Read/Write (R/W) and Data Memory (DM) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, AS, DS, and R/W, allowing the Z86D73 to share common resources in multiprocessor and DMA applications. Port 1 can also be configured for standard port output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

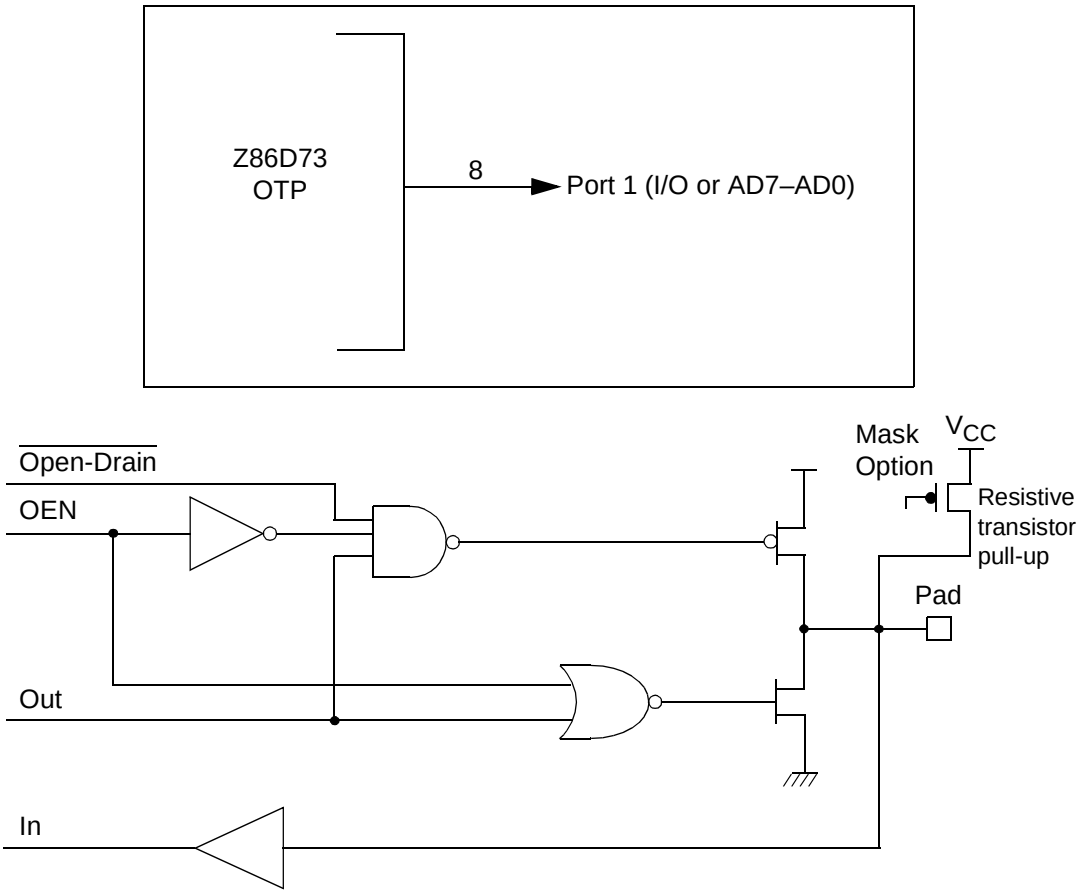


Figure 11. Port 1 Configuration

Stack

The Z86D73 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed

Table 10. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to its location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Therefore, reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

Example

When the status of bit 5 is 1, a timer reset condition occurs.

T8 Clock

This bit defines the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

Table 12. CTR(D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Initial_T16_Out/ Falling_Edge	-------0			**Transmit Mode**
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If the result is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/ Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the Ping-Pong mode or in independent normal operation mode. Setting this field to “Normal Operation Mode” terminates the “Ping-Pong Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This

ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register

Table 13 lists and briefly describes the fields for this register.

Table 13. CTR2 (D)02h: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		**Transmit Mode**
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Timeout
			1	Counter Timeout Occurred
		W	0	No Effect
			1	Reset Flag to 0

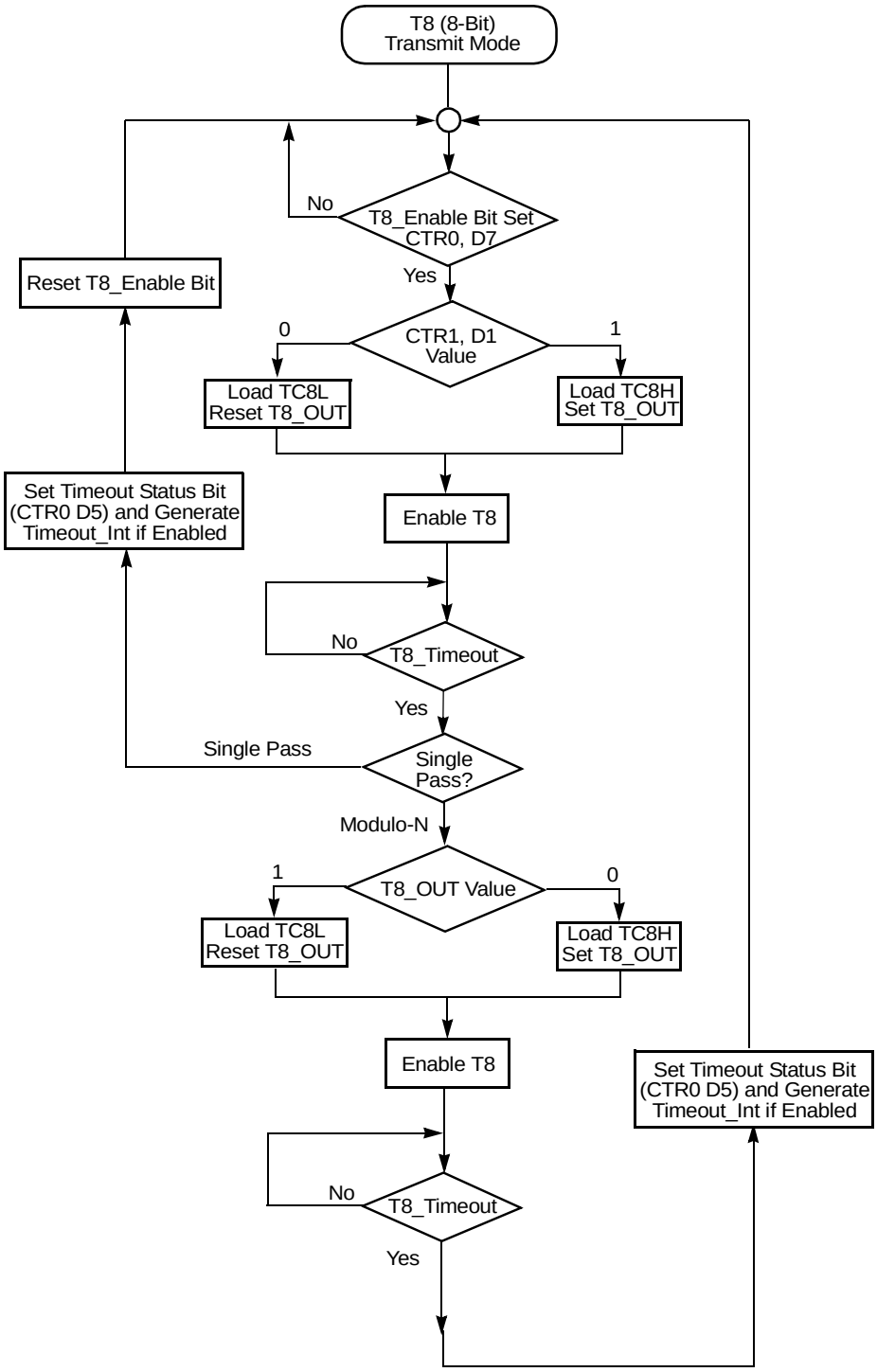


Figure 20. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In Single-Pass Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 21.

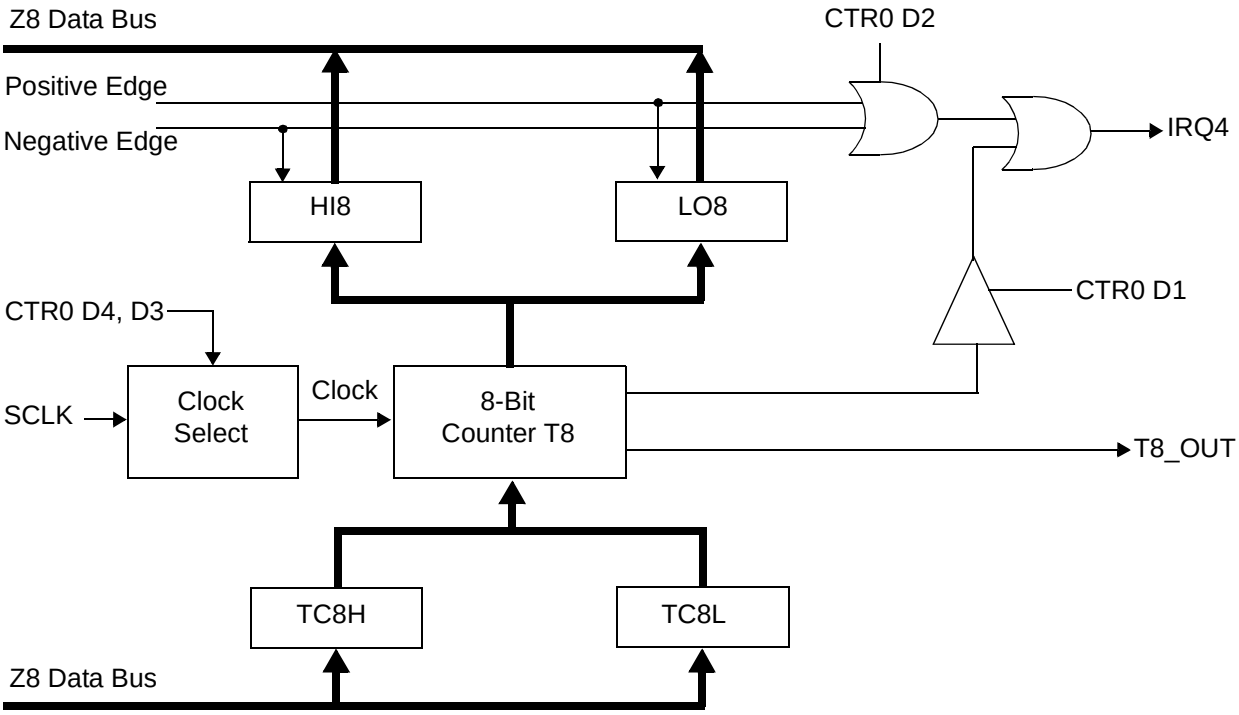


Figure 21. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: Do not write these registers at the time the values are to be loaded into the counter/timer to ensure known operation. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFh to FEh.

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation, thereby reducing the standby current to 10 µA or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR, or external reset. This condition causes the processor to restart the application program at address 000Ch. In order to enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Op Code = FFh) immediately before the appropriate sleep instruction, as follows:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
```

or

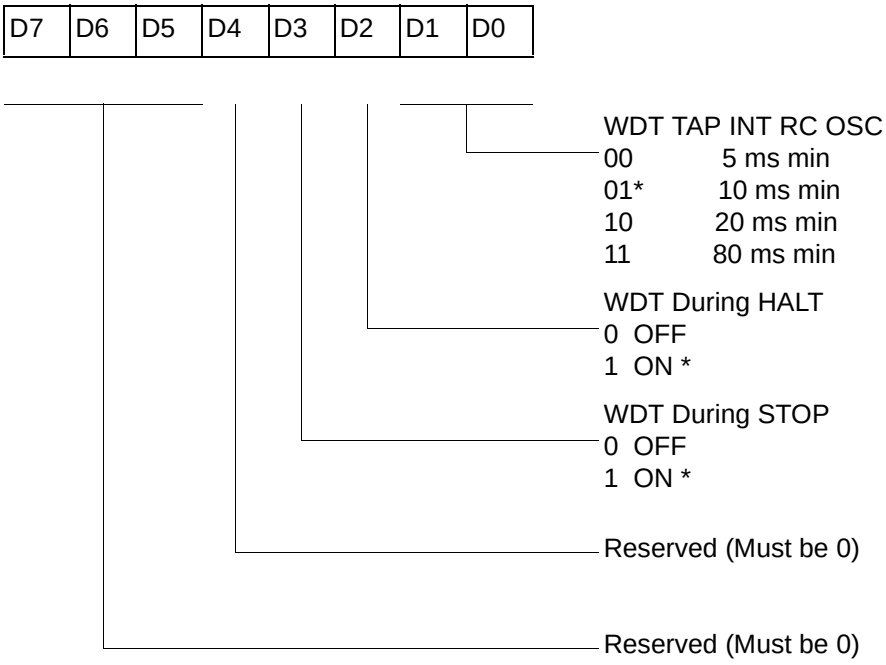
```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bits 0 and 1 control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 38). This register is accessible only during the first 61 processor cycles (122 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 37). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location `0Fh`. It is organized as shown in Figure 38.

WDTMR (0F) 0F



* Default setting after reset

Figure 38. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 18.

Table 18. WDT Time Select*

D1	D0	Timeout of Internal RC OSC	Timeout of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 Tpc
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Note:
***TpC = XTAL clock cycle. The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 39.

CTR1 (0D) 1H

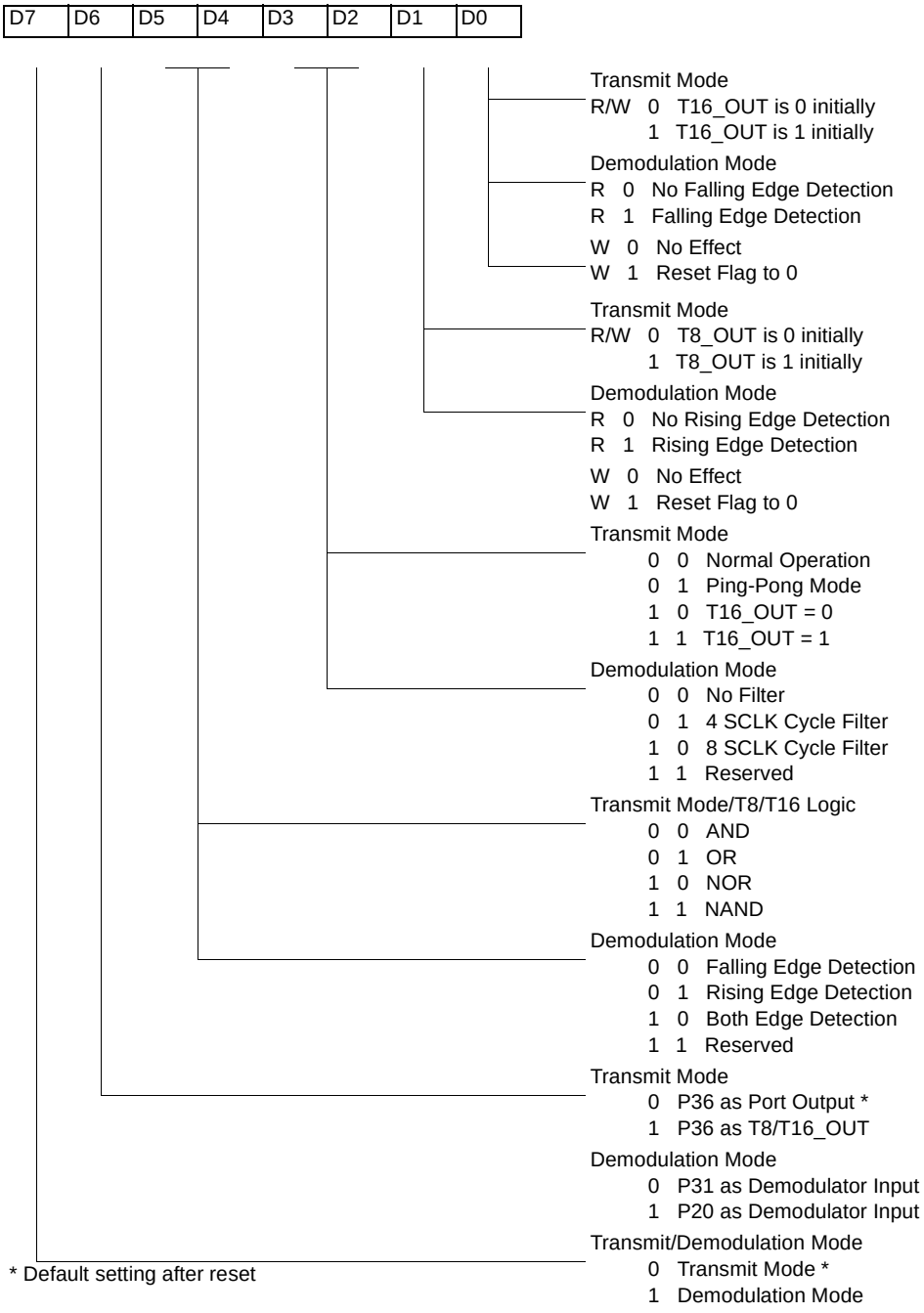


Figure 41. T8 and T16 Common Control Functions ((0D) 1h: Read/Write)

Notes: Care must be taken in differentiating Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be done without disabling the counter/timers.

CTR2 (0D) 02H

D7	D6	D5	D4	D3	D2	D1	D0

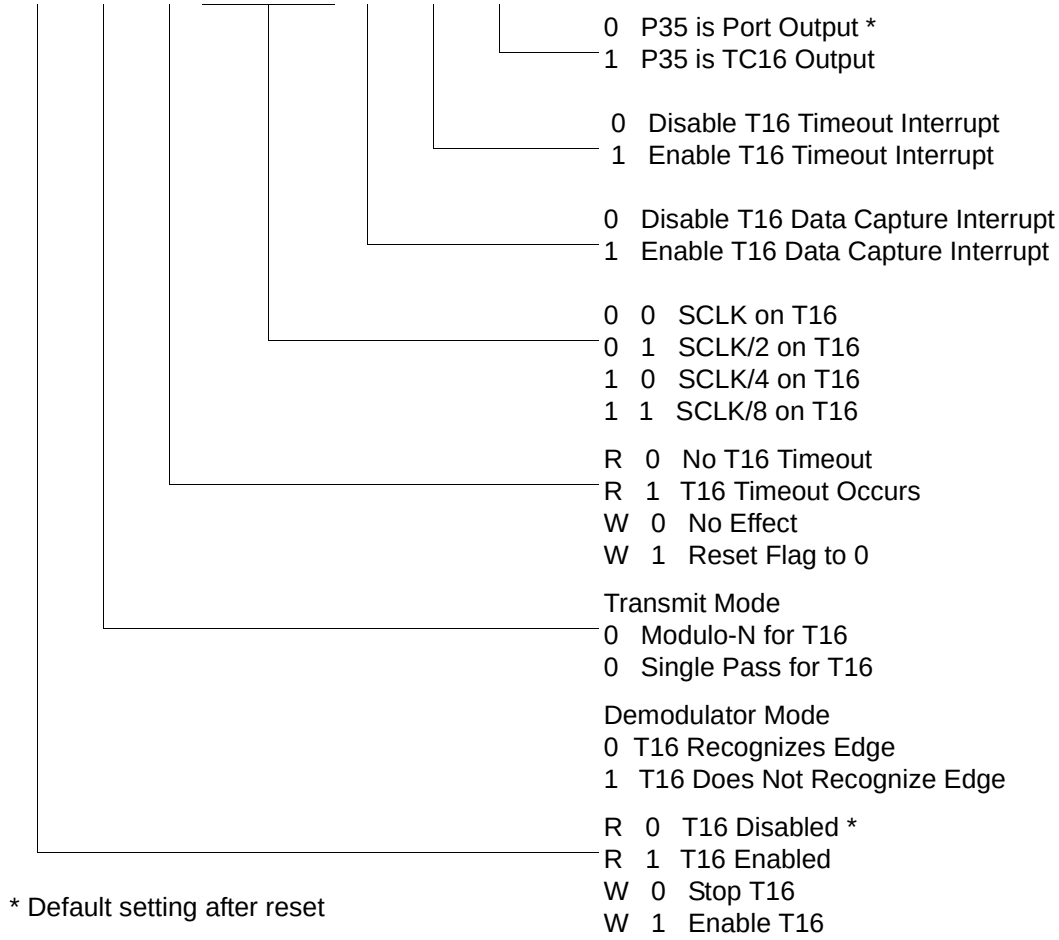
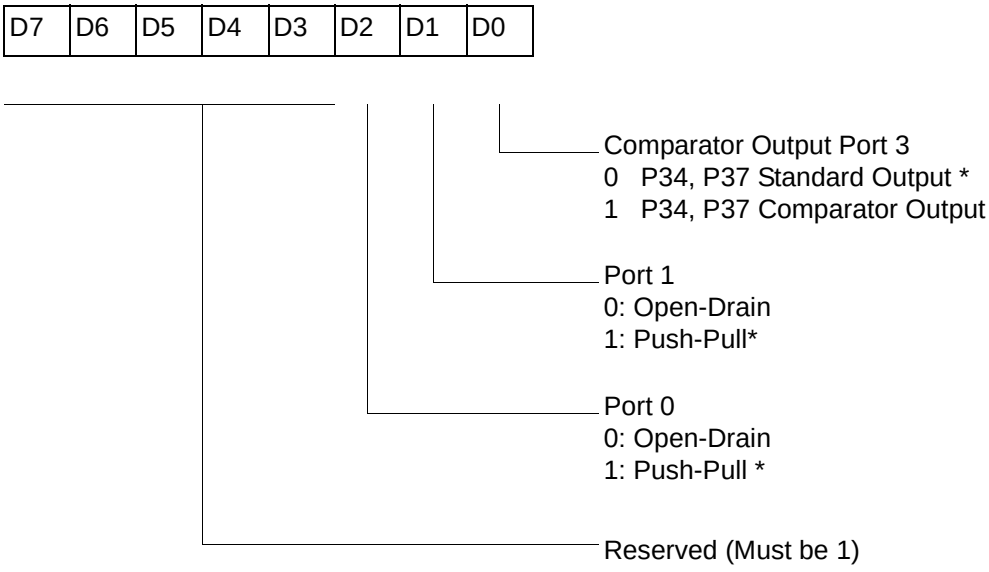


Figure 42. T16 Control Register ((0D) 2h: Read/Write Except Where Noted)

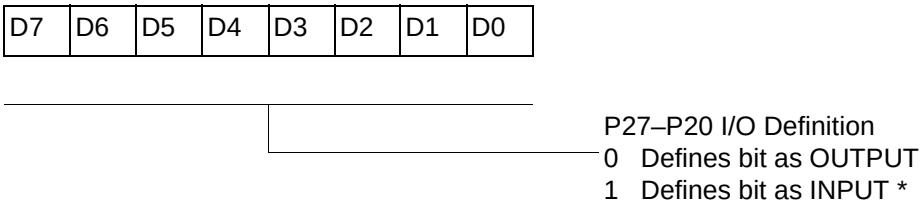
PCON (FH) 00H



* Default setting after reset

Figure 47. Port Configuration Register (PCON) ((0F) 0h: Write Only)

R246 P2M



* Default setting after reset

Figure 48. Port 2 Mode Register (F6h: Write Only)

R252 Flags

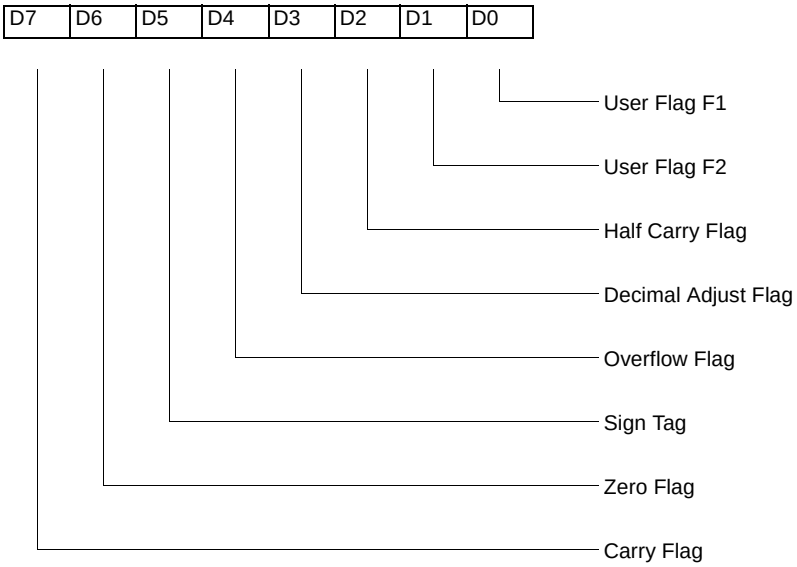
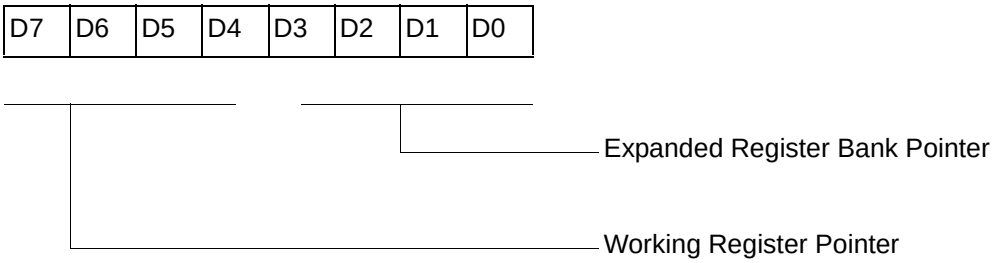


Figure 54. Flag Register (FCh: Read/Write)

R253 RP



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDh: Read/Write)