Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 10x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84766vlkr

- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.6 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.6.7 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 25 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.12 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.13 Phase-locked loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.14 Clock sources

1.6.14.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.14.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.15 Cyclic Redundancy Check (CRC) generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation

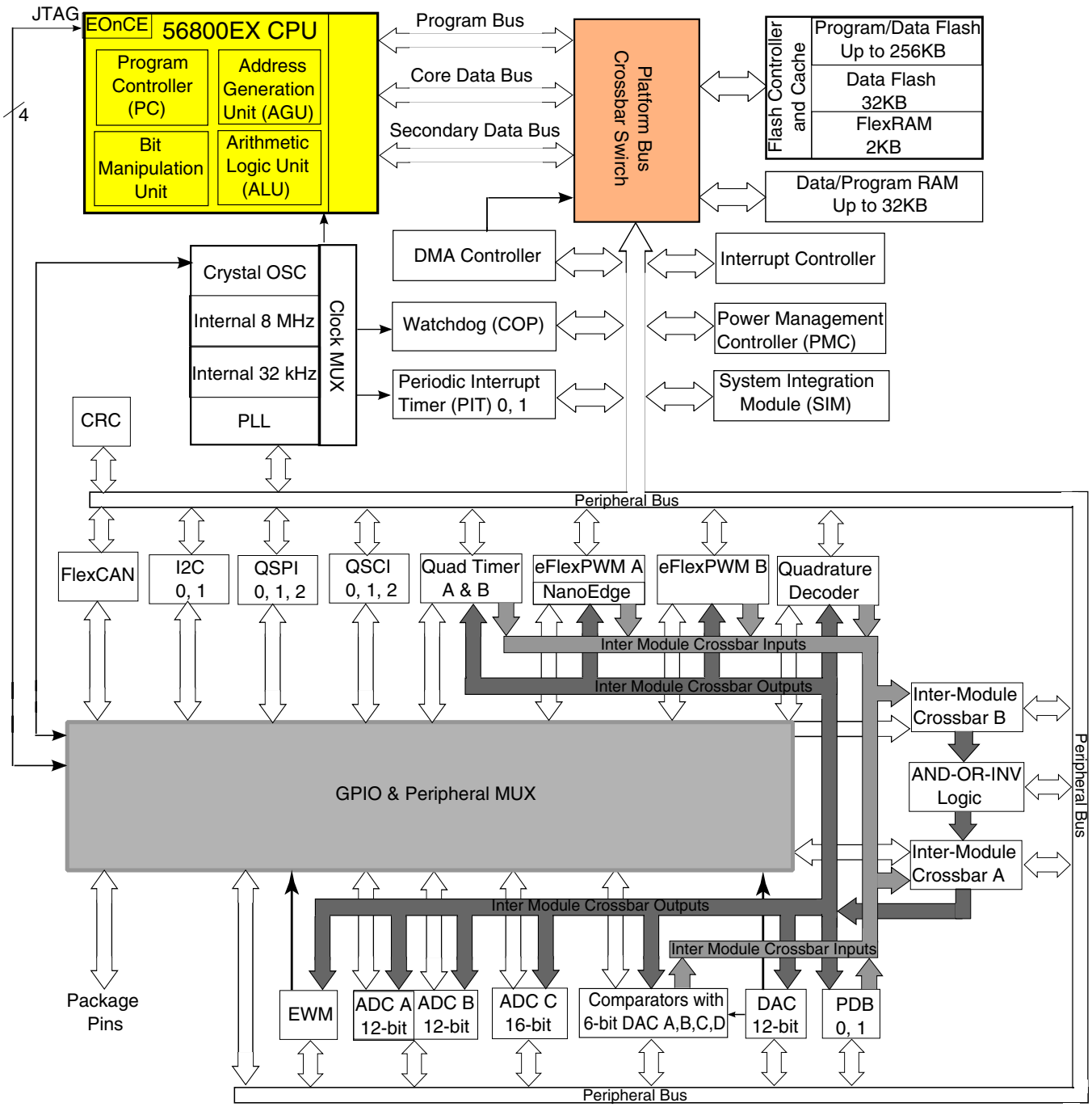


Figure 2. System diagram

Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
V_{CAP}	16	12	-	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
V_{CAP}	35	30	26			
V_{CAP}	93	73	57			
TDI	100	80	64	Input	Input, internal pullup enabled	Test Data Input — Provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/ Output	Input, internal pullup enabled	GPIO Port D0
TDO	98	78	62	Output	Output	Test Data Output — This tri-stateable pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO.
(GPIOD1)				Input/ Output	Input, internal pullup enabled	GPIO Port D1
TCK	1	1	1	Input	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK.
(GPIOD2)				Input/ Output	Input, internal pullup enabled	GPIO Port D2

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOA11	37	32	-	Input/ Output	Input	GPIO Port A11: After reset, the default state is GPIOA11.
(ANC19&VREFHC)				Input		ANC19 is input to channel 19 of ADCC. VREFHC is the analog reference high of ADCC.
GPIOB0	33	28	24	Input/ Output	Input	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)				Input		ANB0 is input to channel 0 of ADCB; CMPB_IN3 is input 3 of analog comparator B. When used as an analog input, the signal goes to both places (ANB0 and CMPB_IN3), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOB1	34	29	25	Input/ Output	Input	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)				Input		ANB1 is input to channel 1 of ADCB; CMPB_IN0 is input 0 of analog comparator B. When used as an analog input, the signal goes to both places (ANB1 and CMPB_IN0), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOB2	36	31	27	Input/ Output	Input	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VREFHB&CMPC_IN3)				Input		ANB2 is input to channel 2 of ADCB; VREFHB is the reference high of ADCB; CMPC_IN3 is input 3 of analog comparator C. When used as an analog input, the signal goes to both places (ANB2 and CMPC_IN3), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin. This input can be configured as either ANB2 or VREFHB using the ADCB control register.
GPIOB3	42	34	28	Input/ Output	Input	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB&CMPC_IN0)				Input		ANB3 is input to channel 3 of ADCB; VREFLB is the reference low of ADCB; CMPC_IN0 is input 0 of analog comparator C. When used as an analog input, the signal goes to both places (ANB3 and CMPC_IN0), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin. This input can be configured as either ANB3 or VREFLB using the ADCB control register.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOG7	92	72	-	Input/ Output	Input	GPIO Port G7: After reset, the default state is GPIOG7.
(PWMA_FAULT5)				Input		PWM module A fault input 5 is used for disabling selected PWM module A outputs in cases where fault conditions originate off-chip
(PWMB_FAULT5)				Input		PWM module B fault input 5 is used for disabling selected PWM module B outputs in cases where fault conditions originate off-chip
(XB_OUT9)				Output		Crossbar module output 9
GPIOG8	64	-	-	Input/ Output	Input	GPIO Port G8: After reset, the default state is GPIOG8.
(PWMB_0X)				Input/ Output		PWM module B, submodule 0, output X or input capture X
(PWMA_0X)				Input/ Output		PWM module A, submodule 0, output X or input capture X
(TA2)				Input/ Output		Quad timer module A channel 2 input/ output
(XB_OUT10)				Output		Crossbar module output 10
GPIOG9	65	-	-	Input/ Output	Input	GPIO Port G9: After reset, the default state is GPIOG9.
(PWMB_1X)				Input/ Output		PWM module B, submodule 1, output X or input capture X
(PWMA_1X)				Input/ Output		PWM module A, submodule 1, output X or input capture X
(TA3)				Input/ Output		Quad timer module A channel 3 input/ output
(XB_OUT11)				Output		Crossbar module output 11
GPIOG10	51	-	-	Input/ Output	Input	GPIO Port G10: After reset, the default state is GPIOG10.
(PWMB_2X)				Input/ Output		PWM module B, submodule 2, output X or input capture X
(PWMA_2X)				Input/ Output		PWM module A, submodule 2, output X or input capture X
(XB_IN8)				Input		Crossbar module input 8
(SS2_B)				Input/ Output		In slave mode, SS2_B indicates to the SPI2 module that the current transfer is to be received.

Table continues on the next page...

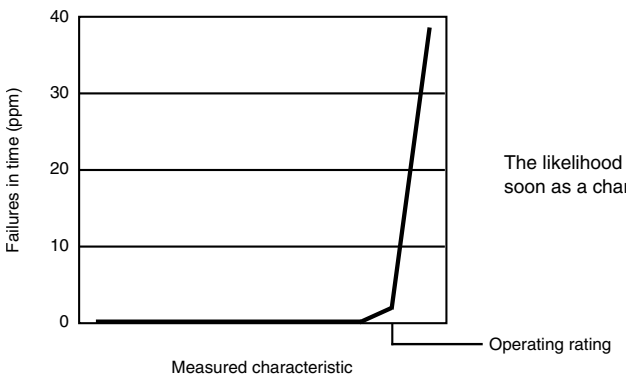
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

6.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

6.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.2 AC electrical characteristics

Tests are conducted using the input levels specified in Table 8. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

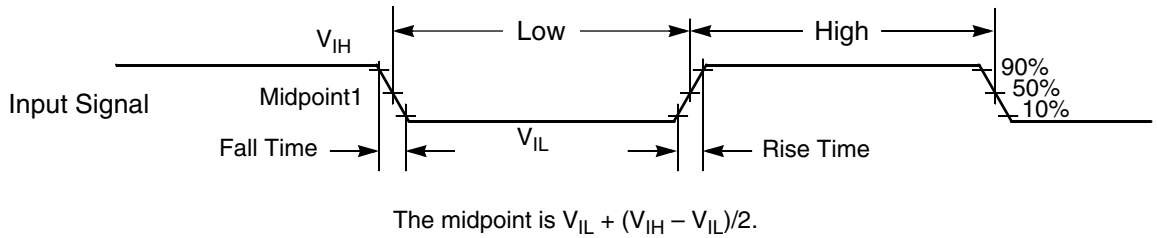


Figure 3. Input signal measurement references

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

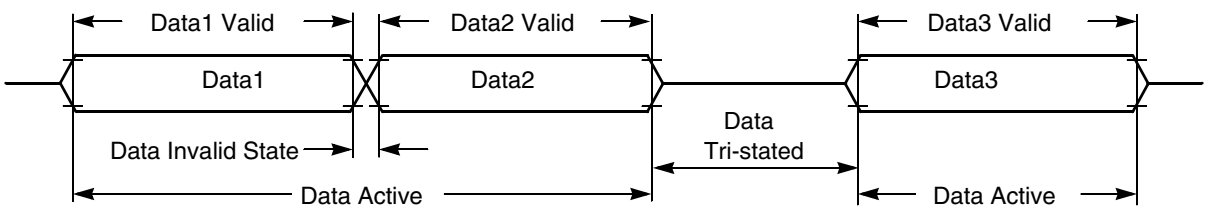


Figure 4. Signal states

8.3 Nonswitching electrical specifications

8.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V

Table continues on the next page...

NOTE

To filter noise on the RESETB pin, install a capacitor (up to 0.1 uF) on it.

Table 9. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

NOTE

In the Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 100MHz, T=10ns. At 4MHz (used coming out of reset and stop modes), T=250ns.

Table 10. Power-On-Reset mode transition times

Symbol	Description	Min	Max	Unit	Notes
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7V to when the first instruction executes (over the operating temperature range).	199	225	us	
	LPS mode to LPRUN mode	240	551	us	4
	VLPS mode to VLPRUN mode	1424	1500	us	5
	STOP mode to RUN mode	6.79	7.29	us	3
	WAIT mode to RUN mode	0.570	0.620	us	2
	VLPWAIT mode to VLPRUN mode	1413	1500	us	5
	LPWAIT mode to LPRUN mode	237.2	554	us	4

1. Normal boot (FTFL_OPT[LPBOOT]=1)
2. Clock configuration: CPU clock = 100 MHz, bus clock = 100 MHz, flash clock = 25 MHz
3. Clock configuration: CPU clock = 4 MHz, system clock source is 8 MHz IRC
4. CPU Clock = 200 kHz and 8 Mhz IRC in standby mode
5. Clock configuration: Using 64 kHz external clock source, CPU Clock = 32 kHz

8.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

8.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

8.4 Switching specifications

8.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{IPBUS}	IP bus clock	—	100	MHz	

8.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	3

Table continues on the next page...

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	40	49	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	44	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	34	43	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	24	35	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	12	17	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

Table 23. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

9.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					—
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	µs	1
$t_{rd1sec2k}$	Read 1s Section execution time (program flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					—
$t_{pgmsec512p}$	• 512 B program flash	—	2.4	—	ms	
$t_{pgmsec512d}$	• 512 B data flash	—	4.7	—	ms	
$t_{pgmsec1kp}$	• 1 KB program flash	—	4.7	—	ms	
$t_{pgmsec1kd}$	• 1 KB data flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	—
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	175	1500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					—
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	

Table continues on the next page...

Table 24. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set FlexRAM Function execution time:					—
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					—
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	—
	Word-write to FlexRAM execution time:					—
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	—
	Longword-write to FlexRAM execution time:					—
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

9.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

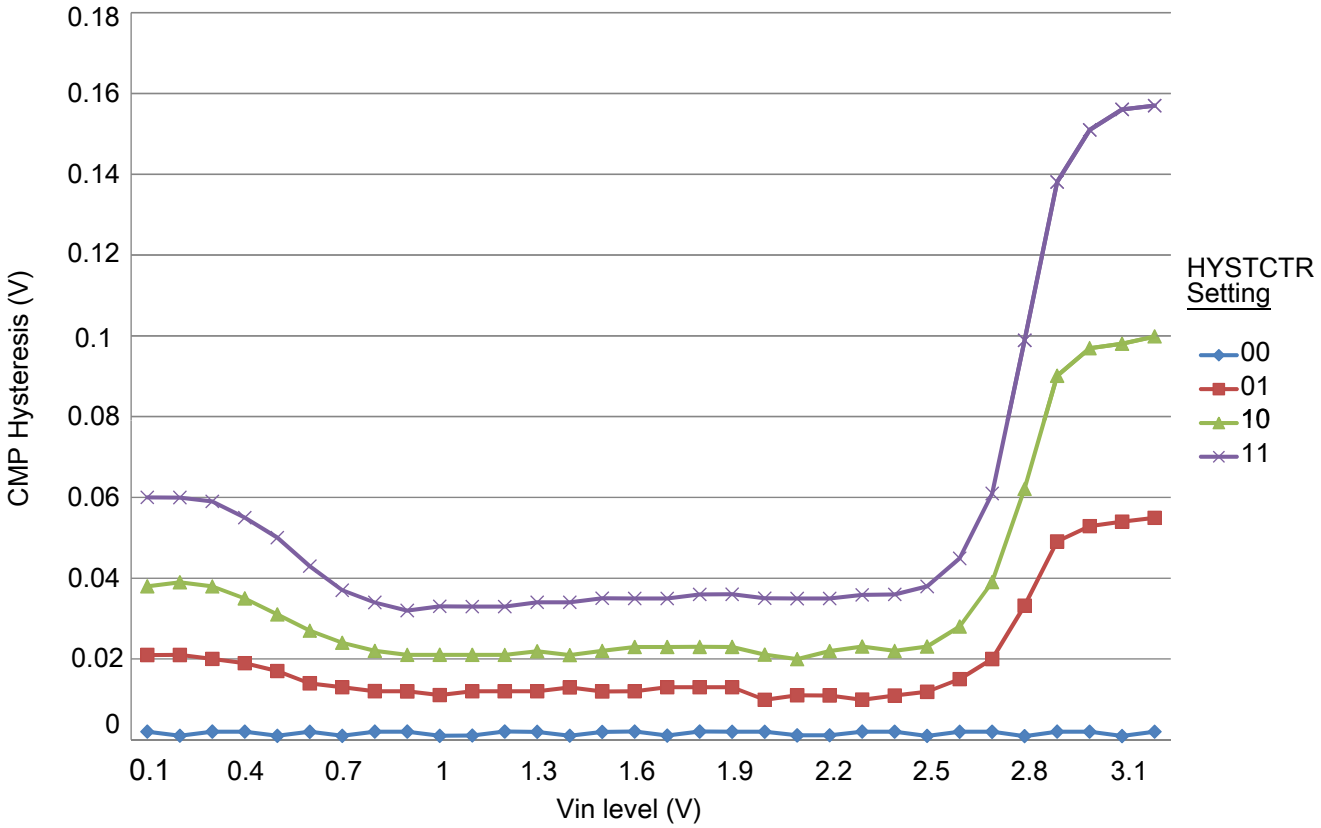


Figure 13. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

9.6 PWMs and timers

9.6.1 Enhanced NanoEdge PWM characteristics

Table 32. NanoEdge PWM timing parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency			100		MHz
NanoEdge Placement (NEP) Step Size[1, 2]	pwmp		312		ps
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

9.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

Table 33. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 14
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 14
Timer output period	P_{OUT}	20	—	ns	Figure 14
Timer output high/low period	P_{OUTHL}	10	—	ns	Figure 14

1. T = clock cycle. For 100 MHz operation, T = 10 ns.

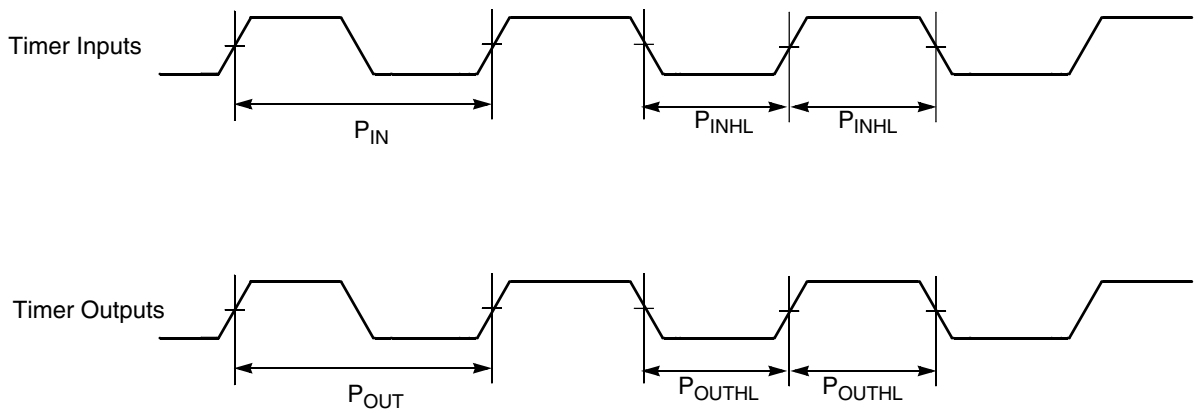


Figure 14. Timer timing

9.7 Communication interfaces

9.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 34. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time	t_C	35	—	ns	Figure 15
Master		35	—	ns	Figure 16
Slave					Figure 17
					Figure 18

Table continues on the next page...

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which TJ value is closer to the application depends on the power dissipated by other components on the board.

- The TJ value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The TJ value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

10.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

11 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23174W
100-pin LQFP	98ASS23308W

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
22	17	13	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
23	18	14	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
24	19	15	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
25	20	16	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
26	21	17	GPIOB7	GPIOB7	ANB7&ANC15&CMPB_IN2			
27	22	18	GPIOC5	GPIOC5	DACO	XB_IN7		
28	23	19	GPIOB6	GPIOB6	ANB6&ANC14&CMPB_IN1			
29	24	20	GPIOB5	GPIOB5	ANB5&ANC13&CMPC_IN2			
30	25	21	GPIOB4	GPIOB4	ANB4&ANC12&CMPC_IN1			
31	26	22	VDDA	VDDA				
32	27	23	VSSA	VSSA				
33	28	24	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
34	29	25	GPIOB1	GPIOB1	ANB1&CMPB_IN0			
35	30	26	VCAP	VCAP				
36	31	27	GPIOB2	GPIOB2	ANB2&VREFHB&CMPC_IN3			
37	32	—	GPIOA11	GPIOA11	ANC19&VREFHC			
38	33	—	GPIOB8	GPIOB8	ANC20&VREFLC			
39	—	—	GPIOB9	GPIOB9	ANC21	XB_IN9	MISO2	
40	—	—	GPIOB10	GPIOB10	ANC22	XB_IN8	MOSI2	
41	—	—	GPIOB11	GPIOB11	ANC23	XB_IN7	SCLK2	
42	34	28	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
43	35	29	VDD	VDD				
44	36	30	VSS	VSS				
45	—	—	GPIOF11	GPIOF11	TXD0	XB_IN11		
46	—	—	GPIOF15	GPIOF15	RXD0	XB_IN10		
47	37	—	GPIOD7	GPIOD7	XB_OUT11	XB_IN7	MISO1	
48	38	—	GPIOG11	GPIOG11	TB3	CLKO0	MOSI1	
49	39	31	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	
50	40	32	GPIOC7	GPIOC7	SS0_B	TXD0		
51	—	—	GPIOG10	GPIOG10	PWMB_2X	PWMA_2X	XB_IN8	SS2_B
52	41	33	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
53	42	34	GPIOC9	GPIOC9	SCLK0	XB_IN4		
54	43	35	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	
55	44	36	GPIOF0	GPIOF0	XB_IN6	TB2	SCLK1	
56	45	—	GPIOF10	GPIOF10	TXD2	PWMA_FAULT6	PWMB_FAULT6	XB_OUT10
57	46	—	GPIOF9	GPIOF9	RXD2	PWMA_FAULT7	PWMB_FAULT7	XB_OUT11
58	47	37	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
59	48	38	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	

13 Product documentation

The documents listed in Table 38 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at **freescale.com**.

Table 38. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F847xx Reference Manual	Detailed functional description and programming model	MC56F847XXRM
MC56F847xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F847XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

14 Revision history

The following table summarizes changes to this document since the release of the previous version.

Table 39. Revision history

Rev.	Date	Substantial Changes

3.1	06/2014	Changes include:
		• Updates and corrections to "56F844xx/5xx/7xx family" table.
		• In "Signal groups" section, in "Functional Group Pin Allocations" table, made corrections to "Functional Group Pin Allocations" table.
		• For "Power mode transition operating behaviors" section,
		  • Changed the name to "Power mode operating behaviors".
		• In "Power consumption operating behaviors" section, updated mode currrent values in "Current Consumption" table.
		• In "Memories and memory interfaces" section,
		  • "Flash Memory Characteristics" section is now called "Flash electrical specifications" section.
		  • Added new section "Flash timing specifications — program and erase", where the "Flash Timing Parameters" table (now called "NVM program/erase timing specifications" table, and table was updated.
		  • Added new section "Flash high voltage current behaviors".
		• In "Pinout" section, in "Signal Multiplexing and Pin Assignments" section,
		  • Added 3 notes.
		  • In pin mux table, changed SCK0 to SCLK0, SCK1 to SCLK1, updates to 64LQFP[62-64] and 48LQFP[46-48].
		  • In "64-pin LQFP" figure, made updates to pins 62-64, and added a note.