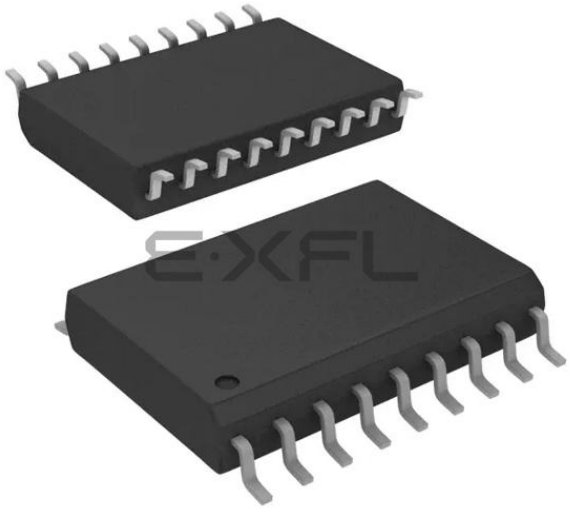

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Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	M8B
Program Memory Type	OTP (3kB)
Controller Series	CY7C632xx
RAM Size	96 x 8
Interface	USB
Number of I/O	10
Voltage - Supply	3.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c63231a-sxc

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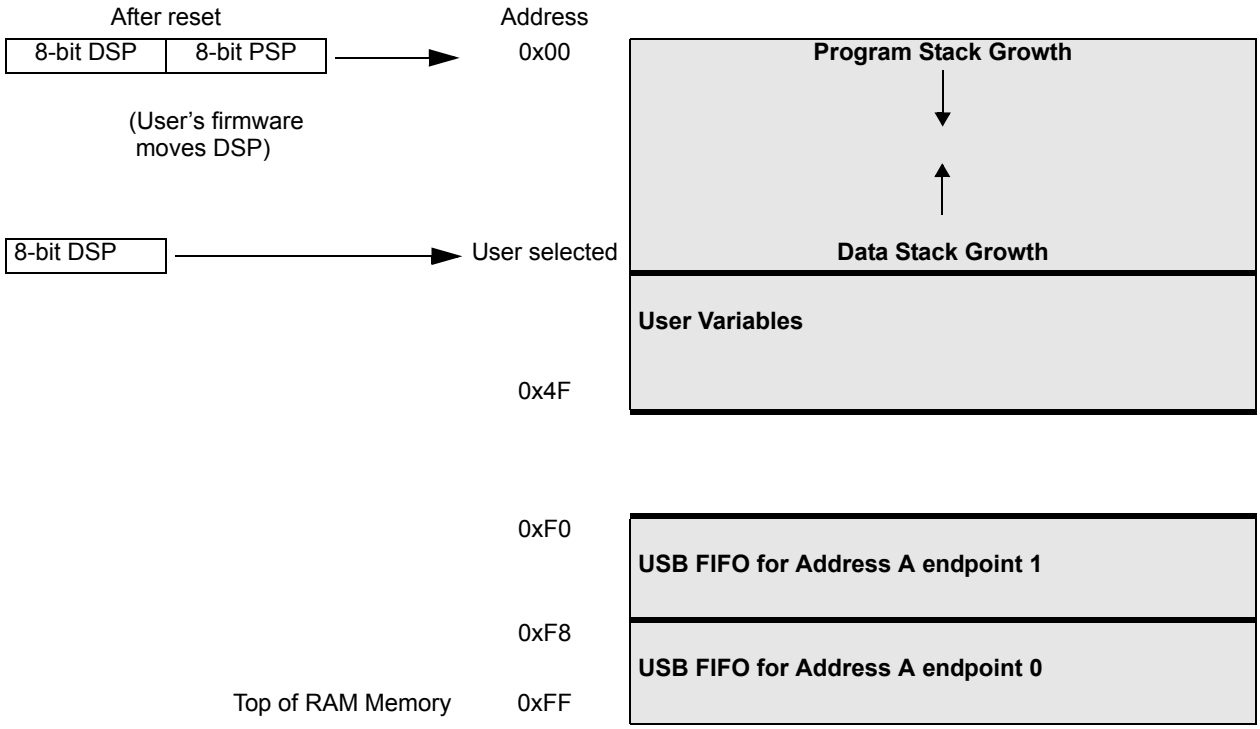
8.2 Data Memory Organization

The microcontroller provides 96 bytes of data RAM. In normal usage, the SRAM is partitioned into four areas: program stack, data stack, user variables and USB endpoint FIFOs as shown below:



execution begins from address 0x0000 after this t_{START} delay period. This provides time for V_{CC} to stabilize before the part executes code. See Section 10.1 for more details.

1 = Disables the LVR circuit.

0 = Enables the LVR circuit.

Bit 2: Precision USB Clocking Enable

The Precision USB Clocking Enable only affects operation in internal oscillator mode. **In that mode, this bit must be set to 1 to cause the internal clock to automatically precisely tune to USB timing requirements (6 MHz ±1.5%)**. The frequency may have a looser initial tolerance at power-up, but all USB transmissions from the chip will meet the USB specification.

1 = Enabled. The internal clock accuracy is **6 MHz ±1.5%** after USB traffic is received**.**

0 = Disabled. The internal clock accuracy is 6 MHz ±5%.

Bit 1: Internal Clock Output Disable

The Internal Clock Output Disable is used to keep the internal clock from driving out to the XTALOUT pin. This bit has no effect in the external oscillator mode.

1 = Disable internal clock output. XTALOUT pin will drive HIGH.

0 = Enable the internal clock output. The internal clock is driven out to the XTALOUT pin.

Bit 0: External Oscillator Enable

At power-up, the chip operates from the internal clock by default. Setting the External Oscillator Enable bit HIGH disables the internal clock, and halts the part while the external resonator/crystal oscillator is started. Clearing this bit has no immediate effect, although the state of this bit is used when waking out of suspend mode to select between internal and external clock. In internal clock mode, XTALIN pin will be configured as an input with a weak pull-down and can be used as a GPIO input (P2.1).

1 = Enable the external oscillator. The clock is switched to external clock mode, as described in Section 9.1.

0 = Enable the internal oscillator.

9.1 Internal/External Oscillator Operation

The internal oscillator provides an operating clock, factory set to a nominal frequency of 6 MHz. This clock requires no external components. At power-up, the chip operates from the internal clock. In this mode, the internal clock is buffered and driven to the XTALOUT pin by default, and the state of the XTALIN pin can be read at Port 2.1. While the internal clock is enabled, its output can be disabled at the XTALOUT pin by setting the Internal Clock Output Disable bit of the Clock Configuration Register.

Setting the External Oscillator Enable bit of the Clock Configuration Register HIGH disables the internal clock, and halts the part while the external resonator/crystal oscillator is started. The steps involved in switching from Internal to External Clock mode are as follows:

1. At reset, chip begins operation using the internal clock.
2. Firmware sets Bit 0 of the Clock Configuration Register. For example,

```
mov A, 1h       ; Set Bit 0 HIGH (External Oscillator Enable bit). Bit 7 cleared gives faster start-up
iowr F8h        ; Write to Clock Configuration Register
```

3. Internal clocking is halted, the internal oscillator is disabled, and the external clock oscillator is enabled.
4. After the external clock becomes stable, chip clocks are re-enabled using the external clock signal. (Note that the time for the external clock to become stable depends on the external resonating device; see next section.)
5. After an additional delay the CPU is released to run. This delay depends on the state of the Ext. Clock Resume Delay bit of the Clock Configuration Register. The time is 128 μs if the bit is 0, or 4 ms if the bit is 1.
6. Once the chip has been set to external oscillator, it can only return to internal clock when waking from suspend mode. Clearing bit 0 of the Clock Configuration Register will not re-enable internal clock mode until suspend mode is entered. See Section 11.0 for more details on suspend mode operation.

If the Internal Clock is enabled, the XTALIN pin can serve as a general-purpose input, and its state can be read at Port 2, Bit 1 (P2.1). Refer to *Figure 12-8* for the Port 2 Data Register. In this mode, there is a weak pull-down at the XTALIN pin. This input cannot provide an interrupt source to the CPU.

9.2 External Oscillator

The user can connect a low-cost ceramic resonator or an external oscillator to the XTALIN/XTALOUT pins to provide a precise reference frequency for the chip clock, as shown in *Figure 9-1*. The external components required are a ceramic resonator or crystal and any associated capacitors. To run from the external resonator, the External Oscillator Enable bit of the Clock Configuration Register must be set to 1, as explained in the previous section.

10.3 Watchdog Reset (WDR)

The Watchdog Timer Reset (WDR) occurs when the internal Watchdog timer rolls over. Writing any value to the write-only Watchdog Reset Register at address 0x26 will clear the timer. The timer will roll over and WDR will occur if it is not cleared within t_{WATCH} (see *Figure 10-1*) of the last clear. Bit 6 (Watchdog Reset bit) of the Processor Status and Control Register is set to record this event (see Section 18.0 for more details). A Watchdog Timer Reset lasts for typically 2–4 ms after which the microcontroller begins execution at ROM address 0x0000.

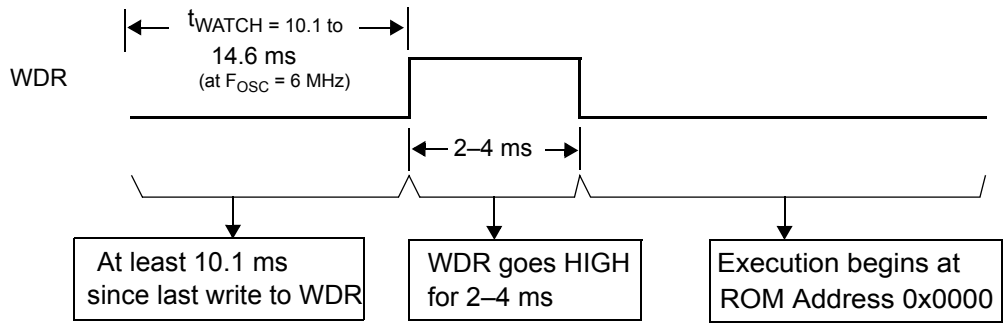


Figure 10-1. Watchdog Reset (WDR, Address 0x26)

11.0 Suspend Mode

The parts support a versatile low-power suspend mode. In suspend mode, only an enabled interrupt or a LOW state on the D–/SDATA pin will wake the part. Two options are available. For lowest power, all internal circuits can be disabled, so only an external event will resume operation. Alternatively, a low-power internal wake-up timer can be used to trigger the wake-up interrupt. This timer is described in Section 11.2, and can be used to periodically poll the system to check for changes, such as looking for movement in a mouse, while maintaining a low average power.

The is placed into a low-power state by setting the Suspend bit of the Processor Status and Control Register (*Figure 18-1*). All logic blocks in the device are turned off except the GPIO interrupt logic, the D–/SDATA pin input receiver, and (optionally) the wake-up timer. The clock oscillators, as well as the free-running and watchdog timers are shut down. Only the occurrence of an enabled GPIO interrupt, wake-up interrupt, SPI slave interrupt, or a LOW state on the D–/SDATA pin will wake the part from suspend (D– LOW indicates non-idle USB activity). Once one of these resuming conditions occurs, clocks will be restarted and the device returns to full operation after the oscillator is stable and the selected delay period expires. This delay period is determined by selection of internal vs. external clock, and by the state of the Ext. Clock Resume Delay as explained in Section 9.0.

In suspend mode, any enabled and pending interrupt will wake the part up. The state of the Interrupt Enable Sense bit (Bit 2, *Figure 18-1*) does not have any effect. As a result, any interrupts not intended for waking from suspend should be disabled through the Global Interrupt Enable Register and the USB End Point Interrupt Enable Register (Section 19.0).

If a resuming condition exists when the suspend bit is set, the part will still go into suspend and then awake after the appropriate delay time. The Run bit in the Processor Status and Control Register must be set for the part to resume out of suspend.

Once the clock is stable and the delay time has expired, the microcontroller will execute the instruction following the I/O write that placed the device into suspend mode before servicing any interrupt requests.

To achieve the lowest possible current during suspend mode, all I/O should be held at either V_{CC} or ground. In addition, the GPIO *bit* interrupts (*Figure 19-4* and *Figure 19-5*) should be disabled for any pins that are not being used for a wake-up interrupt. This should be done even if the main GPIO Interrupt Enable (*Figure 19-1*) is off.

Typical code for entering suspend is shown below:

```
...         ; All GPIO set to low-power state (no floating pins, and bit interrupts disabled unless using for wake-up)
...         ; Enable GPIO and/or wake-up timer interrupts if desired for wake-up
...         ; Select clock mode for wake-up (see Section 11.1)
mov a, 09h  ; Set suspend and run bits
iowr FFh    ; Write to Status and Control Register - Enter suspend, wait for GPIO/wake-up interrupt or USB activity
nop         ; This executes before any ISR
...         ; Remaining code for exiting suspend routine
```

11.1 Clocking Mode on Wake-up from Suspend

When exiting suspend on a wake-up event, the device can be configured to run in either Internal or External Clock mode. The mode is selected by the state of the External Oscillator Enable bit in the Clock Configuration Register (*Figure 9-2*). Using the

Bit #	7	6	5	4	3	2	1	0
Bit Name	Reserved						P1[1:0]	
Notes							Pins 1:0 in all parts	
Read/Write	-	-	-	-	-	-	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Figure 12-3. Port 1 Data (Address 0x01)

Bit [7:2]: Reserved

Bit [1:0]: P1[1:0]

1 = Port Pin is logic HIGH

0 = Port Pin is logic LOW

Bit #	7	6	5	4	3	2	1	0
Bit Name	P0[7:0] Mode0							
Read/Write	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Figure 12-4. GPIO Port 0 Mode0 Register (Address 0x0A)

Bit [7:0]: P0[7:0] Mode 0

1 = Port Pin Mode 0 is logic HIGH

0 = Port Pin Mode 0 is logic LOW

Bit #	7	6	5	4	3	2	1	0
Bit Name	P0[7:0] Mode1							
Read/Write	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Figure 12-5. GPIO Port 0 Mode1 Register (Address 0x0B)

Bit [7:0]: P0[7:0] Mode 1

1 = Port Pin Mode 1 is logic HIGH

0 = Port Pin Mode 1 is logic LOW

Bit #	7	6	5	4	3	2	1	0
Bit Name	Reserved						P1[1:0] Mode0	
Read/Write	-	-	-	-	-	-	W	W
Reset	0	0	0	0	0	0	0	0

Figure 12-6. GPIO Port 1 Mode0 Register (Address 0x0C)

Bit [7:2]: Reserved

Bit [1:0]: P1[1:0] Mode 0

1 = Port Pin Mode 0 is logic HIGH

0 = Port Pin Mode 0 is logic LOW

Bit #	7	6	5	4	3	2	1	0
Bit Name	Reserved		D+ (SCLK) State	D– (SDATA) State	Reserved	P2.2 (Internal Clock Mode Only)	P2.1 (Internal Clock Mode Only)	P2.0 VREG Pin State
Read/Write	-	-	R	R	-	R	R	R
Reset	0	0	0	0	0	0	0	0

Figure 12-8. Port 2 Data Register (Address 0x02)

Bit [7:6]: Reserved

Bit [5:4]: D+ (SCLK) and D- (SDATA) States

The state of the D+ and D– pins can be read at Port 2 Data Register. Performing a read from the port pins returns their logic values.

1 = Port Pin is logic HIGH

0 = Port Pin is logic LOW

Bit 3: Reserved

Bit 2: P2.2 (Internal Clock Mode Only)

In the Internal Clock mode, the XTALOUT pin can serve as a general purpose input, and its state can be read at Port 2, Bit 2 (P2.2). See Section 9.1 for more details.

1 = Port Pin is logic HIGH

0 = Port Pin is logic LOW

Bit 1: P2.1 (Internal Clock Mode Only)

In the Internal Clock mode, the XTALIN pin can serve as a general purpose input, and its state can be read at Port 2, Bit 1 (P2.1). See Section 9.1 for more details.

1 = Port Pin is logic HIGH

0 = Port Pin is logic LOW

Bit 0: P2.0/ VREG Pin State

In PS/2 mode, the VREG pin can be used as an input and its state can be read at port P2.0. Section 15.0 for more details.

1 = Port Pin is logic HIGH

0 = Port Pin is logic LOW

13.0 USB Serial Interface Engine (SIE)

The SIE allows the microcontroller to communicate with the USB host. The SIE simplifies the interface between the microcontroller and USB by incorporating hardware that handles the following USB bus activity independently of the microcontroller:

- Translate the encoded received data and format the data to be transmitted on the bus.
- CRC checking and generation. Flag the microcontroller if errors exist during transmission.
- Address checking. Ignore the transactions not addressed to the device.
- Send appropriate ACK/NAK/STALL handshakes.
- Token type identification (SETUP, IN, or OUT). Set the appropriate token bit once a valid token is received.
- Place valid received data in the appropriate endpoint FIFOs.
- Send and update the data toggle bit (Data1/0).
- Bit stuffing/unstuffing.

Firmware is required to handle the rest of the USB interface with the following tasks:

- Coordinate enumeration by decoding USB device requests.
- Fill and empty the FIFOs.
- Suspend/Resume coordination.
- Verify and select Data toggle values.

13.1 USB Enumeration

A typical USB enumeration sequence is shown below. In this description, 'Firmware' refers to embedded firmware in the controller.

1. The host computer sends a SETUP packet followed by a DATA packet to USB address 0 requesting the Device descriptor.
2. Firmware decodes the request and retrieves its Device descriptor from the program memory tables.
3. The host computer performs a control read sequence and Firmware responds by sending the Device descriptor over the USB bus, via the on-chip FIFO.
4. After receiving the descriptor, the host sends a SETUP packet followed by a DATA packet to address 0 assigning a new USB address to the device.
5. Firmware stores the new address in its USB Device Address Register after the no-data control sequence completes.
6. The host sends a request for the Device descriptor using the new USB address.
7. Firmware decodes the request and retrieves the Device descriptor from program memory tables.
8. The host performs a control read sequence and Firmware responds by sending its Device descriptor over the USB bus.
9. The host generates control reads from the device to request the Configuration and Report descriptors.
10. Once the device receives a Set Configuration request, its functions may now be used.
11. Firmware should take appropriate action for Endpoint 1 transactions, which may occur from this point.

13.2 USB Port Status and Control

USB status and control is regulated by the USB Status and Control Register as shown in *Figure 13-1*.

Bit #	7	6	5	4	3	2	1	0
Bit Name	PS/2 Pull-up Enable	VREG Enable	USB Reset-PS/2 Activity Interrupt Mode	Reserved	USB Bus Activity	D+/D- Forcing Bit		
Read/Write	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Figure 13-1. USB Status and Control Register (Address 0x1F)

Bit 7: PS/2 Pull-up Enable

This bit is used to enable the internal PS/2 pull-up resistors on the SDATA and SCLK pins. Normally the output high level on these pins is V_{CC}, but note that the output will be clamped to approximately 1 Volt above V_{REG} if the VREG Enable bit is set, or if the Device Address is enabled (bit 7 of the USB Device Address Register, *Figure 14-1*).

1 = Enable PS/2 pull-up resistors. The SDATA and SCLK pins are pulled up internally to V_{CC} with two resistors of approximately 5 kΩ (see Section 23.0 for the value of R_{PS2}).

0 = Disable PS/2 pull-up resistors.

Bit 6: VREG Enable

A 3.3V voltage regulator is integrated on chip to provide a voltage source for a 1.5-kΩ pull-up resistor connected to the D– pin as required by the USB Specification. Note that the VREG output has an internal series resistance of approximately 200Ω, the external pull-up resistor required is approximately 1.3-kΩ (see *Figure 16-1*).

1 = Enable the 3.3V output voltage on the VREG pin.

0 = Disable. The VREG pin can be configured as an input.

Bit 5: USB-PS/2 Interrupt Select

This bit allows the user to select whether an USB bus reset interrupt or a PS/2 activity interrupt will be generated when the interrupt conditions are detected.

1 = PS/2 interrupt mode. A PS/2 activity interrupt will occur if the SDATA pin is continuously LOW for 128 to 256 μs.

0 = USB interrupt mode (default state). In this mode, a USB bus reset interrupt will occur if the single ended zero (SE0, D– and D+ are LOW) exists for 128 to 256 μs.

See Section 19.0 for more details.

Bit 4: Reserved. Must be written as a '0'.

Bit 3: USB Bus Activity

The Bus Activity bit is a “sticky” bit that detects any non-idle USB event has occurred on the USB bus. Once set to HIGH by the SIE to indicate the bus activity, this bit retains its logical HIGH value until firmware clears it. Writing a ‘0’ to this bit clears it; writing a ‘1’ preserves its value. The user firmware should check and clear this bit periodically to detect any loss of bus activity. Firmware can clear the Bus Activity bit, but only the SIE can set it. The 1.024-ms timer interrupt service routine is normally used to check and clear the Bus Activity bit.

1 = There has been bus activity since the last time this bit was cleared. This bit is set by the SIE.

0 = No bus activity since last time this bit was cleared (by firmware).

Bit [2:0]: D+/D– Forcing Bit [2:0]

Forcing bits allow firmware to directly drive the D+ and D– pins, as shown in *Table 13-1*. Outputs are driven with controlled edge rates in these modes for low EMI. For forcing the D+ and D– pins in USB mode, D+/D– Forcing Bit 2 should be 0. Setting D+/D– Forcing Bit 2 to ‘1’ puts both pins in an open-drain mode, preferred for applications such as PS/2 or LED driving.

Table 13-1. Control Modes to Force D+/D– Outputs

D+/D– Forcing Bit [2:0]	Control Action	Application
000	Not forcing (SIE controls driver)	Any Mode
001	Force K (D+ HIGH, D– LOW)	USB Mode
010	Force J (D+ LOW, D– HIGH)	
011	Force SE0 (D– LOW, D+ LOW)	
100	Force D– LOW, D+ LOW	PS/2 Mode[2]
101	Force D– LOW, D+ HiZ	
110	Force D– HiZ, D+ LOW	
111	Force D– HiZ, D+ HiZ	

Note:
2. For PS/2 operation, the D+/D- Forcing Bit [2:0] = 111b mode must be set initially (one time only) before using the other PS/2 force modes.

14.0 USB Device

The supports one USB Device Address with two endpoints: EP0 and EP1.

14.1 USB Address Register

The USB Device Address Register contains a 7-bit USB address and one bit to enable USB communication. This register is cleared during a reset, setting the USB device address to zero and marking this address as disabled. *Figure 14-1* shows the format of the USB Address Register.

Bit #	7	6	5	4	3	2	1	0
Bit Name	Device Address Enable	Device Address Bit						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Figure 14-1. USB Device Address Register (Address 0x10)

In either USB or PS/2 mode, this register is cleared by both hardware resets and the USB bus reset. See Section 19.3 for more information on the USB Bus Reset - PS/2 interrupt.

Bit 7: Device Address Enable

This bit must be enabled by firmware before the serial interface engine (SIE) will respond to USB traffic at the address specified in Bit [6:0].

1 = Enable USB device address.

0 = Disable USB device address.

Bit [6:0]: Device Address Bit[6:0]

These bits must be set by firmware during the USB enumeration process (i.e., SetAddress) to the non-zero address assigned by the USB host.

14.2 USB Control Endpoint

All USB devices are required to have an endpoint number 0 (EP0) that is used to initialize and control the USB device. EP0 provides access to the device configuration information and allows generic USB status and control accesses. EP0 is bidirectional, as the device can both receive and transmit data. EP0 uses an 8-byte FIFO at SRAM locations 0xF8-0xFF, as shown in Section 8.2.

The EP0 endpoint mode register uses the format shown in *Figure 14-2*.

Bit #	7	6	5	4	3	2	1	0
Bit Name	SETUP Received	IN Received	OUT Received	ACKed Transaction	Mode Bit			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Figure 14-2. Endpoint 0 Mode Register (Address 0x12)

The SIE provides a locking feature to prevent firmware from overwriting bits in the USB Endpoint 0 Mode Register. Writes to the register have no effect from the point that Bit[6:0] of the register are updated (by the SIE) until the firmware reads this register. The CPU can unlock this register by reading it.

Because of these hardware-locking features, firmware should perform an read after a write to the USB Endpoint 0 Mode Register and USB Endpoint 0 Count Register (*Figure 14-4*) to verify that the contents have changed as desired, and that the SIE has not updated these values.

Bit [7:4] of this register are cleared by any non-locked write to this register, regardless of the value written.

Bit 7: SETUP Received

1 = A valid SETUP packet has been received. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval.

The polarity that triggers an interrupt is controlled independently for each GPIO pin by the GPIO Interrupt Polarity Registers. *Figure 19-6* and *Figure 19-7* control the interrupt polarity of each GPIO pin.

Bit #	7	6	5	4	3	2	1	0
Bit Name	P0 Interrupt Polarity							
Read/Write	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Figure 19-6. Port 0 Interrupt Polarity Register (Address 0x06)

Bit [7:0]: P0[7:0] Interrupt Polarity

1 = Rising GPIO edge

0 = Falling GPIO edge

Bit #	7	6	5	4	3	2	1	0
Bit Name	Reserved						P1[1:0] Interrupt Polarity	
Read/Write	-	-	-	-	-	-	W	W
Reset	0	0	0	0	0	0	0	0

Figure 19-7. Port 1 Interrupt Polarity Register (Address 0x07)

Bit [7:0]: P1[7:0] Interrupt Polarity

1 = Rising GPIO edge

0 = Falling GPIO edge

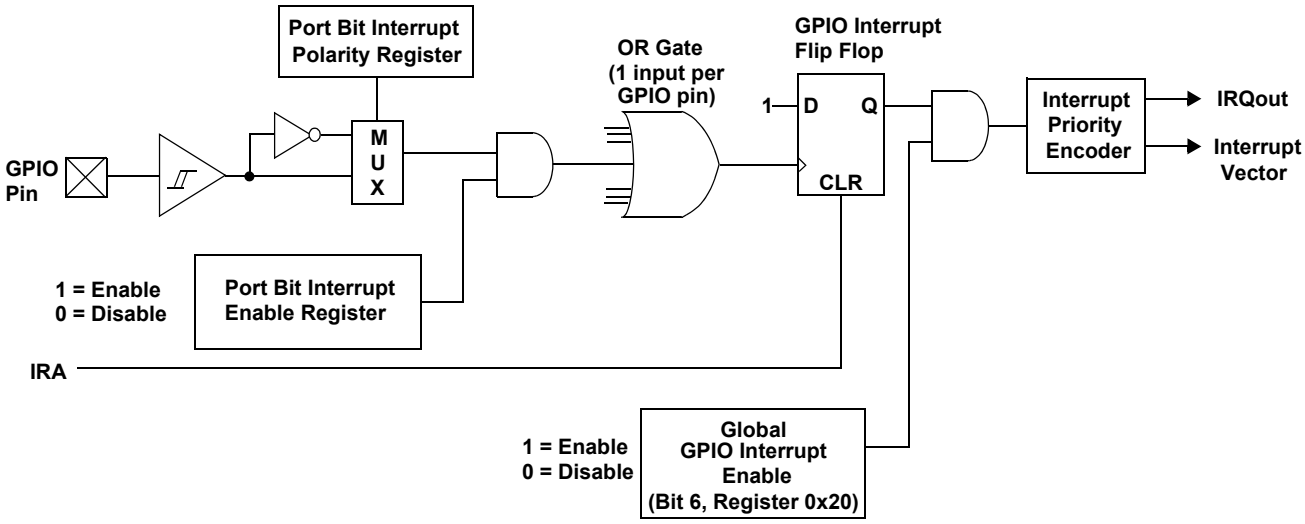


Figure 19-8. GPIO Interrupt Diagram

20.0 USB Mode Tables

The following tables give details on mode setting for the USB Serial Interface Engine (SIE) for both the control endpoint (EP0) and non-control endpoint (EP1).

Table 20-1. USB Register Mode Encoding for Control and Non-Control Endpoint

Mode	Encoding	SETUP	IN	OUT	Comments
Disable	**0000**	Ignore	Ignore	Ignore	Ignore all USB traffic to this endpoint
NAK IN/OUT	**0001**	Accept	NAK	NAK	On Control endpoint, after successfully sending an ACK handshake to a SETUP packet, the SIE forces the endpoint mode (from modes other than 0000) to 0001. The mode is also changed by the SIE to 0001 from mode 1011 on issuance of ACK handshake to an OUT.
Status OUT Only	**0010**	Accept	STALL	Check	For Control endpoints
STALL IN/OUT	**0011**	Accept	STALL	STALL	For Control endpoints
Ignore IN/OUT	**0100**	Accept	Ignore	Ignore	For Control endpoints
Reserved	**0101**	Ignore	Ignore	Always	Reserved
Status IN Only	**0110**	Accept	TX 0 Byte	STALL	For Control Endpoints
Reserved	**0111**	Ignore	TX Count	Ignore	Reserved
NAK OUT	**1000**	Ignore	Ignore	NAK	In mode 1001, after sending an ACK handshake to an OUT, the SIE changes the mode to 1000
ACK OUT($STALL^{[3]}=0$) ACK OUT($STALL^{[3]}=1$)	**1001** **1001**	Ignore Ignore	Ignore Ignore	ACK STALL	This mode is changed by the SIE to mode 1000 on issuance of ACK handshake to an OUT
NAK OUT - Status IN	**1010**	Accept	TX 0 Byte	NAK	
ACK OUT - NAK IN	**1011**	Accept	NAK	ACK	This mode is changed by the SIE to mode 0001 on issuance of ACK handshake to an OUT
NAK IN	**1100**	Ignore	NAK	Ignore	An ACK from mode 1101 changes the mode to 1100
ACK IN($STALL^{[3]}=0$) ACK IN($STALL^{[3]}=1$)	**1101** **1101**	Ignore Ignore	TX Count STALL	Ignore Ignore	This mode is changed by the SIE to mode 1100 on issuance of ACK handshake to an IN
NAK IN - Status OUT	**1110**	Accept	NAK	Check	An ACK from mode 1111 changes the mode to 1110
ACK IN - Status OUT	**1111**	Accept	TX Count	Check	This mode is changed by the SIE to mode 1110 on issuance of ACK handshake to an IN

Note:
3. STALL bit is the bit 7 of the USB Non-Control Device Endpoint Mode registers. Refer to Section 14.3 for more explanation.

Mode Column:

The 'Mode' column contains the mnemonic names given to the modes of the endpoint. The mode of the endpoint is determined by the 4 bit binaries in the 'Encoding' column as discussed below. The Status IN and Status OUT modes represent the status IN or OUT stage of the control transfer.

Encoding Column:

The contents of the 'Encoding' column represent the Mode Bits [3:0] of the Endpoint Mode Registers (*Figure 14-2* and *Figure 14-3*). The endpoint modes determine how the SIE responds to different tokens that the host sends to the endpoints. For example, if the Mode Bits [3:0] of the Endpoint 0 Mode Register (*Figure 14-2*) are set to '0001', which is NAK IN/OUT mode as shown in Table 20-1 above, the SIE of the part will send an ACK handshake in response to SETUP tokens and NAK any IN or OUT tokens. For more information on the functionality of the Serial Interface Engine (SIE), see Section 13.0.

SETUP, IN, and OUT Columns:

Depending on the mode specified in the 'Encoding' column, the 'SETUP', 'IN', and 'OUT' columns contain the device SIE's responses when the endpoint receives SETUP, IN, and OUT tokens respectively.

A 'Check' in the Out column means that upon receiving an OUT token the SIE checks to see whether the OUT is of zero length and has a Data Toggle (Data1/0) of 1. If these conditions are true, the SIE responds with an ACK. If any of the above conditions is not met, the SIE will respond with either a STALL or Ignore. Table 20-3 gives detailed analysis of all possible cases.

A 'TX Count' entry in the IN column means that the SIE will transmit the number of bytes specified in the Byte Count Bit [3:0] of the Endpoint Count Register (*Figure 14-4*) in response to any IN token.

A 'TX 0 Byte' entry in the IN column means that the SIE will transmit a zero byte packet in response to any IN sent to the endpoint. Sending a 0 byte packet is to complete the status stage of a control transfer.

An 'Ignore' means that the device sends no handshake tokens.

An 'Accept' means that the SIE will respond with an ACK to a valid SETUP transaction.

Comments Column:

Some Mode Bits are automatically changed by the SIE in response to many USB transactions. For example, if the Mode Bits [3:0] are set to '1111' which is ACK IN-Status OUT mode as shown in *Table 20-1*, the SIE will change the endpoint Mode Bits [3:0] to NAK IN-Status OUT mode (1110) after ACKing a valid status stage OUT token. The firmware needs to update the mode for the SIE to respond appropriately. See *Table 20-1* for more details on what modes will be changed by the SIE.

Any SETUP packet to an enabled endpoint with mode set to accept SETUPs will be changed by the SIE to 0001 (NAKing). Any mode set to accept a SETUP will send an ACK handshake to a valid SETUP token.

A disabled endpoint will remain disabled until changed by firmware, and all endpoints reset to the Disabled mode (0000). Firmware normally enables the endpoint mode after a SetConfiguration request.

The control endpoint has three status bits for identifying the token type received (SETUP, IN, or OUT), but the endpoint must be placed in the correct mode to function as such. Non-Control endpoint should not be placed into modes that accept SETUPs.

21.0 Register Summary

	Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/Write)/ Both(B)	Default/ Reset
GPIO CONFIGURATION PORTS 0, 1, AND 2	0x00	Port 0 Data	P0								BBBBBBBB	00000000
	0x01	Port 1 Data	Reserved						P1[1:0]		------BB	00000000
	0x02	Port 2 Data	Reserved		D+(SCLK) State	D- (SDATA) State	Reserved	P2.2(Int Clk Mode only)	P2.1 (Int Clk Mode only)	P2.0 Vreg Pin State	--RR-RRR	00000000
	0x0A	GPIO Port 0 Mode 0	P0[7:0] Mode0								WWWWWWWW	00000000
	0x0B	GPIO Port 0 Mode 1	P0[7:0] Mode1								WWWWWWWW	00000000
	0x0C	GPIO Port 1 Mode 0	Reserved						P1[1:0] Mode0		------WW	00000000
	0x0D	GPIO Port 1 Mode 1	Reserved						P1[1:0] Mode1		------WW	00000000
	0x04	Port 0 Interrupt Enable	P0[7:0] Interrupt Enable								WWWWWWWW	00000000
	0x05	Port 1 Interrupt Enable	Reserved						P1[1:0] Interrupt Enable		------WW	00000000
	0x06	Port 0 Interrupt Polarity	P0[7:0] Interrupt Polarity								WWWWWWWW	00000000
	0x07	Port 1 Interrupt Polarity	Reserved						P1[1:0] Interrupt Polarity		------WW	00000000
Clock Config.	0xF8	Clock Configuration	Ext. Clock Resume Delay	Wake-up Timer Adjust Bit [2:0]			Low Voltage Reset Disable	Precision USB Clocking Enable	Internal Clock Output Disable	External Oscillator Enable	BBBBBBBB	00000000
ENDPOINT 0, I AND 2 CONFIGURATION	0x10	USB Device Address	Device Address Enable	Device Address							BBBBBBBB	00000000
	0x12	EP0 Mode	SETUP Received	IN Received	OUT Received	ACKed Transaction	Mode Bit				BBBBBBBB	00000000
	0x14	EP1 Mode Register	STALL	Reserved		ACKed Transaction	Mode Bit				B--BBBBB	00000000
	0x11, 0x13	EP0 and 1Counter	Data 0/1 Toggle	Data Valid	Reserved		Byte Count				BB--BBBB	00000000
USB-SC	0x1F	USB Status and Control	PS/2 Pull-up Enable	VREG Enable	USB Reset-PS/2 Activity Interrupt Mode	Reserved	USB Bus Activity	D+/D- Forcing Bit			BBB-BBBB	00000000
INTERRUPT	0x20	Global Interrupt Enable	Wake-up Interrupt Enable	GPIO Interrupt Enable	Reserved			1.024 ms Interrupt Enable	128 µs Interrupt Enable	USB Bus Reset-PS/2 Activity Intr. Enable	BB---BBB	00000000
	0x21	Endpoint Interrupt Enable	Reserved						EP1 Interrupt Enable	EP0 Interrupt Enable	------BB	00000000
TIMER	0x24	Timer LSB	Timer Bit [7:0]								RRRRRRRR	00000000
	0x25	Timer (MSB)	Reserved				Timer Bit [11:8]				----RRRR	00000000
PROC SC.	0xFF	Process Status & Control	IRQ Pending	Watch Dog Reset	Bus Interrupt Event	LVR/BOR Reset	Suspend	Interrupt Enable Sense	Reserved	Run	RBBBBR-B	See Section 18.0

22.0 Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C
Ambient Temperature with Power Applied .....–0°C to +70°C
Supply voltage on V_{CC} relative to V_{SS} .....–0.5V to +7.0V
DC Input Voltage..... –0.5V to +V_{CC}+0.5V
DC Voltage Applied to Outputs in High Z State..... –0.5V to + V_{CC}+0.5V
Maximum Total Sink Output Current into Port 0 and 1 and Pins..... 70 mA
Maximum Total Source Output Current into Port 0 and 1 and Pins ..... 30 mA
Maximum On-chip Power Dissipation on any GPIO Pin .....50 mW
Power Dissipation .....300 mW
Static Discharge Voltage ..... >2000V
Latch-up Current ..... >200 mA

23.0 DC Characteristics

F_{OSC} = 6 MHz; Operating Temperature = 0 to 70°C

	Parameter	Min	Max	Units	Conditions
	General				
V_{CC1}	Operating Voltage	V_{LVR}	5.5	V	Note 4
V_{CC2}	Operating Voltage	4.35	5.25	V	Note 4
I_{CC1}	V_{CC} Operating Supply Current - Internal Oscillator Mode. Typical I_{CC1} = 16 mA[5]		20	mA	V_{CC} = 5.5V, no GPIO loading V_{CC} = 5.0V. T = Room Temperature
I_{CC2}	V_{CC} Operating Supply Current - External Oscillator Mode. Typical I_{CC2}= 13 mA[5]		17	mA	V_{CC} = 5.5V, no GPIO loading V_{CC} = 5.0V. T = Room Temperature
I_{SB1}	Standby Current - No Wake-up Osc		25	µA	Oscillator off, D– > 2.7V
I_{SB2}	Standby Current - With Wake-up Osc		75	µA	Oscillator off, D– > 2.7V
V_{PP}	Programming Voltage (disabled)	–0.4	0.4	V	
T_{RSNTR}	Resonator Start-up Interval		256	µs	V_{CC} = 5.0V, ceramic resonator
I_{IL}	Input Leakage Current		1	µA	Any I/O pin
I_{SNK}	Max I_{SS} GPIO Sink Current		70	mA	Cumulative across all ports[6]
I_{SRC}	Max I_{CC} GPIO Source Current		30	mA	Cumulative across all ports[6]
	Low-voltage and Power-on Reset				
V_{LVR}	Low-voltage Reset Trip Voltage	3.5	4.0	V	V_{CC} below V_{LVR} for >100 ns[7]
t_{VCCS}	V_{CC} Power-on Slew Time		100	ms	linear ramp: 0 to 4V[8]
	USB Interface				
V_{REG}	VREG Regulator Output Voltage	3.0	3.6	V	Load = R_{PU} +R_{PD}[9, 10]
C_{REG}	Capacitance on VREG Pin		300	pF	External cap not required
V_{OHU}	Static Output High, driven	2.8	3.6	V	R_{PD} to Gnd[4]
V_{OLU}	Static Output Low		0.3	V	With R_{PU} to VREG pin
V_{OHZ}	Static Output High, idle or suspend	2.7	3.6	V	R_{PD} connected D– to Gnd, R_{PU} connected D– to VREG pin[4]

Notes:
4. Full functionality is guaranteed in V_{CC1} range, except USB transmitter specifications and GPIO output currents are guaranteed for V_{CC2} range.
5. Bench measurements taken under nominal operating conditions. Spec cannot be guaranteed at final test.
6. Total current cumulative across all Port pins, limited to minimize Power and Ground-Drop noise effects.
7. LVR is automatically disabled during suspend mode.
8. LVR will re-occur whenever V_{CC} drops below V_{LVR}. In suspend or with LVR disabled, BOR occurs whenever V_{CC} drops below approximately 2.5V.
9. V_{RG} specified for regulator enabled, idle conditions (i.e., no USB traffic), with load resistors listed. During USB transmits from the internal SIE, the VREG output is not regulated, and should not be used as a general source of regulated voltage in that case. During receive of USB data, the VREG output drops when D– is LOW due to internal series resistance of approximately 200Ω at the VREG pin.
10. In suspend mode, V_{RG} is only valid if R_{PU} is connected from D– to VREG pin, and R_{PD} is connected from D– to ground

	Parameter	Min	Max	Units	Conditions
V_{DI}	Differential Input Sensitivity	0.2		V	|(D+)–(D–)|
V_{CM}	Differential Input Common Mode Range	0.8	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	2.0	V	
C_{IN}	Transceiver Capacitance		20	pF	
I_{LO}	Hi-Z State Data Line Leakage	–10	10	µA	0 V < V_{in}<3.3 V (D+ or D– pins)
R_{PU}	External Bus Pull-up resistance (D–)	1.274	1.326	kΩ	1.3 kΩ ±2% to VREG[11]
R_{PD}	External Bus Pull-down resistance	14.25	15.75	kΩ	15 kΩ ±5% to Gnd
	PS/2 Interface				
V_{OLP}	Static Output Low		0.4	V	Isink = 5 mA, SDATA or SCLK pins
R_{PS2}	Internal PS/2 Pull-up Resistance	3	7	kΩ	SDATA, SCLK pins, PS/2 Enabled
	General Purpose I/O Interface				
R_{UP}	Pull-up Resistance	8	24	kΩ	
V_{ICR}	Input Threshold Voltage, CMOS mode	40%	60%	V_{CC}	Low to high edge, Port 0 or 1
V_{ICF}	Input Threshold Voltage, CMOS mode	35%	55%	V_{CC}	High to low edge, Port 0 or 1
V_{HC}	Input Hysteresis Voltage, CMOS mode	3%	10%	V_{CC}	High to low edge, Port 0 or 1
V_{ITTL}	Input Threshold Voltage, TTL mode	0.8	2.0	V	Ports 0, 1, and 2
V_{OL1A} V_{OL1B}	Output Low Voltage, high drive mode		0.8 0.4	V V	I_{OL1} = 50 mA, Ports 0 or 1[4] I_{OL1} = 25 mA, Ports 0 or 1[4]
V_{OL2}	Output Low Voltage, medium drive mode		0.4	V	I_{OL2} = 8 mA, Ports 0 or 1[4]
V_{OL3}	Output Low Voltage, low drive mode		0.4	V	I_{OL3} = 2 mA, Ports 0 or 1[4]
V_{OH}	Output High Voltage, strong drive mode	V_{CC}–2		V	Port 0 or 1, I_{OH} = 2 mA[4]
R_{XIN}	Pull-down resistance, XTALIN pin	50		kΩ	Internal Clock Mode only

Note:
11. The 200Ω internal resistance at the VREG pin gives a standard USB pull-up using this value. Alternately, a 1.5 kΩ, 5% pull-up from D– to an external 3.3V supply can be used.

24.0 Switching Characteristics

Parameter	Description	Min.	Max.	Unit	Conditions
	Internal Clock Mode				
F_{ICLK}	Internal Clock Frequency	5.7	6.3	MHz	Internal Clock Mode enabled
F_{ICLK2}	Internal Clock Frequency, USB mode	5.91	6.09	MHz	Internal Clock Mode enabled, Bit 2 of register 0xF8h is set (Precision USB Clocking)[12]
	External Oscillator Mode				
T_{CYC}	Input Clock Cycle Time	164.2	169.2	ns	USB Operation, with External ±1.5% Ceramic Resonator or Crystal
T_{CH}	Clock HIGH Time	0.45 t_{CYC}		ns	
T_{CL}	Clock LOW Time	0.45 t_{CYC}		ns	
	Reset Timing				
t_{START}	Time-out Delay after LVR/BOR	24	60	ms	
t_{WAKE}	Internal Wake-up Period	1	5	ms	Enabled Wake-up Interrupt[13]
t_{WATCH}	WatchDog Timer Period	10.1	14.6	ms	F_{OSC} = 6 MHz
	USB Driver Characteristics				
T_R	Transition Rise Time	75		ns	CLoad = 200 pF (10% to 90%[4])
T_R	Transition Rise Time		300	ns	CLoad = 600 pF (10% to 90%[4])
T_F	Transition Fall Time	75		ns	CLoad = 200 pF (10% to 90%[4])
T_F	Transition Fall Time		300	ns	CLoad = 600 pF (10% to 90%[4])
T_{RFM}	Rise/Fall Time Matching	80	125	%	t_r/t_f[4, 14]
V_{CRS}	Output Signal Crossover Voltage[17]	1.3	2.0	V	CLoad = 200 to 600 pF[4]
	USB Data Timing				
T_{DRATE}	Low Speed Data Rate	1.4775	1.5225	Mb/s	Ave. Bit Rate (1.5 Mb/s ±1.5%)
T_{DJR1}	Receiver Data Jitter Tolerance	–75	75	ns	To Next Transition[15]
T_{DJR2}	Receiver Data Jitter Tolerance	–45	45	ns	For Paired Transitions[15]
T_{DEOP}	Differential to EOP transition Skew	–40	100	ns	Note 15
T_{EOPR2}	EOP Width at Receiver	670		ns	Accepts as EOP[15]
T_{EOPT}	Source EOP Width	1.25	1.50	µs	
T_{UDJ1}	Differential Driver Jitter	–95	95	ns	To next transition, *Figure 24-5*
T_{UDJ2}	Differential Driver Jitter	–150	150	ns	To paired transition, *Figure 24-5*
T_{LST}	Width of SE0 during Diff. Transition		210	ns	
	Non-USB Mode Driver Characteristics				Note 16
T_{FPS2}	SDATA / SCK Transition Fall Time	50	300	ns	CLoad = 150 pF to 600 pF

Notes:
12. Initially F_{ICLK2}=F_{ICLK} until a USB packet is received.
13. Wake-up time for Wake-up Adjust Bits cleared to 000b (minimum setting)
14. Tested at 200 pF.
15. Measured at cross-over point of differential data signals.
16. Non-USB Mode refers to driving the D–/SDATA and/or D+/SCLK pins with the Control Bits of the USB Status and Control Register, with Control Bit 2 HIGH.
17. Per the USB 2.0 Specification, Table 7.7, Note 10, the first transition from the Idle state is excluded.

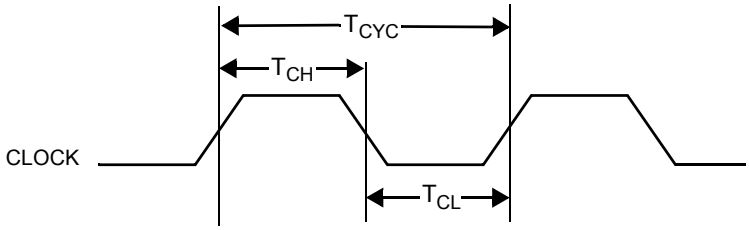


Figure 24-1. Clock Timing

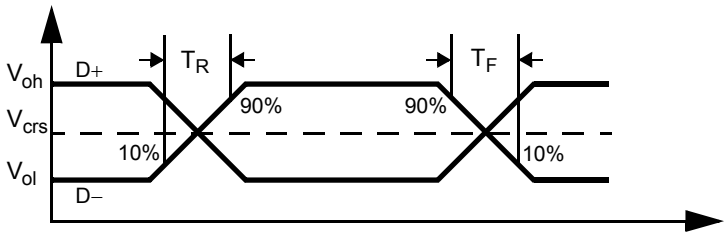


Figure 24-2. USB Data Signal Timing

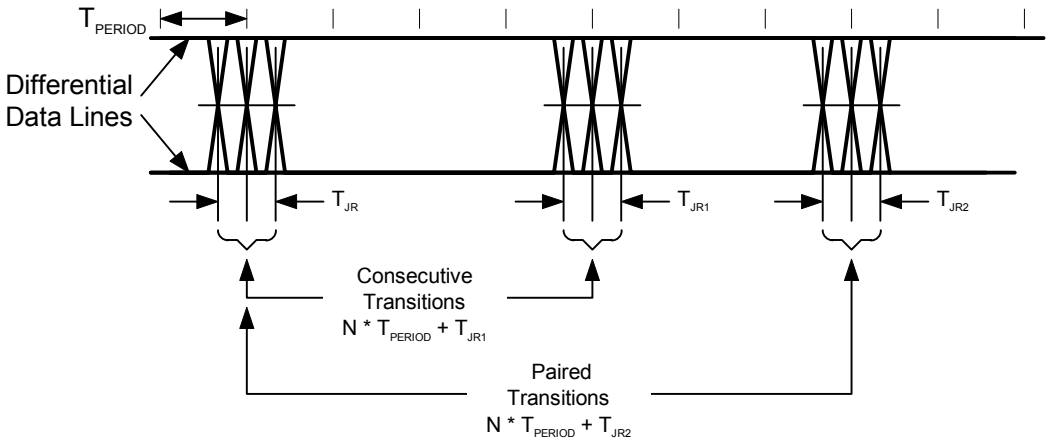


Figure 24-3. Receiver Jitter Tolerance

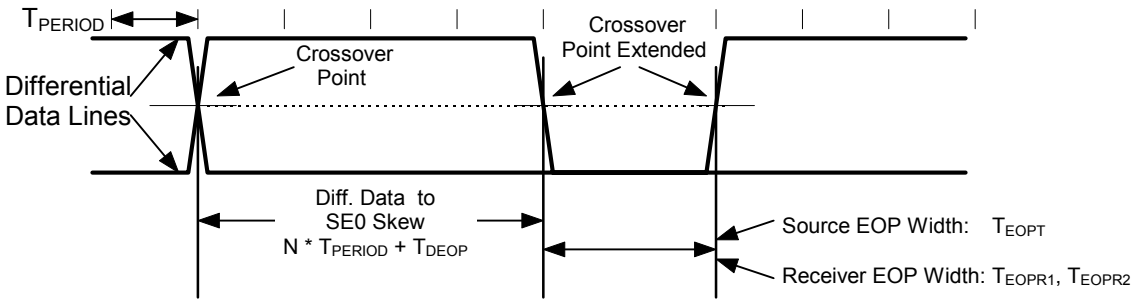


Figure 24-4. Differential to EOP Transition Skew and EOP Width

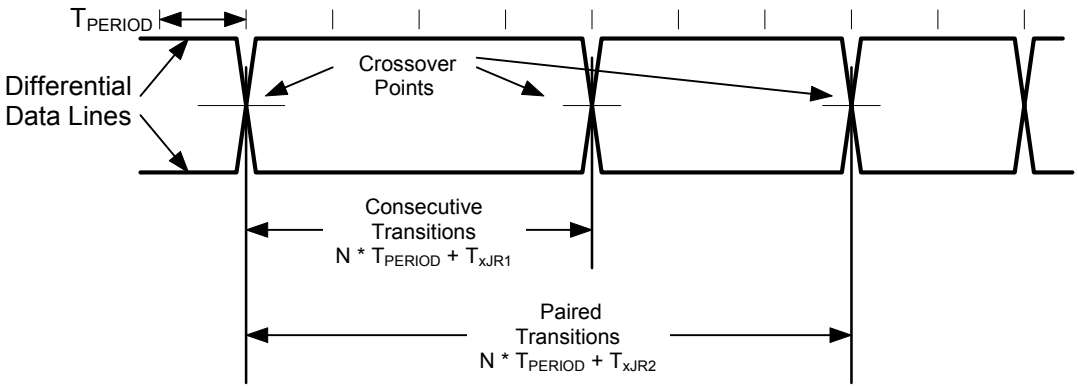


Figure 24-5. Differential Data Jitter

Table 26-1 below shows the die pad coordinates for the CY7C63221A-XC. The center location of each bond pad is relative to the center of the die which has coordinate (0,0) as shown above.

Table 26-1. CY7C63221A-XC Probe Pad Coordinates in microns ((0,0) to bond pad centers)

Pad Number	Pin Name	X (microns)	Y (microns)
1	P0.0	–351.75	995.00
2	P0.1	–543.20	995.00
3	P0.2	–734.65	995.00
4	P0.3	–861.05	779.25
5	P1.0	–861.05	587.80
6	Vss	–861.05	–949.65
7	Vpp	–468.20	–968.10
8	VREG	–300.40	–968.10
9	XTALIN	63.30	–968.10
10	XTALOUT	207.50	–968.10
11	Vcc	594.60	–968.10
12	D–	771.35	–968.10
13	D+	844.05	–863.10
14	P1.1	861.05	581.95
15	P0.7	861.05	773.95
16	P0.6	720.15	995.00
17	P0.5	528.70	995.00
18	P0.4	337.25	995.00

Document History Page

Document Title: CY7C63221/31A enCoRe™ Low-speed USB Peripheral Controller Document Number: 38-08028				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116226	06/17/02	DSG	Change from Spec number: 38-01049 to 38-08028
*A	116976	10/23/02	BON	Reformat. Add note 5 to 24.0. Add DIE sale, Section 21.0. Change *Figure 9-1*
*B	270731	See ECN	BON	Replaced the 16-Lead (300-Mil) Molded SOIC S1 graphic with the correct 18-Lead (300-Mil) Molded SOIC S1 one in the Package Diagram Section and corrected part numbers for lead-free packages.