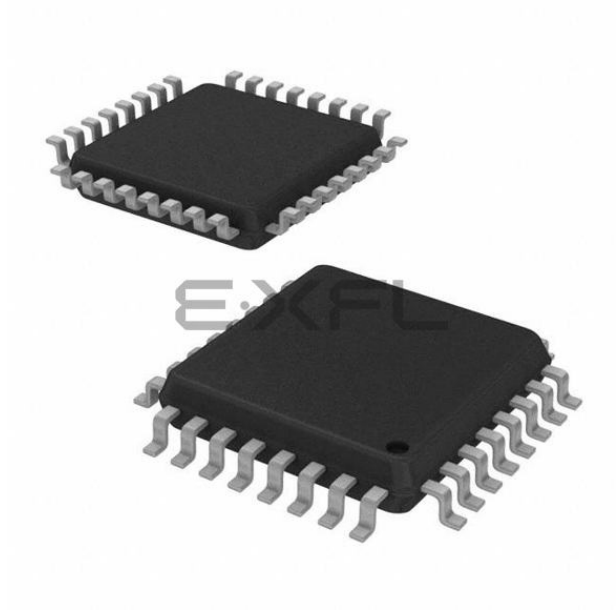

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Details	
Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
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Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pt32vlc

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x303F	Reserved	—	—	—	—	—	—	—	—
0x3040	PMC_SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
0x3041	PMC_SPMSC2	—	LVDV	LVWV		—	—	—	—
0x3042-0x3049	Reserved	—	—	—	—	—	—	—	—
0x304A	SYS_ILLAH	Bit 15	14	13	12	11	19	9	Bit 8
0x304B	SYS_ILLAL	Bit 7	6	5	4	3	2	1	Bit 0
0x304C-0x304F	Reserved	—	—	—	—	—	—	—	—
0x3050	IPC_ILRS0	ILR3		ILR2		ILR1		ILR0	
0x3051	IPC_ILRS1	ILR7		ILR6		ILR5		ILR4	
0x3052	IPC_ILRS2	ILR11		ILR10		ILR9		ILR8	
0x3053	IPC_ILRS3	ILR15		ILR14		ILR13		ILR12	
0x3054	IPC_ILRS4	ILR19		ILR18		ILR17		ILR16	
0x3055	IPC_ILRS5	ILR23		ILR22		ILR21		ILR20	
0x3056	IPC_ILRS6	ILR27		ILR26		ILR25		ILR24	
0x3057	IPC_ILRS7	ILR31		ILR30		ILR29		ILR28	
0x3058	IPC_ILRS8	ILR35		ILR34		ILR33		ILR32	
0x3059	IPC_ILRS9	ILR39		ILR38		ILR37		ILR36	
0x305A-0x305F	Reserved	—	—	—	—	—	—	—	—
0x3060	CRC_D0	Bit 31	30	29	28	27	26	25	Bit 24
0x3061	CRC_D1	Bit 23	22	21	20	19	18	17	Bit 16
0x3062	CRC_D2	Bit 15	14	13	12	11	10	9	Bit 8
0x3063	CRC_D3	Bit 7	6	5	4	3	2	1	Bit 0
0x3064	CRC_P0	Bit 31	30	29	28	27	26	25	Bit 24
0x3065	CRC_P1	Bit 23	22	21	20	19	18	17	Bit 16
0x3066	CRC_P2	Bit 15	14	13	12	11	10	9	Bit 8
0x3067	CRC_P3	Bit 7	6	5	4	3	2	1	Bit 0
0x3068	CRC_CTRL	TOT		TOTR		0	FXOR	WAS	TCRC
0x3069	Reserved	—	—	—	—	—	—	—	—
0x306A	RTC_SC1	RTIF	RTIE	—	RTCO	—	—	—	—
0x306B	RTC_SC2	RTCLKS		—	—	—	RTCPS		
0x306C	RTC_MODH	MODH							
0x306D	RTC_MODL	MODL							
0x306E	RTC_CNTH	CNTH							
0x306F	RTC_CNTL	CNTL							
0x3070	I2C_A1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0x3071	I2C_F	MULT		ICR					
0x3072	I2C_C1	IICEN	IICIE	MST	TX	TXAK	RSTA	WUEN	—
0x3073	I2C_S	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
0x3074	I2C_D	DATA							

Table continues on the next page...

4.5.2.2 Flash and EEPROM memory map

The MCU places the flash memory between global address 0x0000 and 0xFFFF as shown in the following table. Not all flash are available to users because some addresses are overlapped with RAM, EEPROM, and registers.

MC9S08PT60 contains a piece of 64 KB flash in which only 60,864 bytes flash are available for users. This flash block is divided into 128 sectors of 512 bytes. MC9S08PT32 contains a piece of 32 KB flash that is fully available for users. This flash block is divided into 64 sectors of 512 bytes.

Table 4-6. Flash memory addressing

Device	Global address	Size (Bytes)	Description	User availability
MC9S08PT60	0x0000 — 0xFFFF	64 KB	Flash block contains flash configuration field	Sector [0:7]: N/A Sector [8]: Last 448 bytes available Sector [9:23]: fully available Sector [24]: N/A Sector [25:127]: fully available
MC9S08PT32	0x8000 — 0xFFFF	32 KB	Flash block contains flash configuration field	Sector [64:127]: fully available

4.5.2.3 Flash and EEPROM initialization after system reset

On each system reset, the flash and EEPROM module executes an initialization sequence that establishes initial values for the flash and EEPROM block configuration parameters, the FPROT and EEPROT protection registers, and the FOPT and FSEC registers. The initialization routine reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If a double bit fault is detected during the reset sequence, both FSTAT[MGSTAT] bits will be set.

FSTAT[CCIF] is cleared throughout the initialization sequence. The NVM module holds off all CPU access for a portion of the initialization sequence. Flash and EEPROM reads are allowed after the hold is removed. Completion of the initialization sequence is marked by setting FSTAT[CCIF] high, which enables user commands.

If a reset occurs while any flash or EEPROM command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

Table 5-1. Vector summary (from lowest to highest priority) (continued)

Vector number	Address (high/ low)	Vector name	Module	Source	Local enable	Description
				TC	TCIE	
24	0xFFCE:FFCF	Vsci0rx	SCI0	IDLE RDRF LBKDIF RXEDGIF	ILIE RIE LBKDIE RXEDGIE	SCI0 receive
23	0xFFD0:FFD1	Vsci0err	SCI0	OR NF FE PF	ORIE NEIE FEIE PEIE	SCI0 error
22	0xFFD2:FFD3	Vadc	ADC	COCO	AIEN	ADC conversion complete interrupt
21	0xFFD4:FFD5	Vacmp	ACMP	ACF	ACIE	Analog comparator interrupt
20	0xFFD6:FFD7	Vmtim1	MTIM1	TOF	TOIE	MTIM1 overflow interrupt
19	0xFFD8:FFD9	Vmtim0	MTIM0	TOF	TOIE	MTIM0 overflow interrupt
18	0xFFDA:FFDB	Vftm0ovf	FTM0	TOF	TOIE	FTM0 overflow
17	0xFFDC:FFDD	Vftm0ch1	FTM0CH1	CH1F	CH1IE	FTM0 channel 1
16	0xFFDE:FFDF	Vftm0ch0	FTM0CH0	CH0F	CH0IE	FTM0 channel 0
15	0xFFE0:FFE1	Vftm1ovf	FTM1	TOF	TOIE	FTM1 overflow
14	0xFFE2:FFE3	Vftm1ch1	FTM1CH1	CH1F	CH1IE	FTM1 channel 1
13	0xFFE4:FFE5	Vftm1ch0	FTM1CH0	CH0F	CH0IE	FTM1 channel 0
12	0xFFE6:FFE7	Vftm2ovf	FTM2	TOF	TOIE	FTM2 overflow
11	0xFFE8:FFE9	Vftm2ch5	FTM2CH5	CH5F	CH5IE	FTM2 channel 5
10	0xFFEA:FFEB	Vftm2ch4	FTM2CH4	CH4F	CH4IE	FTM2 channel 4
9	0xFFEC:FFED	Vftm2ch3	FTM2CH3	CH3F	CH3IE	FTM2 channel 3
8	0xFFEE:FFEF	Vftm2ch2	FTM2CH2	CH2F	CH2IE	FTM2 channel 2
7	0xFFF0:FFF1	Vftm2ch1	FTM2CH1	CH1F	CH1IE	FTM2 channel 1
6	0xFFF2:FFF3	Vftm2ch0	FTM2CH0	CH0F	CH0IE	FTM2 channel 0
5	0xFFF4:FFF5	Vftm2fault	FTM2	FAULTF	FAULTIE	FTM2 fault
4	0xFFF6:FFF7	Vclk	ICS	LOLS	LOLIE	Clock loss of lock
3	0xFFF8:FFF9	Vlvw	System control	LVWF	LVWIE	Low-voltage warning
2	0xFFFA:FFFB	Vwdog Virq	WDOG IRQ	WDOGF IRQF	WDOGI IRQIE	WDOG timeout IRQ interrupt
1	0xFFFC:FFFD	Vswi	Core	SWI Instruction	—	Software interrupt
0	0xFFFE:FFFF	Vreset	System control	WDOG LVD RESET pin	WDOGE LVDRE RSTPE	Watchdog timer Low-voltage detect External pin

6.6.14 Universally Unique Identifier Register 4 (SYS_UUID4)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + FBh offset = 30FBh

Bit	7	6	5	4	3	2	1	0
Read	ID[39:32]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID4 field descriptions

Field	Description
ID[39:32]	Universally Unique Identifier

6.6.15 Universally Unique Identifier Register 5 (SYS_UUID5)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FCh offset = 30FCh

Bit	7	6	5	4	3	2	1	0
Read	ID[31:24]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID5 field descriptions

Field	Description
ID[31:24]	Universally Unique Identifier

PORT_PTHOE field descriptions (continued)

Field	Description
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHOE2	Output Enable for Port H Bit 2 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 2. 1 Output Enabled for port H bit 2.
1 PTHOE1	Output Enable for Port H Bit 1 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 1. 1 Output Enabled for port H bit 1.
0 PTHOE0	Output Enable for Port H Bit 0 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 0. 1 Output Enabled for port H bit 0.

7.7.18 Port A Input Enable Register (PORT_PTAIE)

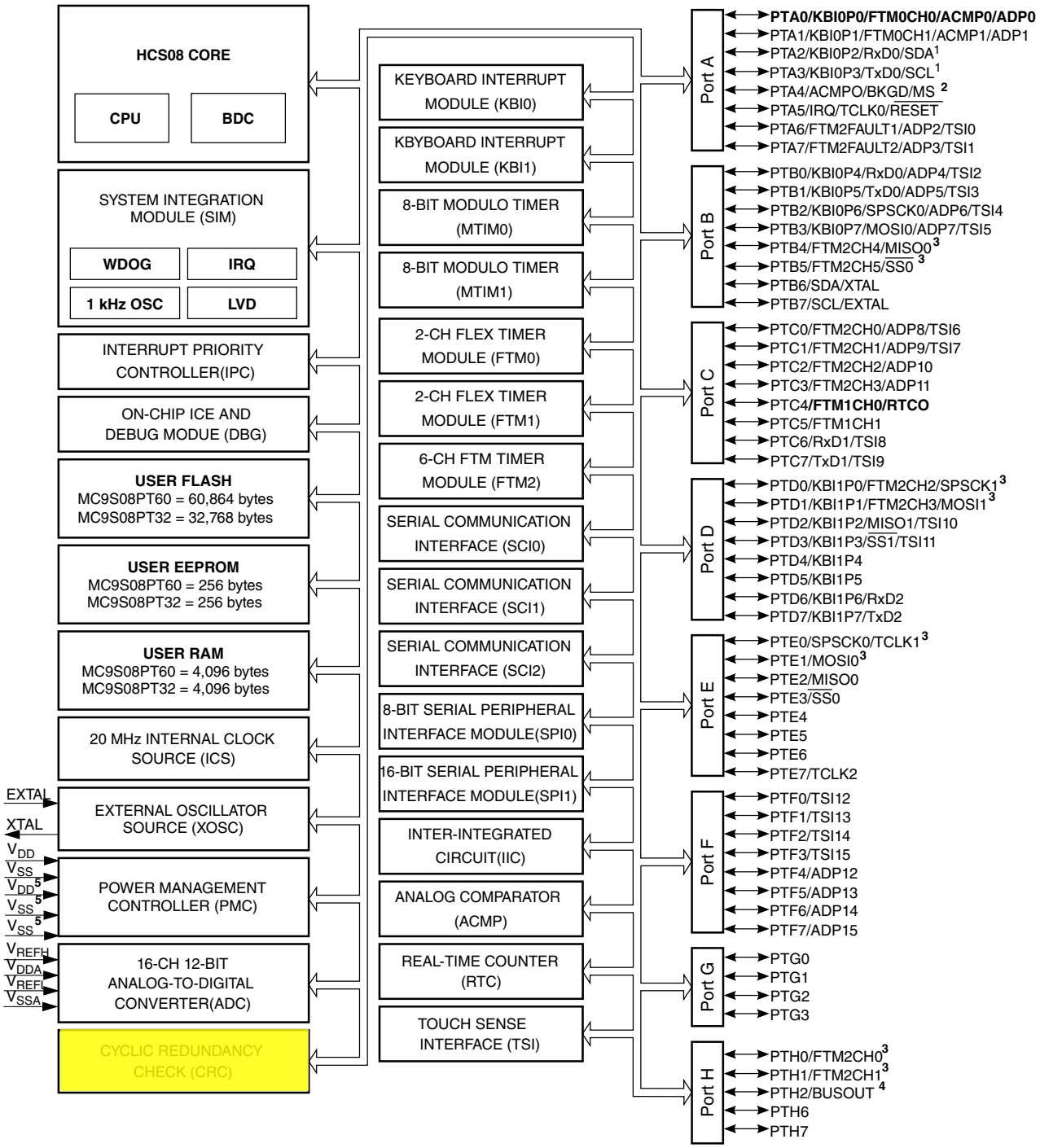
Address: 0h base + 30B8h offset = 30B8h

Bit	7	6	5	4	3	2	1	0
Read	PTAIE7	PTAIE6	PTAIE5	0	PTAIE3	PTAIE2	PTAIE1	PTAIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAIE field descriptions

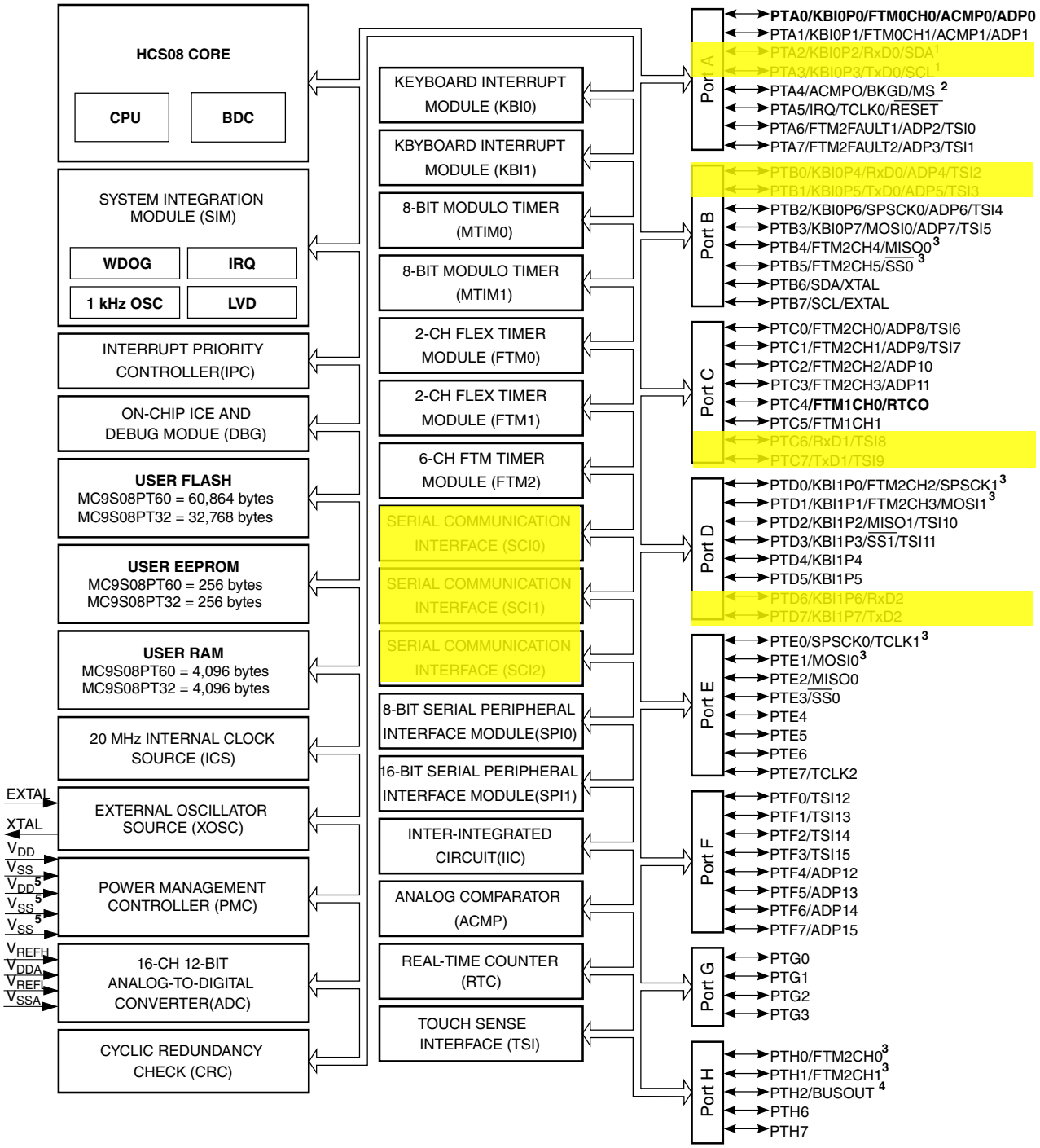
Field	Description
7 PTAIE7	Input Enable for Port A Bit 7 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 7. 1 Input enabled for port A bit 7.
6 PTAIE6	Input Enable for Port A Bit 6 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 6. 1 Input enabled for port A bit 6.
5 PTAIE5	Input Enable for Port A Bit 5 This read/write bit enables the port A pin as an input.

Table continues on the next page...



1. **PTA2 and PTA3 operate as true open drain when working as output .**
2. **PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.**
3. **PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 can provide ultra-high source/sink current up to 20 mA.**
4. **The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.**
5. **The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded** in 32-pin packages.

Figure 9-2. Device block diagram highlighting CRC module



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 can provide ultra-high source/sink current up to 20 mA.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-6. Device block diagram highlighting SCI modules and pins

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
26	Channel Value High (FTM0_C0VH)	8	R/W	00h	12.3.9/315
27	Channel Value Low (FTM0_C0VL)	8	R/W	00h	12.3.10/316
28	Channel Status and Control (FTM0_C1SC)	8	R/W	00h	12.3.8/312
29	Channel Value High (FTM0_C1VH)	8	R/W	00h	12.3.9/315
2A	Channel Value Low (FTM0_C1VL)	8	R/W	00h	12.3.10/316
2B	Channel Status and Control (FTM0_C2SC)	8	R/W	00h	12.3.8/312
2C	Channel Value High (FTM0_C2VH)	8	R/W	00h	12.3.9/315
2D	Channel Value Low (FTM0_C2VL)	8	R/W	00h	12.3.10/316
2E	Channel Status and Control (FTM0_C3SC)	8	R/W	00h	12.3.8/312
2F	Channel Value High (FTM0_C3VH)	8	R/W	00h	12.3.9/315
30	Channel Value Low (FTM0_C3VL)	8	R/W	00h	12.3.10/316
31	Channel Status and Control (FTM0_C4SC)	8	R/W	00h	12.3.8/312
32	Channel Value High (FTM0_C4VH)	8	R/W	00h	12.3.9/315
33	Channel Value Low (FTM0_C4VL)	8	R/W	00h	12.3.10/316
34	Channel Status and Control (FTM0_C5SC)	8	R/W	00h	12.3.8/312
35	Channel Value High (FTM0_C5VH)	8	R/W	00h	12.3.9/315
36	Channel Value Low (FTM0_C5VL)	8	R/W	00h	12.3.10/316
37	Counter Initial Value High (FTM0_CNTINH)	8	R/W	00h	12.3.11/316
38	Counter Initial Value Low (FTM0_CNTINL)	8	R/W	00h	12.3.12/317
39	Capture and Compare Status (FTM0_STATUS)	8	R/W	00h	12.3.13/317
3A	Features Mode Selection (FTM0_MODE)	8	R/W	04h	12.3.14/319
3B	Synchronization (FTM0_SYNC)	8	R/W	00h	12.3.15/320
3C	Initial State for Channel Output (FTM0_OUTINIT)	8	R/W	00h	12.3.16/322
3D	Output Mask (FTM0_OUTMASK)	8	R/W	00h	12.3.17/324
3E	Function for Linked Channels (FTM0_COMBINE0)	8	R/W	00h	12.3.18/325
3F	Function for Linked Channels (FTM0_COMBINE1)	8	R/W	00h	12.3.18/325
40	Function for Linked Channels (FTM0_COMBINE2)	8	R/W	00h	12.3.18/325
42	Deadtime Insertion Control (FTM0_DEADTIME)	8	R/W	00h	12.3.19/327
43	External Trigger (FTM0_EXTTRIG)	8	R/W	00h	12.3.20/328
44	Channels Polarity (FTM0_POL)	8	R/W	00h	12.3.21/329
45	Fault Mode Status (FTM0_FMS)	8	R/W	00h	12.3.22/331
46	Input Capture Filter Control (FTM0_FILTER0)	8	R/W	00h	12.3.23/332
47	Input Capture Filter Control (FTM0_FILTER1)	8	R/W	00h	12.3.23/332
48	Fault Input Filter Control (FTM0_FLTFILTER)	8	R/W	00h	12.3.24/333
49	Fault Input Control (FTM0_FLTCTRL)	8	R/W	00h	12.3.25/334
30	Status and Control (FTM1_SC)	8	R/W	00h	12.3.3/309
31	Counter High (FTM1_CNTH)	8	R/W	00h	12.3.4/310
32	Counter Low (FTM1_CNTL)	8	R/W	00h	12.3.5/311

Table continues on the next page...

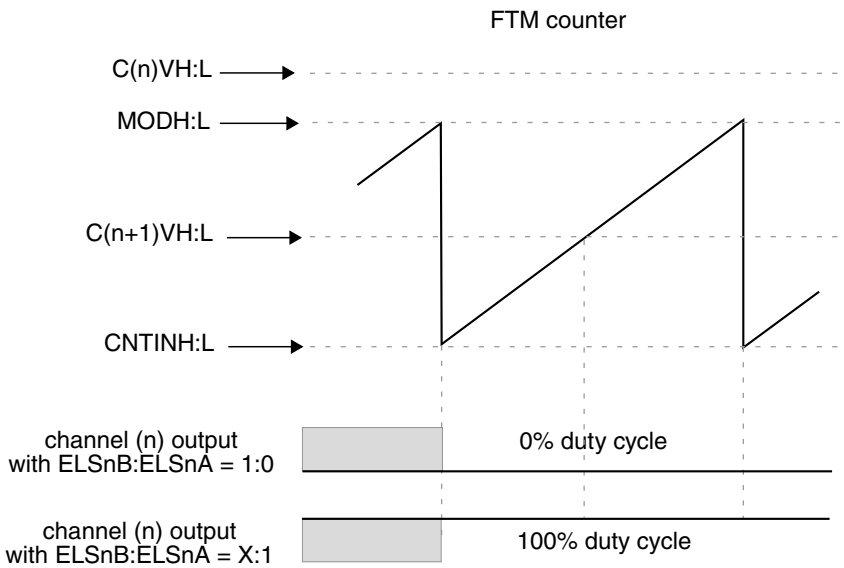


Figure 12-218. Channel (n) output if (C(n)V > MOD) and (CNTIN < C(n+1)V < MOD)

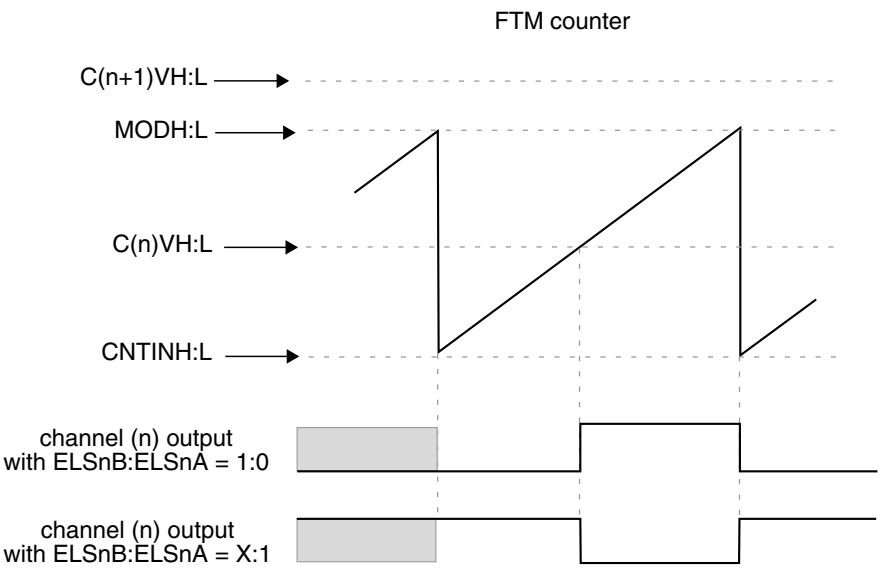


Figure 12-219. Channel (n) output if (C(n+1)V > MOD) and (CNTIN < C(n)V < MOD)

12.4.23 BDM mode

When BDM mode is active, the FlexTimer counter and the channels output are frozen.

However, the value of FlexTimer counter or the channels output are modified in BDM mode when:

- A write of any value to the CNTH or CNTL registers (Counter reset) resets the FTM counter to the value of CNTINH:L and the channels output to their initial value, except for channels in output compare mode.
- The PWM synchronization with REINIT = 1 (see FTM counter synchronization) resets the FTM counter to the value of CNTINH:L registers and the channels output to their initial value, except for channels in output compare mode.
- The initialization (Initialization) forces the value of the CHnOI bit to the channel (n) output.

Note

Do not use the above cases together with fault control (Fault control). If fault control is enabled and the fault condition is at the enabled fault input, these cases reset the FTM counter to the CNTINH:L value and the channels output to their initial value.

12.5 Reset overview

The FTM is reset whenever any chip reset occurs.

When the FTM exits from reset:

- The FTM counter and the prescaler counter are zero and are stopped (CLKS[1:0] = 0b00)
- The timer overflow interrupt is zero (Timer overflow interrupt)
- The channels interrupts are zero (Channel (n) interrupt)
- The fault interrupt is zero (Fault interrupt)
- The channels are in input capture mode (Input capture mode)
- The channels outputs are zero
- The channels pins are not controlled by FTM (ELS(n)B:ELS(n)A = 0b00). See table "Mode, Edge, and Level Selection"

SCIx_C2 field descriptions (continued)

Field	Description
	TE must be 1 to use the SCI transmitter. When TE is set, the SCI forces the TxD pin to act as an output for the SCI system. When the SCI is configured for single-wire operation (LOOPS = RSRC = 1), TXDIR controls the direction of traffic on the single SCI communication line (TxD pin). TE can also queue an idle character by clearing TE then setting TE while a transmission is in progress. When TE is written to 0, the transmitter keeps control of the port TxD pin until any data, queued idle, or queued break character finishes transmitting before allowing the pin to revert to a general-purpose I/O pin. 0 Transmitter off. 1 Transmitter on.
2 RE	Receiver Enable When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS is set the RxD pin reverts to being a general-purpose I/O pin even if RE is set. 0 Receiver off. 1 Receiver on.
1 RWU	Receiver Wakeup Control This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is an idle line between messages, WAKE = 0, idle-line wakeup, or a logic 1 in the most significant data bit in a character, WAKE = 1, address-mark wakeup. Application software sets RWU and, normally, a selected hardware condition automatically clears RWU. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	Send Break Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 or 12, 13 or 14 or 15 if BRK13 = 1, bit times of logic 0 are queued as long as SBK is set. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

15.3.5 SCI Status Register 1 (SCIx_S1)

This register has eight read-only status flags. Writes have no effect. Special software sequences, which do not involve writing to this register, clear these status flags.

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write								
Reset	1	1	0	0	0	0	0	0

SPI0_C2 field descriptions (continued)

Field	Description
0 SPC0	SPI pin control 0 This bit enables bidirectional pin configurations. 0 SPI uses separate pins for data input and data output (pin mode is normal). In master mode of operation: MISO is master in and MOSI is master out. In slave mode of operation: MISO is slave out and MOSI is slave in. 1 SPI configured for single-wire bidirectional operation (pin mode is bidirectional). In master mode of operation: MISO is not used by SPI; MOSI is master in when BIDIROE is 0 or master I/O when BIDIROE is 1. In slave mode of operation: MISO is slave in when BIDIROE is 0 or slave I/O when BIDIROE is 1; MOSI is not used by SPI.

16.3.3 SPI baud rate register (SPIx_BR)

Use this register to set the prescaler and bit rate divisor for an SPI master. This register may be read or written at any time.

Address: 3098h base + 2h offset = 309Ah

Bit	7	6	5	4	3	2	1	0
Read	0	SPPR[2:0]			SPR[3:0]			
Write								
Reset	0	0	0	0	0	0	0	0

SPI0_BR field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 SPPR[2:0]	SPI baud rate prescale divisor This 3-bit field selects one of eight divisors for the SPI baud rate prescaler. The input to this prescaler is the bus rate clock (BUSCLK). The output of this prescaler drives the input of the SPI baud rate divider. Refer to the description of “SPI Baud Rate Generation” for details. 000 Baud rate prescaler divisor is 1 001 Baud rate prescaler divisor is 2 010 Baud rate prescaler divisor is 3 011 Baud rate prescaler divisor is 4 100 Baud rate prescaler divisor is 5 101 Baud rate prescaler divisor is 6 110 Baud rate prescaler divisor is 7 111 Baud rate prescaler divisor is 8

Table continues on the next page...

SPI1_BR field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 SPPR[2:0]	SPI Baud Rate Prescale Divisor This 3-bit field selects one of eight divisors for the SPI baud rate prescaler. The input to this prescaler is the bus rate clock (BUSCLK). The output of this prescaler drives the input of the SPI baud rate divider. Refer to the description of “SPI Baud Rate Generation” for details. 000 Baud rate prescaler divisor is 1. 001 Baud rate prescaler divisor is 2. 010 Baud rate prescaler divisor is 3. 011 Baud rate prescaler divisor is 4. 100 Baud rate prescaler divisor is 5. 101 Baud rate prescaler divisor is 6. 110 Baud rate prescaler divisor is 7. 111 Baud rate prescaler divisor is 8.
SPR[3:0]	SPI Baud Rate Divisor This 4-bit field selects one of nine divisors for the SPI baud rate divider. The input to this divider comes from the SPI baud rate prescaler. Refer to the description of “SPI Baud Rate Generation” for details. 0000 Baud rate divisor is 2. 0001 Baud rate divisor is 4. 0010 Baud rate divisor is 8. 0011 Baud rate divisor is 16. 0100 Baud rate divisor is 32. 0101 Baud rate divisor is 64. 0110 Baud rate divisor is 128. 0111 Baud rate divisor is 256. 1000 Baud rate divisor is 512. All others Reserved

17.3.4 SPI Status Register (SPIx_S)

This register contains read-only status bits. Writes have no meaning or effect.

When the FIFO is supported and enabled (FIFOMODE is 1): This register has four flags that provide mechanisms to support an 8-byte FIFO mode: RNFULLF, TNEARF, TXFULLF, and RFIFOEF. When the SPI is in 8-byte FIFO mode, the function of SPRF and SPTEF differs slightly from their function in the normal buffered modes, mainly regarding how these flags are cleared by the amount available in the transmit and receive FIFOs.

- The RNFULLF and TNEAREF help improve the efficiency of FIFO operation when transfering large amounts of data. These flags provide a "watermark" feature of the FIFOs to allow continuous transmissions of data when running at high speed.

NOTE

When the TCKSEL bit is set, there is no need to monitor the SHTF1 bit because the bus speed is too high to match the protocol of SMBus.

Address: 3070h base + 8h offset = 3078h

Bit	7	6	5	4	3	2	1	0
Read	FACK	ALERTEN	SIICAEN	TCKSEL	SLTF	SHTF1	SHTF2	SHTF2IE
Write					w1c		w1c	
Reset	0	0	0	0	0	0	0	0

I2C_SMB field descriptions

Field	Description
7 FACK	Fast NACK/ACK Enable For SMBus packet error checking, the CPU must be able to issue an ACK or NACK according to the result of receiving data byte. 0 An ACK or NACK is sent on the following receiving data byte 1 Writing 0 to TXAK after receiving a data byte generates an ACK. Writing 1 to TXAK after receiving a data byte generates a NACK.
6 ALERTEN	SMBus Alert Response Address Enable Enables or disables SMBus alert response address matching. **NOTE:** After the host responds to a device that used the alert response address, you must use software to put the device's address on the bus. The alert protocol is described in the SMBus specification. 0 SMBus alert response address matching is disabled 1 SMBus alert response address matching is enabled
5 SIICAEN	Second I2C Address Enable Enables or disables SMBus device default address. 0 I2C address register 2 matching is disabled 1 I2C address register 2 matching is enabled
4 TCKSEL	Timeout Counter Clock Select Selects the clock source of the timeout counter. 0 Timeout counter counts at the frequency of the I2C module clock / 64 1 Timeout counter counts at the frequency of the I2C module clock
3 SLTF	SCL Low Timeout Flag This bit is set when the SLT register (consisting of the SLTH and SLTL registers) is loaded with a non-zero value (LoValue) and an SCL low timeout occurs. Software clears this bit by writing a logic 1 to it. **NOTE:** The low timeout function is disabled when the SLT register's value is 0. 0 No low timeout occurs 1 Low timeout occurs

Table continues on the next page...

18.4.6.3 Exit from low-power/stop modes

The slave receive input detect circuit and address matching feature are still active on low power modes (wait and stop). An asynchronous input matching slave address or general call address brings the CPU out of low power/stop mode if the interrupt is not masked. Therefore, TCF and IAAS both can trigger this interrupt.

18.4.6.4 Arbitration lost interrupt

The I2C is a true multimaster bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, the relative priority of the contending masters is determined by a data arbitration procedure. The I2C module asserts the arbitration-lost interrupt when it loses the data arbitration process and the ARBL bit in the Status Register is set.

Arbitration is lost in the following circumstances:

1. SDA is sampled as low when the master drives high during an address or data transmit cycle.
2. SDA is sampled as low when the master drives high during the acknowledge bit of a data receive cycle.
3. A START cycle is attempted when the bus is busy.
4. A repeated START cycle is requested in slave mode.
5. A STOP condition is detected when the master did not request it.

The ARBL bit must be cleared (by software) by writing 1 to it.

18.4.6.5 Timeout interrupt in SMBus

When the IICIE bit is set, the I2C module asserts a timeout interrupt (outputs SLTF and SHTF2) upon detection of any of the mentioned timeout conditions, with one exception. The SCL high and SDA high TIMEOUT mechanism must not be used to influence the timeout interrupt output, because this timeout indicates an idle condition on the bus. SHTF1 rises when it matches the SCL high and SDA high TIMEOUT and falls automatically just to indicate the bus status. The SHTF2's timeout period is the same as that of SHTF1, which is short compared to that of SLTF, so another control bit, SHTF2IE, is added to enable or disable it.

ADC_APCTL1 field descriptions (continued)

Field	Description
1 ADPC1	ADC Pin Control 1 ADPC1 controls the pin associated with channel AD1. 0 AD1 pin I/O control enabled. 1 AD1 pin I/O control disabled.
0 ADPC0	ADC Pin Control 0 ADPC0 controls the pin associated with channel AD0. 0 AD0 pin I/O control enabled. 1 AD0 pin I/O control disabled.

19.3.10 Pin Control 2 Register (ADC_APCTL2)

APCTL2 controls channels 8-15 of the ADC module.

Address: 10h base + 309Dh offset = 30ADh

Bit	7	6	5	4	3	2	1	0
Read Write	ADPC15	ADPC14	ADPC13	ADPC12	ADPC11	ADPC10	ADPC9	ADPC8
Reset	0	0	0	0	0	0	0	0

ADC_APCTL2 field descriptions

Field	Description
7 ADPC15	ADC Pin Control 15 ADPC15 controls the pin associated with channel AD15. 0 AD15 pin I/O control enabled. 1 AD15 pin I/O control disabled.
6 ADPC14	ADC Pin Control 14 ADPC14 controls the pin associated with channel AD14. 0 AD14 pin I/O control enabled. 1 AD14 pin I/O control disabled.
5 ADPC13	ADC Pin Control 13 ADPC13 controls the pin associated with channel AD13. 0 AD13 pin I/O control enabled. 1 AD13 pin I/O control disabled.
4 ADPC12	ADC Pin Control 12 ADPC12 controls the pin associated with channel AD12.

Table continues on the next page...

12. Reduce Rs value by incrementing TSI_CS2[EXTCHRG] by 1 if (Rs > minimum value) (i.e., TSI_CS2[EXTCHRG] < 111b), and then go to END (Now a matching DVOLT corresponding to the noise level is found)
13. Reduce DVOLT by incrementing TSI_CS2[DVOLT] by 1 if (Rs = maximum value) (i.e.,TSI_CS2[EXTCHRG] = 011b); (Now a matching DVOLT corresponding to the noise level is found)
14. END:

NOTE

The END condition of above algorithm can be one of

- TSI counter value within the WINDOW and Rs ≥ minimum value
- TSI counter value out of the WINDOW and Rs = minimum value and DVOLT = maximum value

At the end of the above steps, the correct matching DVOLT value and the electrode oscillator charge and discharge current value for the current noise level is found. That is, the correct TSI_CS2[DVOLT] value and TSI_CS2[EXTCHRG] value are found for the current noise level. And now users can proceed with normal capacitive sense procedure by keeping both TSI_CS[DVOLT] and TSI_CS2[EXTCHRG] untouched, that is, users just need switch to normal capacitive sense mode by clearing TSI_CS3[STAT_STUP[3:2]] bits and start TSI scan.

For typical applications, the noise detection/sense algorithm shall be performed first followed by normal capacitive sense for a given channel and then alternate between noise sense and capacitive sense as shown in Figure 21-15.

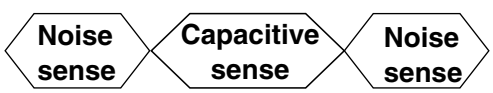


Figure 21-15. Noise detection/sense algorithm of typical application

The following flow chart shows how to detect touch with noise sense and normal capacitive sense.

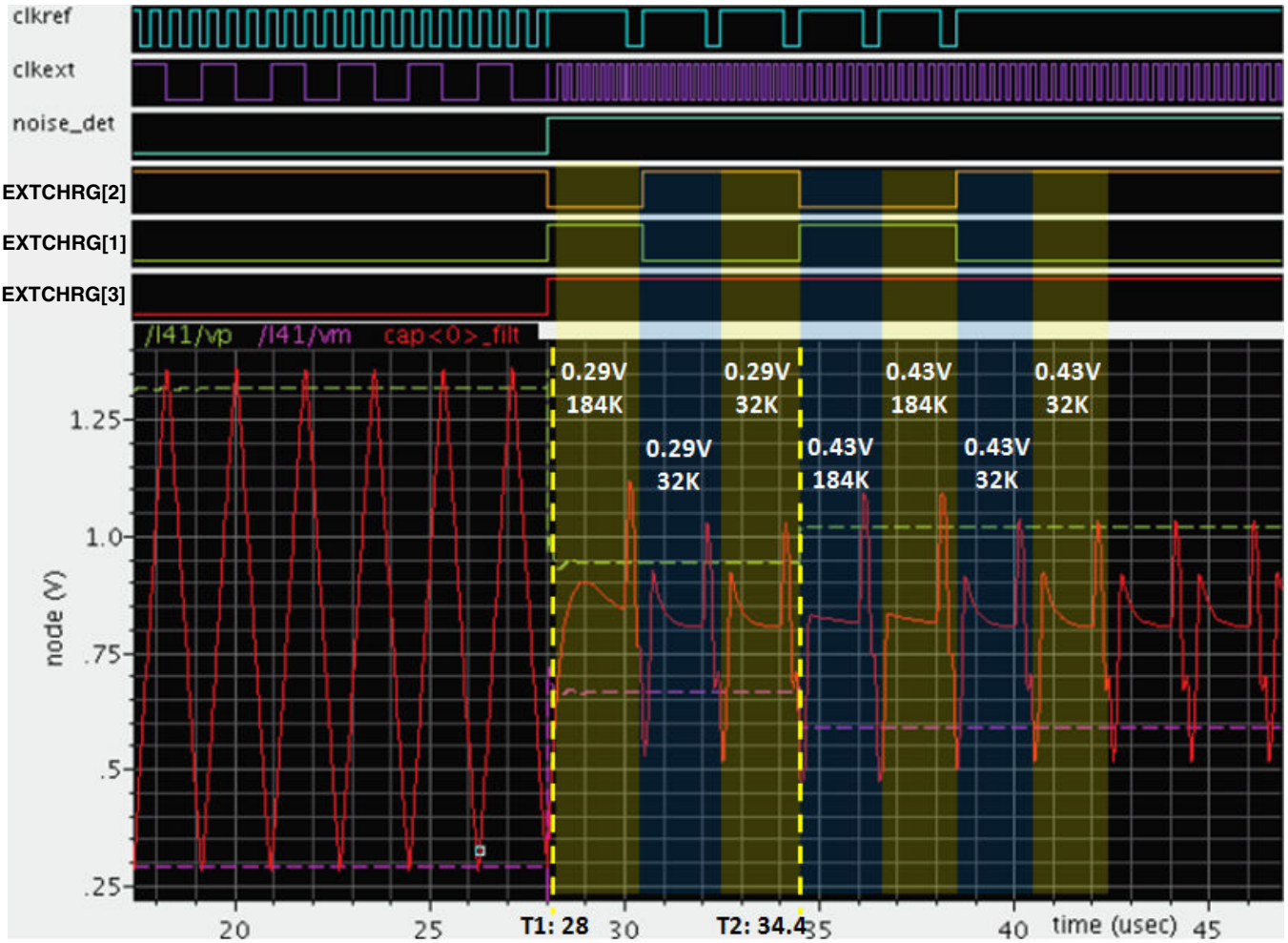


Figure 21-17. TSI noise detection mode waveform

22.5.6 CRC Polynomial 1 Register (CRC_P1)

P1 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 5h offset = 3065h

Bit	7	6	5	4	3	2	1	0
Read Write	P1							
Reset	0	0	0	0	0	0	0	0

CRC_P1 field descriptions

Field	Description
P1	CRC Polynominal Bit 23:16

22.5.7 CRC Polynomial 2 Register (CRC_P2)

P2 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 6h offset = 3066h

Bit	7	6	5	4	3	2	1	0
Read Write	P2							
Reset	0	0	0	1	0	0	0	0

CRC_P2 field descriptions

Field	Description
P2	CRC Polynominal Bit 15:8

Note

Before starting the refresh sequence, disable global interrupts. Otherwise, an interrupt could effectively invalidate the refresh sequence if writing the four bytes takes more than 16 bus clocks. Re-enable interrupts when the sequence is finished.

23.3.1.3 Example code: Refreshing the Watchdog

The following code segment shows the refresh write sequence of the WDOG module.

```
/* Refresh watchdog */

for (;;) // main loop
{
   ...

   DisableInterrupts; // disable global interrupt

   WDOG_CNT = 0xA602; // write the 1st refresh word

   WDOG_CNT = 0xB480; // write the 2nd refresh word to refresh counter

   EnableInterrupts; // enable global interrupt

   ...
}
```

23.3.2 Configuring the Watchdog

All watchdog control bits, timeout value, and window value are write-once after reset. This means that after a write has occurred they cannot be changed unless a reset occurs. This provides a robust mechanism to configure the watchdog and ensure that a runaway condition cannot mistakenly disable or modify the watchdog configuration after configured.

This is guaranteed by the user configuring the window and timeout value first, followed by the other control bits, and ensuring that CS1[UPDATE] is also set to 0. The new configuration takes effect only after all registers except WDOG_CNTH:L are written once after reset. Otherwise, the WDOG uses the reset values by default. If window mode is not used (CS2[WIN] is 0), writing to WDOG_WINH:L is not required to make the new configuration take effect.