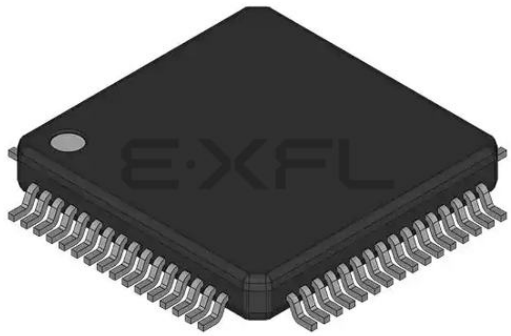

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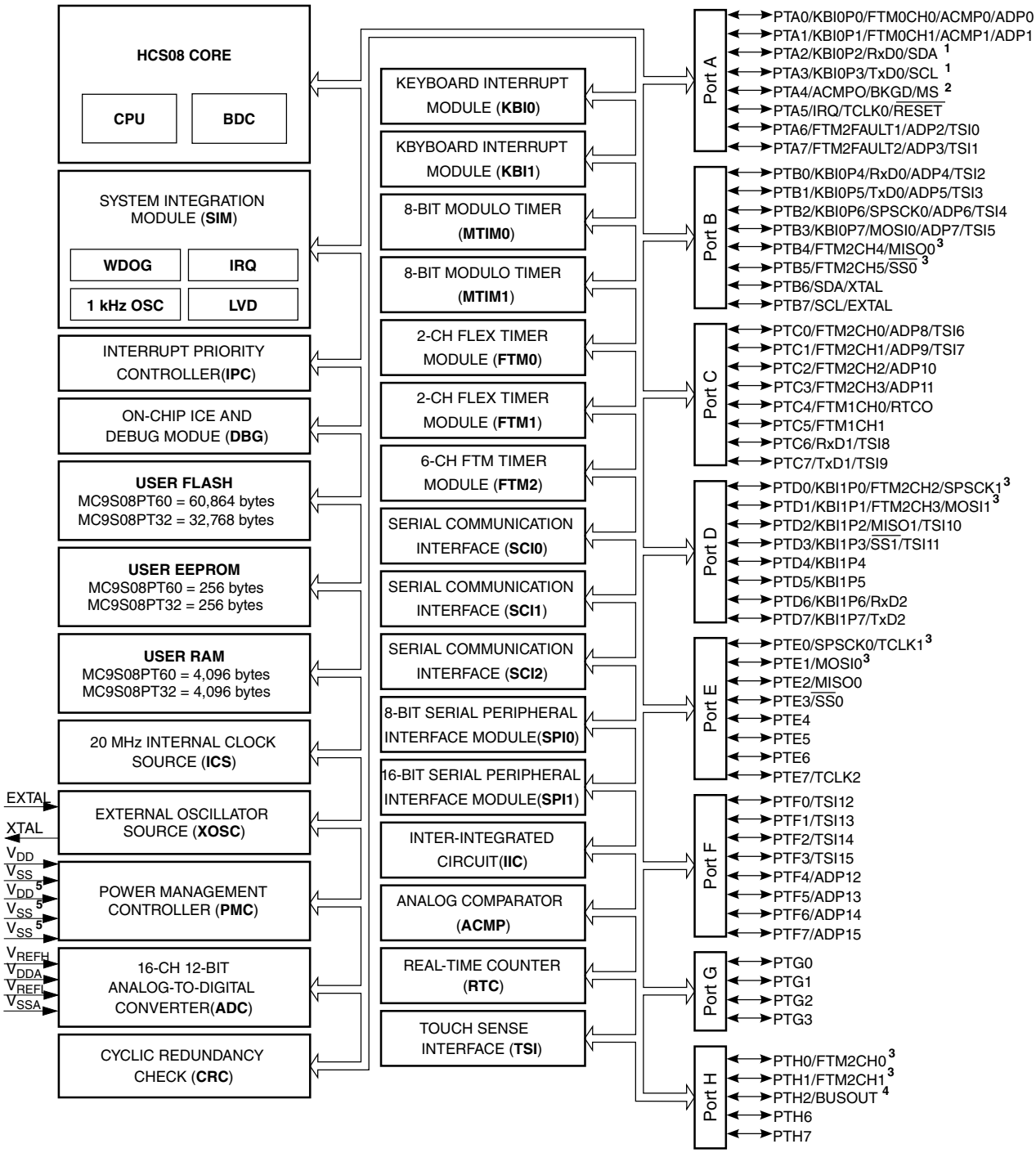
Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08pt32vlh

Chapter 5
Interrupt



1. PTA2 and PTA3 operate as true open drain when working as output.
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 1-1. MCU block diagram

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x303F	Reserved	—	—	—	—	—	—	—	—
0x3040	PMC_SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
0x3041	PMC_SPMSC2	—	LVDV	LVWV		—	—	—	—
0x3042-0x3049	Reserved	—	—	—	—	—	—	—	—
0x304A	SYS_ILLAH	Bit 15	14	13	12	11	19	9	Bit 8
0x304B	SYS_ILLAL	Bit 7	6	5	4	3	2	1	Bit 0
0x304C-0x304F	Reserved	—	—	—	—	—	—	—	—
0x3050	IPC_ILRS0	ILR3		ILR2		ILR1		ILR0	
0x3051	IPC_ILRS1	ILR7		ILR6		ILR5		ILR4	
0x3052	IPC_ILRS2	ILR11		ILR10		ILR9		ILR8	
0x3053	IPC_ILRS3	ILR15		ILR14		ILR13		ILR12	
0x3054	IPC_ILRS4	ILR19		ILR18		ILR17		ILR16	
0x3055	IPC_ILRS5	ILR23		ILR22		ILR21		ILR20	
0x3056	IPC_ILRS6	ILR27		ILR26		ILR25		ILR24	
0x3057	IPC_ILRS7	ILR31		ILR30		ILR29		ILR28	
0x3058	IPC_ILRS8	ILR35		ILR34		ILR33		ILR32	
0x3059	IPC_ILRS9	ILR39		ILR38		ILR37		ILR36	
0x305A-0x305F	Reserved	—	—	—	—	—	—	—	—
0x3060	CRC_D0	Bit 31	30	29	28	27	26	25	Bit 24
0x3061	CRC_D1	Bit 23	22	21	20	19	18	17	Bit 16
0x3062	CRC_D2	Bit 15	14	13	12	11	10	9	Bit 8
0x3063	CRC_D3	Bit 7	6	5	4	3	2	1	Bit 0
0x3064	CRC_P0	Bit 31	30	29	28	27	26	25	Bit 24
0x3065	CRC_P1	Bit 23	22	21	20	19	18	17	Bit 16
0x3066	CRC_P2	Bit 15	14	13	12	11	10	9	Bit 8
0x3067	CRC_P3	Bit 7	6	5	4	3	2	1	Bit 0
0x3068	CRC_CTRL	TOT		TOTR		0	FXOR	WAS	TCRC
0x3069	Reserved	—	—	—	—	—	—	—	—
0x306A	RTC_SC1	RTIF	RTIE	—	RTCO	—	—	—	—
0x306B	RTC_SC2	RTCLKS		—	—	—	RTCPS		
0x306C	RTC_MODH	MODH							
0x306D	RTC_MODL	MODL							
0x306E	RTC_CNTH	CNTH							
0x306F	RTC_CNTL	CNTL							
0x3070	I2C_A1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0x3071	I2C_F	MULT		ICR					
0x3072	I2C_C1	IICEN	IICIE	MST	TX	TXAK	RSTA	WUEN	—
0x3073	I2C_S	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
0x3074	I2C_D	DATA							

Table continues on the next page...

Table 4-46. Erase verify EEPROM section command error handling (continued)

Register	Error bit	Error condition
		Set if an invalid global address [23:0] is supplied
		Set if the requested section breaches the end of the EEPROM block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or it blank check failed.

4.5.2.9.14 Program EEPROM command

The program EEPROM operation programs one to four previously erased bytes in the EEPROM block. The program EEPROM operation will confirm that the targeted location(s) were successfully programmed upon completion.

Note

A EEPROM byte must be in the erased state before being programmed. Cumulative programming of bits within a EEPROM byte is not allowed.

Table 4-47. Program EEPROM command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x11	Global address [23:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010		Byte 0 program value
011		Byte 1 program value, if desired
100		Byte 2 program value, if desired
101		Byte 3 program value, if desired

Upon clearing NVM_FSTAT[CCIF] to launch the program EEPROM command, the user-supplied words will be transferred to the memory controller and be programmed if the area is unprotected. The CCOBIX index value at program EEPROM command launch determines how many bytes will be programmed in the EEPROM block. The NVM_FSTAT[CCIF] flag is set when the operation has completed.

Table 4-48. Program EEPROM command error handling

Register	Error Bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] >101 at command launch

Table continues on the next page...

NVM_FCLKDIV field descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset. 1 FCLKDIV register has been written since the last reset.
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing. 1 FDIV value is locked and cannot be changed. After the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in user mode.
FDIV	Clock Divider Bits FDIV[5:0] must be set to effectively divide BUSCLK down to 1MHz to control timed events during flash program and erase algorithms. Refer to the table in the Writing the FCLKDIV register for the recommended values of FDIV based on the BUSCLK frequency.

4.6.2 Flash Security Register (NVM_FSEC)

The FSEC register holds all bits associated with the security of the MCU and NVM module. All bits in the FSEC register are readable but not writable. During the reset sequence, the FSEC register is loaded with the contents of the flash security byte in the flash configuration field at global address 0xFF7F located in flash memory.

See Security for security function.

Address: 3020h base + 1h offset = 3021h

Bit	7	6	5	4	3	2	1	0
Read	KEYEN		Reserved				SEC	
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

NVM_FSEC field descriptions

Field	Description
7–6 KEYEN	Backdoor Key Security Enable Bits The KEYEN[1:0] bits define the enabling of backdoor key access to the flash module. **NOTE:** 01 is the preferred KEYEN state to disable backdoor key access. 00 Disabled 01 Disabled 10 Enabled 11 Disabled

Table continues on the next page...

PORT_PTED field descriptions (continued)

Field	Description
	Reset forces PTED to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.6 Port F Data Register (PORT_PTFD)

Address: 0h base + 5h offset = 5h

Bit	7	6	5	4	3	2	1	0
Read Write	PTFD							
Reset	0	0	0	0	0	0	0	0

PORT_PTFD field descriptions

Field	Description
PTFD	Port F Data Register Bits For port F pins that are configured as inputs, a read returns the logic level on the pin. For port F pins that are configured as outputs, a read returns the last value that was written to this register. For port F pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port F pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTFD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.7 Port G Data Register (PORT_PTGD)

Address: 0h base + 6h offset = 6h

Bit	7	6	5	4	3	2	1	0
Read	0				PTGD			
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGD field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PTGD	Port G Data Register Bits For port G pins that are configured as inputs, a read returns the logic level on the pin. For port G pins that are configured as outputs, a read returns the last value that was written to this register.

Table continues on the next page...

7.7.21 Port D Input Enable Register (PORT_PTDIE)

Address: 0h base + 30BBh offset = 30BBh

Bit	7	6	5	4	3	2	1	0
Read Write	PTDIE7	PTDIE6	PTDIE5	PTDIE4	PTDIE3	PTDIE2	PTDIE1	PTDIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTDIE field descriptions

Field	Description
7 PTDIE7	Input Enable for Port D Bit 7 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 7. 1 Input enabled for port D bit 7.
6 PTDIE6	Input Enable for Port D Bit 6 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 6. 1 Input enabled for port D bit 6.
5 PTDIE5	Input Enable for Port D Bit 5 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 5. 1 Input enabled for port D bit 5.
4 PTDIE4	Input Enable for Port D Bit 4 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 4. 1 Input enabled for port D bit 4.
3 PTDIE3	Input Enable for Port D Bit 3 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 3. 1 Input enabled for port D bit 3.
2 PTDIE2	Input Enable for Port D Bit 2 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 2. 1 Input enabled for port D bit 2.
1 PTDIE1	Input Enable for Port D Bit 1 This read/write bit enables the port D pin as an input.

Table continues on the next page...

7.7.37 Port H Pullup Enable Register (PORT_PTHPE)

Address: 0h base + 30F7h offset = 30F7h

Bit	7	6	5	4	3	2	1	0
Read	PTHPE7	PTHPE6	0			PTHPE2	PTHPE1	PTHPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTHPE field descriptions

Field	Description
7 PTHPE7	Pull Enable for Port H Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 7. 1 Pullup enabled for port H bit 7.
6 PTHPE6	Pull Enable for Port H Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 6. 1 Pullup enabled for port H bit 6.
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHPE2	Pull Enable for Port H Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 2. 1 Pullup enabled for port H bit 2.
1 PTHPE1	Pull Enable for Port H Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 1. 1 Pullup enabled for port H bit 1.
0 PTHPE0	Pull Enable for Port H Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 0. 1 Pullup enabled for port H bit 0.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop locks the frequency to the 512 times the internal reference frequency. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

8.2.2.2 FLL engaged external (FEE)

The FLL engaged external (FEE) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 00b
- ICS_C1[IREFS] bit written to 0b
- ICS_C1[RDIV] bits are written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the external reference clock source. The FLL loop locks the frequency to the 512 times the external reference frequency, as selected by the ICS_C1[RDIV] bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

8.2.2.3 FLL bypassed internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 01
- ICS_C1[IREFS] bit is written to 1
- BDM mode is active or ICS_C2[LP] bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop locks the FLL frequency to the 512 times the internal reference frequency. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

SCG_C2 field descriptions (continued)

Field	Description
	0 Bus clock to the NVM module is disabled. 1 Bus clock to the NVM module is enabled.
3 IPC	IPC Clock Gate Control This bit controls the clock gate to the IPC module. 0 Bus clock to the IPC module is disabled. 1 Bus clock to the IPC module is enabled.
2 CRC	CRC Clock Gate Control This bit controls the clock gate to the CRC module. 0 Bus clock to the CRC module is disabled. 1 Bus clock to the CRC module is enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

8.7.3 System Clock Gating Control 3 Register (SCG_C3)

This high page register contains control bits to enable or disable the bus clock to the SCI, SPI, IIC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 300Ch base + 2h offset = 300Eh

Bit	7	6	5	4	3	2	1	0
Read	0	SCI2	SCI1	SCI0	SPI1	SPI0	IIC	0
Write								
Reset	0	1	1	1	1	1	1	0

SCG_C3 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 SCI2	SCI2 Clock Gate Control This bit controls the clock gate to the SCI2 module.

Table continues on the next page...

The MTIM counter (MTIM_CNT) has three modes of operation: stopped, free-running, and modulo. Out of reset, the counter is stopped. If the counter is started without writing a new value to the modulo register, then the counter will be in free-running mode. The counter is in modulo mode when a value other than 0x00 is in the modulo register while the counter is running.

After any MCU reset, the counter is stopped and reset to 0x00, and the modulus is set to 0x00. The bus clock is selected as the default clock source and the prescale value is divide by 1. To start the MTIM in free-running mode, simply write to the MTIM status and control register (MTIM_SC), and clear the MTIM stop bit (TSTP).

Four clock sources are software selectable: the internal bus clock, the fixed frequency clock (XCLK), and an external clock on the TCLK pin, selectable as incrementing on either rising or falling edges. The MTIM clock select bits, CLKS1:CLKS0, in MTIM_CLK are used to select the desired clock source. If the counter is active (SC[TSTP] = 0) when a new clock source is selected, the counter will continue counting from the previous value using the new clock source.

Nine prescale values are software selectable: clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256. The prescaler select bits (CLK[PS]) in MTIM_CLK select the desired prescale value. If the counter is active (SC[TSTP] = 0) when a new prescaler value is selected, the counter will continue counting from the previous value using the new prescaler value.

The MTIM modulo register (MTIM_MOD) allows the overflow compare value to be set to any value from 0x01 to 0xFF. Reset clears the modulo value to 0x00, which results in a free running counter.

When the counter is active (SC[TSTP] = 0), the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter overflows to 0x00 and continues counting. The MTIM overflow flag (SC[TOF]) is set whenever the counter overflows. The flag sets on the transition from the modulo value to 0x00. Writing to MTIM_MOD while the counter is active resets the counter to 0x00 and clears SC[TOF].

Clearing SC[TOF] is a two-step process. The first step is to read the MTIM_SC register while SC[TOF] is set. The second step is to write a 0 to SC[TOF]. If another overflow occurs between the first and second step, the clearing process is reset and SC[TOF] will remain set after the second step is performed. This will prevent the second occurrence from being missed. SC[TOF] is also cleared when a 1 is written to SC[TRST] or when any value is written to the MTIM_MOD register.

RTC_MODL field descriptions (continued)

Field	Description
	These sixteen read/write bits, MODH and MODL, contain the modulo value used to reset the count to 0x0000 upon a compare match and set the RTIF status bit. A value of 0x00 of the MODH an MODL sets the RTIF bit on each rising edge of the prescaler output. Reset sets the modulo to 0x00.

14.4.5 RTC Counter Register: High (RTC_CNTH)

RTC_CNTH, together with RTC_CNTL, indicates the read-only value of the current RTC count of the 16-bit counter.

NOTE

The RTC_CNTL must be read first to lock the counter and then read RTC_CNTH to correctly read 16-bit counter.

Address: 306Ah base + 4h offset = 306Eh

Bit	7	6	5	4	3	2	1	0
Read	CNTH							
Write								
Reset	0	0	0	0	0	0	0	0

RTC_CNTH field descriptions

Field	Description
CNTH	RTC Count High CNTH and CNTL contain the current value of the 16-bit counter. Writes have no effect to this register. Reset or writing different values to RTCLKS and RTCPS clear the count to 0x00.

14.4.6 RTC Counter Register: Low (RTC_CNTL)

RTC_CNTL, together with RTC_CNTH, indicates the read-only value of the current RTC count of the 16-bit counter.

Address: 306Ah base + 5h offset = 306Fh

Bit	7	6	5	4	3	2	1	0
Read	CNTL							
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_S2 field descriptions (continued)

Field	Description
	0 No LIN break character has been detected. 1 LIN break character has been detected.
6 RXEDGIF	RxD Pin Active Edge Interrupt Flag RXEDGIF is set when an active edge, falling if RXINV = 0, rising if RXINV=1, on the RxD pin occurs. RXEDGIF is cleared by writing a 1 to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 RXINV	Receive Data Inversion Setting this bit reverses the polarity of the received data input. **NOTE:** Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle. 0 Receive data not inverted. 1 Receive data inverted.
3 RWUID	Receive Wake Up Idle Detect RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character.
2 BRK13	Break Character Generation Length BRK13 selects a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is transmitted with length of 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is transmitted with length of 13 bit times (if M = 0, SBNS = 0) or 14 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 15 (if M = 1, SBNS = 1).
1 LBKDE	LIN Break Detection Enable LBKDE selects a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character is detected at length 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is detected at length of 11 bit times (if M = 0, SBNS = 0) or 12 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 13 (if M = 1, SBNS = 1).
0 RAF	Receiver Active Flag RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

16.5.2 Pseudo-Code Example

In this example, the SPI module will be set up for master mode with only hardware match interrupts enabled. The SPI will run at a maximum baud rate of bus clock divided by 2. Clock phase and polarity will be set for an active-high SPI clock where the first edge on SPSCK occurs at the start of the first cycle of a data transfer.

SPIx_C1=0x54(%01010100)				
Bit 7	SPIE	=	0	Disables receive and mode fault interrupts
Bit 6	SPE	=	1	Enables the SPI system
Bit 5	SPTIE	=	0	Disables SPI transmit interrupts
Bit 4	MSTR	=	1	Sets the SPI module as a master SPI device
Bit 3	CPOL	=	0	Configures SPI clock as active-high
Bit 2	CPHA	=	1	First edge on SPSCK at start of first data transfer cycle
Bit 1	SSOE	=	0	Determines SS pin function when mode fault enabled
Bit 0	LSBFE	=	0	SPI serial data transfers start with most significant bit

SPIx_C2 = 0x80(%10000000)				
Bit 7	SPMIE	=	1	SPI hardware match interrupt enabled
Bit 6		=	0	Unimplemented
Bit 5		=	0	Reserved
Bit 4	MODFEN	=	0	Disables mode fault function
Bit 3	BIDIROE	=	0	SPI data I/O pin acts as input
Bit 2		=	0	Reserved
Bit 1	SPISWAI	=	0	SPI clocks operate in wait mode
Bit 0	SPC0	=	0	uses separate pins for data input and output

SPIx_BR = 0x00(%00000000)				
Bit 7		=	0	Reserved
Bit 6:4		=	000	Sets prescale divisor to 1
Bit 3:0		=	0000	Sets baud rate divisor to 2

SPIx_S = 0x00(%00000000)				
Bit 7	SPRF	=	0	Flag is set when receive data buffer is full
Bit 6	SPMF	=	0	Flag is set when SPI_M = receive data buffer
Bit 5	SPTEF	=	0	Flag is set when transmit data buffer is empty
Bit 4	MODF	=	0	Mode fault flag for master mode
Bit 3:0		=	0	Reserved

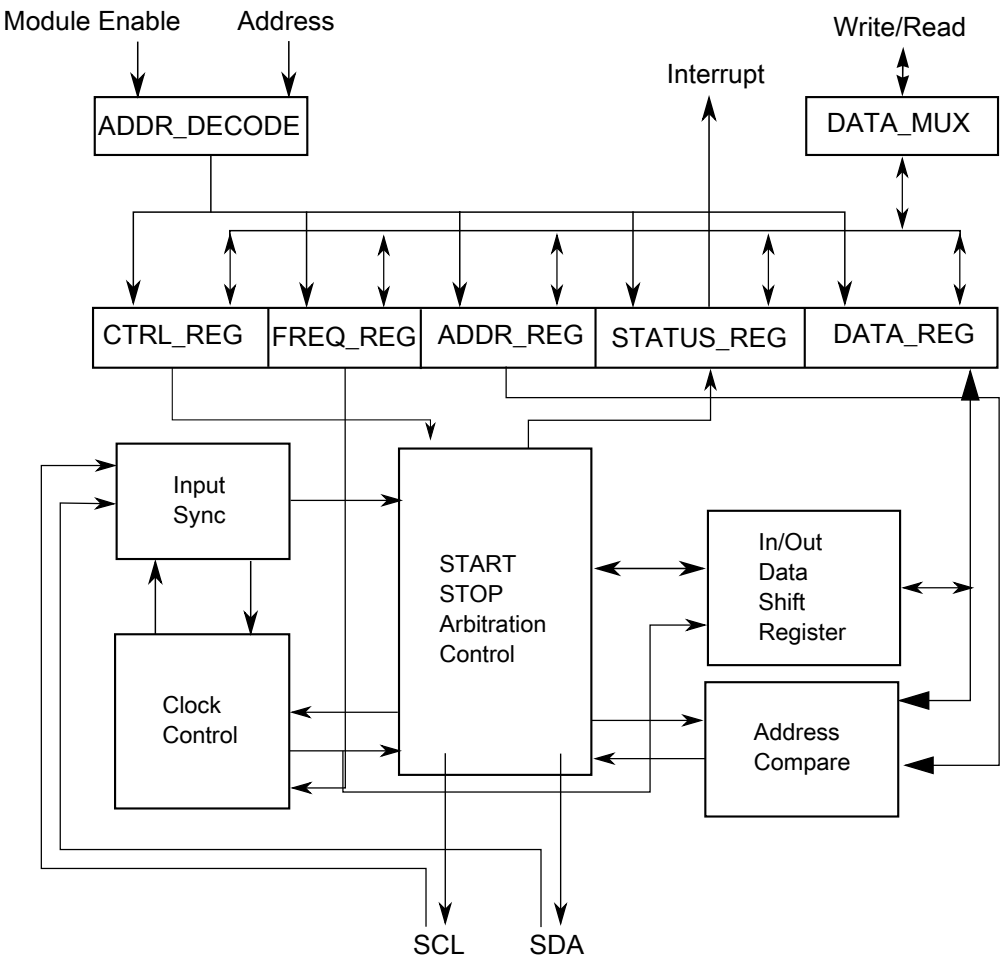


Figure 18-1. I2C Functional block diagram

18.2 I²C signal descriptions

The signal properties of I²C are shown in the table found here.

Table 18-1. I²C signal descriptions

Signal	Description	I/O
SCL	Bidirectional serial clock line of the I²C system.	I/O
SDA	Bidirectional serial data line of the I²C system.	I/O

19.4.7 MCU wait mode operation

Wait mode is a low-power consumption standby mode from which recovery is fast because the clock sources remain active. If a conversion is in progress when the MCU enters wait mode, it continues until completion. Conversions can be initiated while the MCU is in wait mode by means of the hardware trigger or if continuous conversions are enabled.

The bus clock, bus clock divided by two, ALTCLK and ADACK are available as conversion clock sources while in wait mode.

ADC_SC1[COCO] is set by a conversion complete event that generates an ADC interrupt to wake the MCU from wait mode if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1).

19.4.8 MCU Stop3 mode operation

Stop3 mode is a low-power consumption standby mode during which most or all clock sources on the MCU are disabled.

19.4.8.1 Stop3 mode with ADACK disabled

If the asynchronous clock, ADACK, is not selected as the conversion clock, executing a STOP instruction aborts the current conversion and places the ADC in its idle state. The contents of ADC_RH and ADC_RL are unaffected by Stop3 mode. After exiting from Stop3 mode, a software or hardware trigger is required to resume conversions.

19.4.8.2 Stop3 mode with ADACK enabled

If ADACK is selected as the conversion clock, the ADC continues operation during Stop3 mode. For guaranteed ADC operation, the MCU's voltage regulator must remain active during Stop3 mode. See the module introduction for configuration information for this MCU.

If a conversion is in progress when the MCU enters Stop3 mode, it continues until completion. Conversions can be initiated while the MCU is in Stop3 mode by means of the hardware trigger or if continuous conversions are enabled.

21.3.1 TSI Control and Status Register 0 (TSI_CS0)

This control register provides various control and configuration information for the TSI module.

NOTE

When TSI is working, the configuration bits (CS0[TSIEN], CS0[TSIIEN], and CS0[STM]) must not be changed. The EOSF flag is kept until the software acknowledge it.

Address: 8h base + 0h offset = 8h

Bit	7	6	5	4	3	2	1	0
Read	TSIEN	TSIIEN	STPE	STM	SCNIP	EOSF	CURSW	0
Write								SWTS
Reset	0	0	0	0	0	0	0	0

TSI_CS0 field descriptions

Field	Description
7 TSIEN	TSIEN This bit enables TSI module. 0 TSI module disabled. 1 TSI module enabled.
6 TSIIEN	TSIIEN This bit enables TSI module interrupt request to CPU when the scan completes. The interrupt will wake MCU from stop3 mode if this interrupt is enabled. 0 TSI interrupt disabled. 1 TSI interrupt enabled.
5 STPE	STPE This bit enables TSI module function in stop3 mode. When this bit is set, TSI can be woken by external hardware trigger, start scan and submit interrupt request to wake CPU when the scan completes. 0 TSI disabled in stop3 mode. 1 TSI enabled in stop3 mode.
4 STM	STM This bit specifies the trigger mode. When this bit is clear, the software trigger mode is applied to write "1" to SWTS bit to start scan. When this bit is set, the hardware trigger mode is applied. 0 Software trigger scan. 1 Hardware trigger scan.
3 SCNIP	SCNIP This read-only bit indicates if scan is in progress. When this bit reads zero, there is no scan in progress. When this bit reads set, a scan is in progress.

Table continues on the next page...

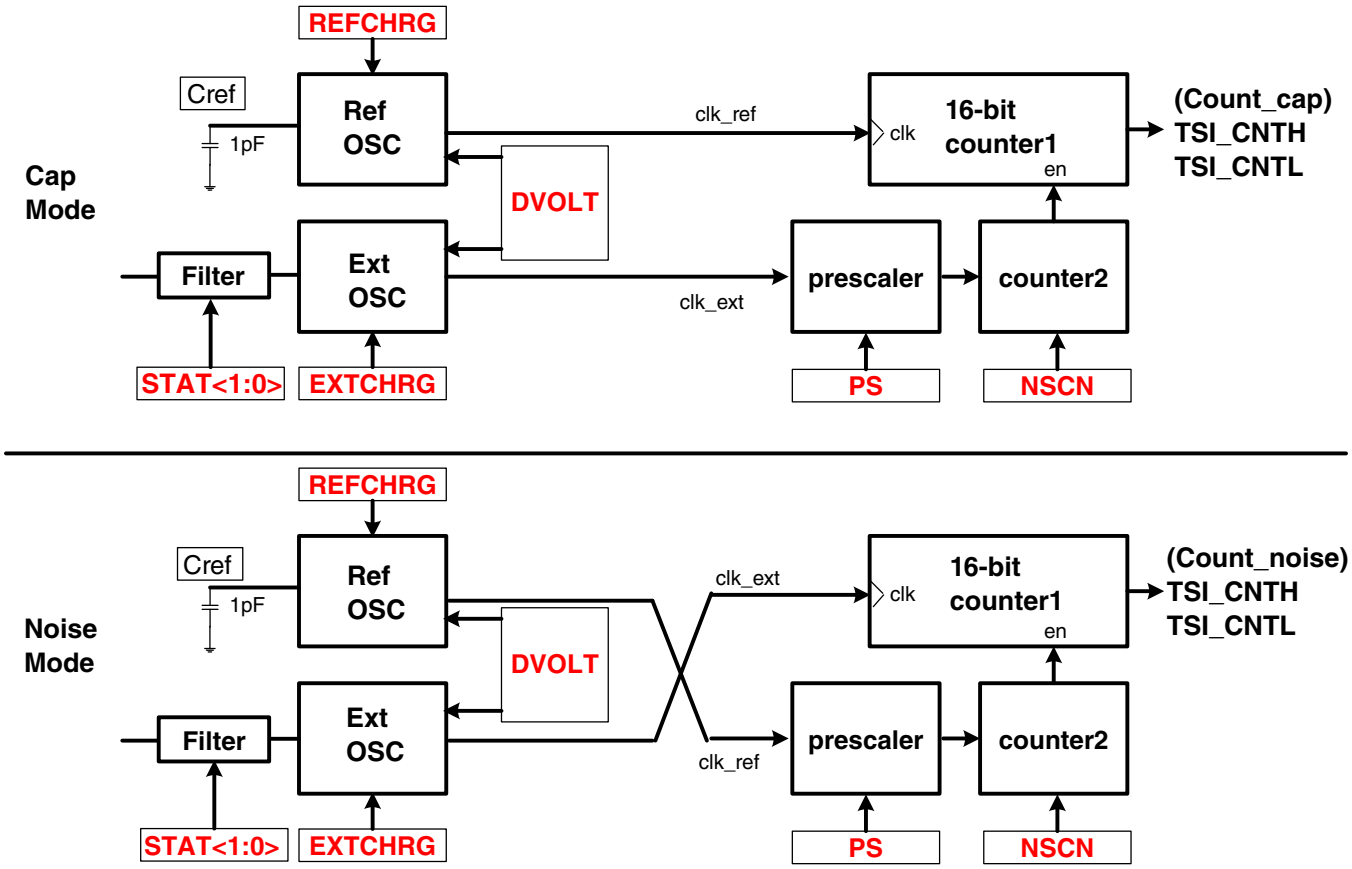


Figure 21-13. TSI noise detection mode block diagram

CRC_CTRL field descriptions (continued)

Field	Description
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 FXOR	Complement of Read This bit allows CRC module to output the complement of the final CRC checksum. 0 Normal checksum output. 1 Complement of checksum output.
1 WAS	Write CRC data register as seed This bit indicates the data written to the CRC data register (D0:D3) is seed or data. 0 Data is written in data registers. 1 Seed is written in data registers.
0 TCRC	Width of Polynomial Generator This bit indicates the bit width of the polynomial generator. 0 16-bit CRC Polynomial Generator. 1 32-bit CRC Polynomial Generator.

22.6 Functional description

22.6.1 16-bit CRC calculation

The following steps show how to start a general 16-bit CRC calculation:

1. Clear CRC_CTRL[TCRC] bit to enable 16-bit CRC mode.
2. Optional to enable reverse and complement function. Please see Bit reverse and Result complement for details.
3. Write 16-bit polynomial to CRC_P2:CRC_P3.
4. Set CRC_CTRL[WAS] bit to allow CRC_D2:CRC_D3 to be written by seed.
5. Write 16-bit seed to CRC_D2:CRC_D3.
6. Clear CRC_CTRL[WAS] bit to start 16-bit CRC calculation.
7. Dummy CRC_D3 with 8-bit CRC raw data.
8. Get the checksum from CRC_D2:CRC_D3 when all CRC raw data dummied.

22.6.2 32-bit CRC calculation

The following steps show how to start a general 32-bit CRC calculation:

1. Set CRC_CTRL[TCRC] bit to enable 32-bit CRC mode.

DBG_CBL field descriptions

Field	Description
CB[7:0]	Comparator B Low The Comparator B Low compare bits control whether Comparator B will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

25.3.5 Debug Comparator C High Register (DBG_CCH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 4h offset = 3014h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CCH field descriptions

Field	Description
CC[15:8]	Comparator C High Compare Bits The Comparator C High compare bits control whether Comparator C will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.