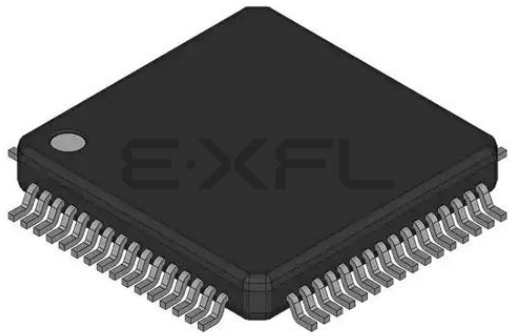

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
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Number of I/O	57
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08pt32vqh

2.2.3 Oscillator (XTAL, EXTAL)

The XTAL and EXTAL pins are used to provide the connections for the on-chip oscillator. The oscillator (XOSC) in this MCU is a Pierce oscillator that can accommodate a crystal or ceramic resonator. Optionally, an external clock source can be connected to the EXTAL input pin. The oscillator can be configured to run in stop3 mode.

Refer to the following figure, R_S (when used) and R_F must be low-inductance resistors such as carbon composition resistors. Wire-wound resistors, and some metal film resistors, have too much inductance. C1 and C2 normally must be high-quality ceramic capacitors that are specifically designed for high-frequency applications.

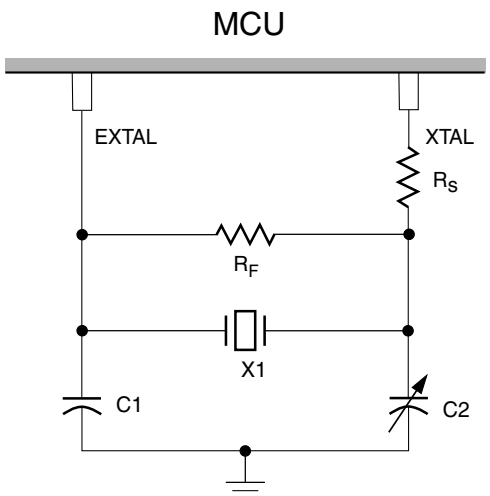


Figure 2-7. Typical crystal or resonator circuit

R_F is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup; its value is not generally critical. Typical systems use 1 M to 10 M. Higher values are sensitive to humidity and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5 pF to 25 pF range and are chosen to match the requirements of a specific crystal or resonator. Take into account printed circuit board (PCB) capacitance and MCU pin capacitance when selecting C1 and C2. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C1 and C2 (which are usually the same size). As a first-order approximation, use 10 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x303F	Reserved	—	—	—	—	—	—	—	—
0x3040	PMC_SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
0x3041	PMC_SPMSC2	—	LVDV	LVWV		—	—	—	—
0x3042-0x3049	Reserved	—	—	—	—	—	—	—	—
0x304A	SYS_ILLAH	Bit 15	14	13	12	11	19	9	Bit 8
0x304B	SYS_ILLAL	Bit 7	6	5	4	3	2	1	Bit 0
0x304C-0x304F	Reserved	—	—	—	—	—	—	—	—
0x3050	IPC_ILRS0	ILR3		ILR2		ILR1		ILR0	
0x3051	IPC_ILRS1	ILR7		ILR6		ILR5		ILR4	
0x3052	IPC_ILRS2	ILR11		ILR10		ILR9		ILR8	
0x3053	IPC_ILRS3	ILR15		ILR14		ILR13		ILR12	
0x3054	IPC_ILRS4	ILR19		ILR18		ILR17		ILR16	
0x3055	IPC_ILRS5	ILR23		ILR22		ILR21		ILR20	
0x3056	IPC_ILRS6	ILR27		ILR26		ILR25		ILR24	
0x3057	IPC_ILRS7	ILR31		ILR30		ILR29		ILR28	
0x3058	IPC_ILRS8	ILR35		ILR34		ILR33		ILR32	
0x3059	IPC_ILRS9	ILR39		ILR38		ILR37		ILR36	
0x305A-0x305F	Reserved	—	—	—	—	—	—	—	—
0x3060	CRC_D0	Bit 31	30	29	28	27	26	25	Bit 24
0x3061	CRC_D1	Bit 23	22	21	20	19	18	17	Bit 16
0x3062	CRC_D2	Bit 15	14	13	12	11	10	9	Bit 8
0x3063	CRC_D3	Bit 7	6	5	4	3	2	1	Bit 0
0x3064	CRC_P0	Bit 31	30	29	28	27	26	25	Bit 24
0x3065	CRC_P1	Bit 23	22	21	20	19	18	17	Bit 16
0x3066	CRC_P2	Bit 15	14	13	12	11	10	9	Bit 8
0x3067	CRC_P3	Bit 7	6	5	4	3	2	1	Bit 0
0x3068	CRC_CTRL	TOT		TOTR		0	FXOR	WAS	TCRC
0x3069	Reserved	—	—	—	—	—	—	—	—
0x306A	RTC_SC1	RTIF	RTIE	—	RTCO	—	—	—	—
0x306B	RTC_SC2	RTCLKS		—	—	—	RTCPS		
0x306C	RTC_MODH	MODH							
0x306D	RTC_MODL	MODL							
0x306E	RTC_CNTH	CNTH							
0x306F	RTC_CNTL	CNTL							
0x3070	I2C_A1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0x3071	I2C_F	MULT		ICR					
0x3072	I2C_C1	IICEN	IICIE	MST	TX	TXAK	RSTA	WUEN	—
0x3073	I2C_S	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
0x3074	I2C_D	DATA							

Table continues on the next page...

- Ability to read the flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of flash memory

EEPROM features:

- 256 bytes of EEPROM memory composed of one 256 byte EEPROM block divided into 128 sectors of 2 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verification and generation of ECC parity bits
- Fast sector erase and byte program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four bytes in a burst sequence

Other features

- No external high-voltage power supply required for flash memory program and erase operations
- Interrupt generation on flash command completion and flash error detection
- Security mechanism to prevent unauthorized access to the flash memory

4.5.2 Function descriptions

4.5.2.1 Modes of operation

The flash and EEPROM module provides the normal user mode of operation. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers.

4.5.2.1.1 Wait mode

The flash and EEPROM module is not affected if the MCU enters wait mode. The flash module can recover the MCU from wait via the CCIF interrupt. See Flash and EEPROM interrupts.

4.5.2.1.2 Stop mode

If a flash and EEPROM command is active, that is, FSTAT[CCIF] = 0, when the MCU requests stop mode, the current NVM operation will be completed before the MCU is allowed to enter stop mode.

Chapter 6
System control

6.1 System device identification (SDID)

This device is hard coded to the value 0x0040 in SDID registers.

6.2 Universally unique identification (UUID)

This device contains up to 64-bit UUID to identify each device in this family. The intent of UUID is to enable distributed systems to uniquely identify information without significant central coordination.

6.3 Reset and system initialization

Resetting the MCU provides a way to start processing from a set of known initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with disabled pullup devices. The CCR[I] bit is set to block maskable interrupts so that the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

This device has the following sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Watchdog (WDOG) timer
- Illegal opcode detect (ILOP)

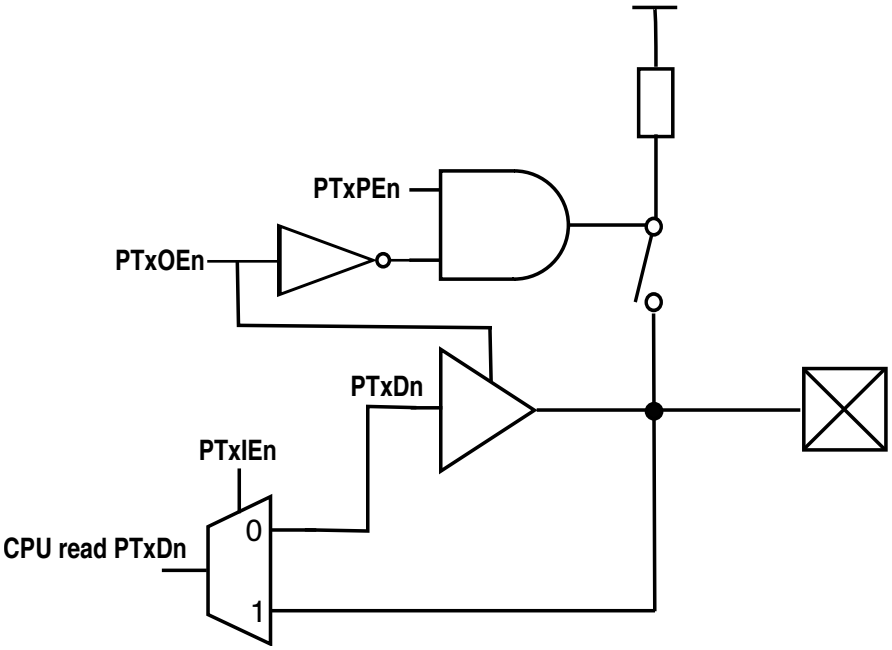


Figure 7-1. Normal I/O structure

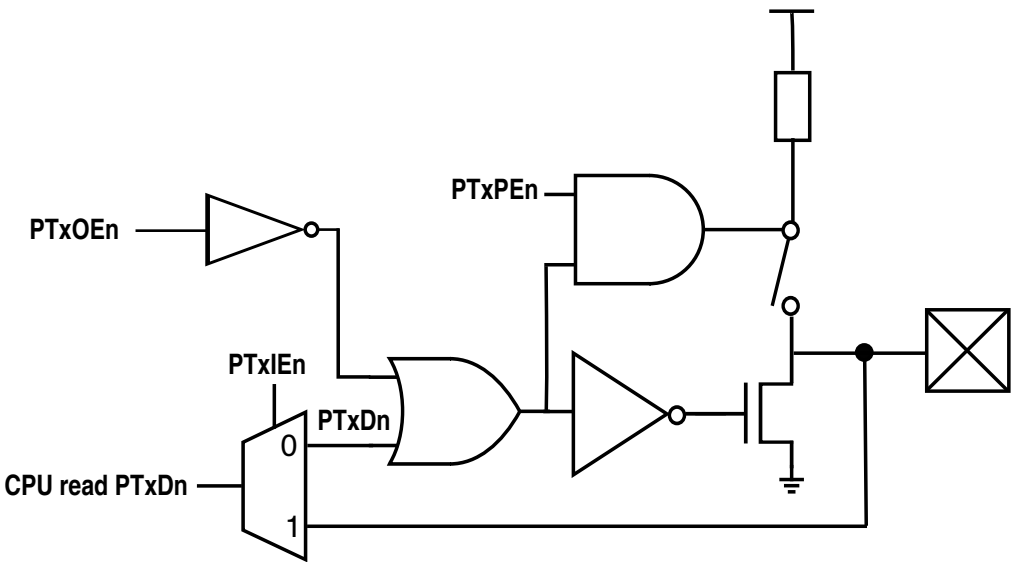


Figure 7-2. SDA(PTA2)/SCL(PTA3) structure

PORT_PTDPE field descriptions (continued)

Field	Description
2 PTDPE2	Pull Enable for Port D Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 2. 1 Pullup enabled for port D bit 2.
1 PTDPE1	Pull Enable for Port D Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 1. 1 Pullup enabled for port D bit 1.
0 PTDPE0	Pull Enable for Port D Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 0. 1 Pullup enabled for port D bit 0.

7.7.34 Port E Pullup Enable Register (PORT_PTEPE)

Address: 0h base + 30F4h offset = 30F4h

Bit	7	6	5	4	3	2	1	0
Read Write	PTEPE7	PTEPE6	PTEPE5	PTEPE4	PTEPE3	PTEPE2	PTEPE1	PTEPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTEPE field descriptions

Field	Description
7 PTEPE7	Pull Enable for Port E Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 7. 1 Pullup enabled for port E bit 7.
6 PTEPE6	Pull Enable for Port E Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 6. 1 Pullup enabled for port E bit 6.
5 PTEPE5	Pull Enable for Port E Bit 5

Table continues on the next page...

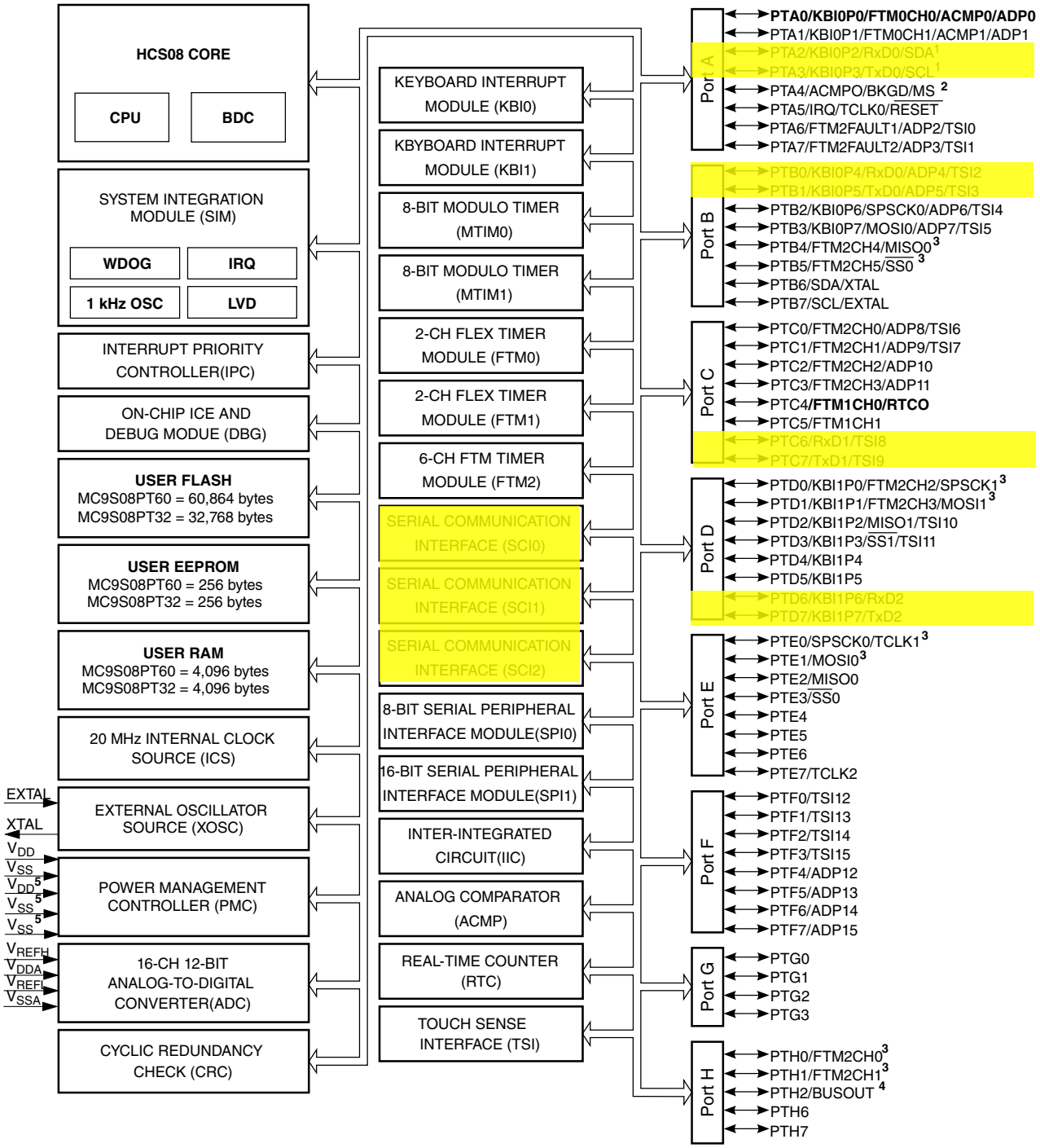
- BDIV=100 (divide by 16), NA
- BDIV=101 (divide by 32), NA
- BDIV=110 (divide by 64), NA
- BDIV=111 (divide by 128), NA

8.2.1.5 BDC clock

The ICS presents the DCO output clock divided by two as ICSLCLK for use as a clock source for BDC communications. ICSLCLK is not available in FLL bypassed internal low power (FBILP) and FLL bypassed external low power (FBELP) modes. The ICSLCLK can be selected as BDC clock.

8.2.2 Modes of operation

There are seven modes of operation for the ICS: FEI, FEE, FBI, FBILP, FBE, FBELP, and stop. The following figure shows the seven states of the ICS as a state diagram. The arrows indicate the allowed movements between the states.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 can provide ultra-high source/sink current up to 20 mA.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-6. Device block diagram highlighting SCI modules and pins

FTMx_MODE field descriptions (continued)

Field	Description
4 CAPTEST	Capture Test Mode Enable Enables the capture test mode. CAPTEST bit is write protected. This bit can be written only if WPDIS = 1. 0 Capture test mode is disabled. 1 Capture test mode is enabled.
3 PWMSYNC	PWM Synchronization Mode Selects which triggers can be used by MOD, CV, CHnOM, and FTM counter synchronization (PWM synchronization). 0 No restrictions. Software and hardware triggers can be used by MOD, CV, CHnOM, and FTM counter synchronization. 1 Software trigger can be used only by MOD and CV synchronization, and hardware triggers can be used only by CHnOM and FTM counter synchronization.
2 WPDIS	Write Protection Disable When write protection is enabled (MODE[WPDIS] = 0), write protected bits can not be written. When write protection is disabled (MODE[WPDIS] = 1), write protected bits can be written. The WPDIS bit is the negation of the WPEN bit. WPDIS is cleared when 1 is written to WPEN. WPDIS is set when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPDIS has no effect. 0 Write protection is enabled. 1 Write protection is disabled.
1 INIT	Initialize the Output Channels When a 1 is written to INIT bit the output channels are initialized according to the state of their corresponding bit in the OUTINIT register. Writing a 0 to INIT bit has no effect. The INIT bit is always read as 0.
0 FTMEN	FTM Enable This bit is write protected, and can be written only if WPDIS = 1. 0 Only the TPM-compatible registers (first set of registers) can be used without any restriction. Do not use the FTM-specific registers. 1 All registers including the FTM-specific registers (second set of registers) are available for use with no restrictions.

12.3.15 Synchronization (FTMx_SYNC)

This register configures the PWM synchronization.

A synchronization event can perform the synchronized update of MOD, CV, and OUTMASK registers with the value of their write buffer and the FTM counter initialization.

The FTM period when using up counting is (MODH:L – CNTINH:L + 0x0001) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MODH:L to CNTINH:L.

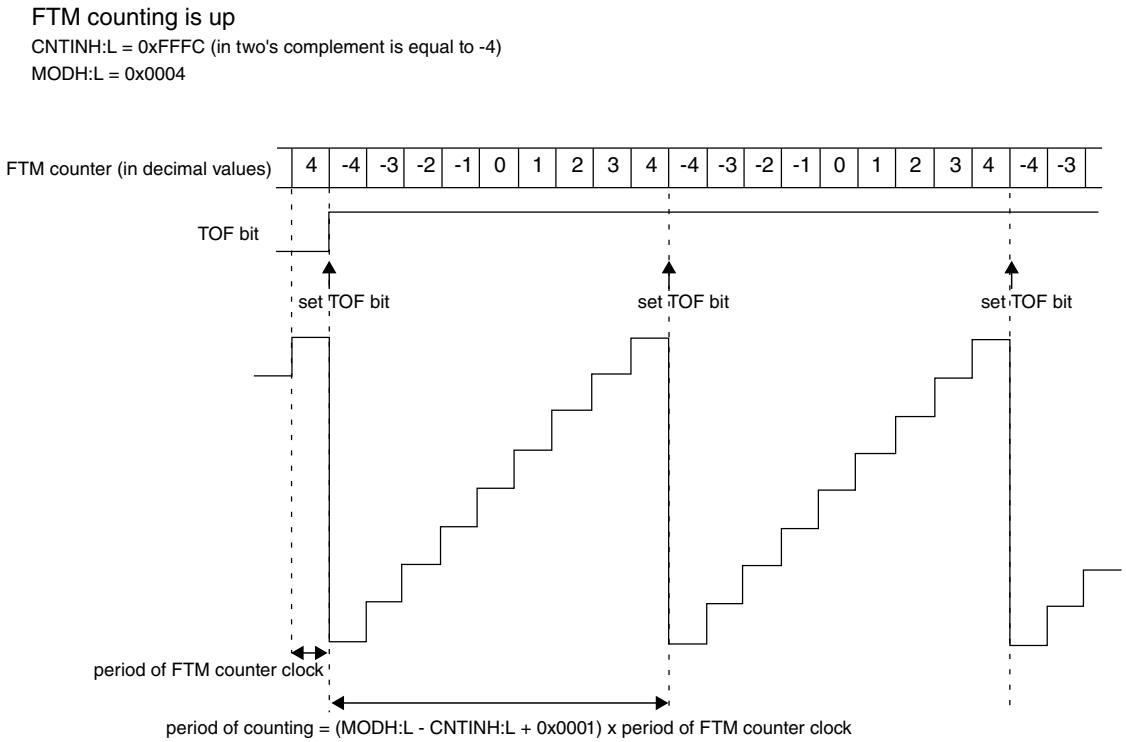


Figure 12-188. Example of FTM up and signed counting

If (CNTINH:L = 0x0000), the FTM counting is equivalent to TPM up counting; that is, up and unsigned counting. See the following figure. If (CNTINH[7] = 1), then the initial value of the FTM counter is a negative number in two's complement format, so the FTM counting is up and signed. Conversely, if (CNTINH[7] = 0 and CNTINH:L ≠ 0x0000), then the initial value of the FTM counter is a positive number, therefore the FTM counting is up and unsigned.

When a rising edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n) capture buffer. The channel (n) capture buffer value is transferred to C(n)VH:L registers when a falling edge occurs in the channel (n) input signal. C(n)VH:L registers have the FTM counter value when the previous rising edge occurred, and the channel (n) capture buffer has the FTM counter value when the last rising edge occurred.

When a negative edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n+1) capture buffer. The channel (n+1) capture buffer value is transferred to C(n+1)VH:L registers when the first byte of C(n)VH:L registers is read.

In the following figure, the read of C(n)VH returns the FTM counter high byte value when the event 1 occurred, and the read of C(n+1)VL returns the FTM counter low byte value when the event 1 occurred. The read of C(n+1)VL returns the FTM counter low byte value when the event 2 occurred, and the read of C(n+1)VH returns the FTM counter high byte value when the event 2 occurred.

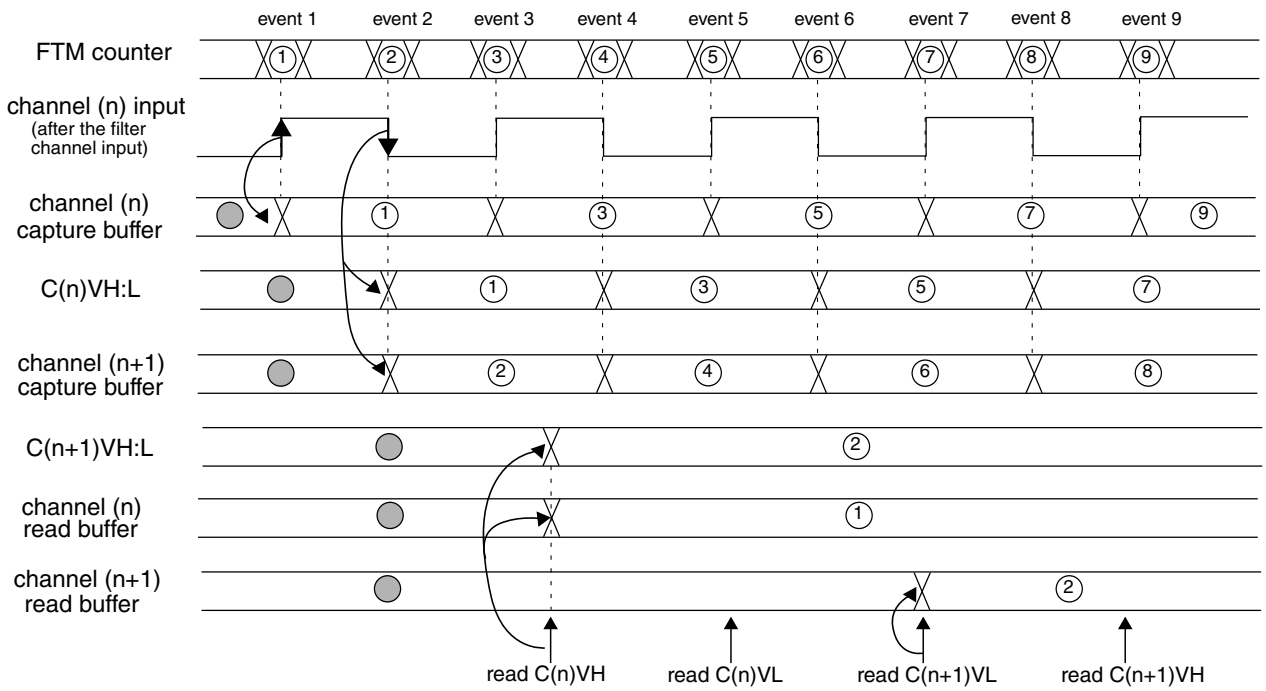


Figure 12-258. Dual edge capture mode read coherency mechanism

C(n)VH:L registers must be read prior to C(n+1)VH:L registers in dual edge capture one-shot and continuous modes for the read coherency mechanism works properly. Either the high or low bytes of C(n)VH:L and C(n+1)VH:L registers can be accessed first; however, the C(n)VH:L registers must be read prior to the C(n+1)VH:L registers in dual edge capture oneshot and continuous modes for the read coherency mechanism to work properly.

13.5 External signal description

The MTIM includes one external signal, TCLK, used to input an external clock when selected as the MTIM clock source. The signal properties of TCLK are shown in the following table.

Table 13-1. MTIM external signal

Signal	Function	I/O
TCLK	External clock source input into MTIM	I

The TCLK input must be synchronized by the bus clock. Also, variations in duty cycle and clock jitter must be accommodated. Therefore, the TCLK signal must be limited to one-fourth of the bus frequency.

The TCLK pin can be muxed with a general-purpose port pin.

13.6 Register definition

MTIM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
18	MTIM Status and Control Register (MTIM0_SC)	8	R/W	10h	13.6.1/400
19	MTIM Clock Configuration Register (MTIM0_CLK)	8	R/W	00h	13.6.2/401
1A	MTIM Counter Register (MTIM0_CNT)	8	R	00h	13.6.3/402
1B	MTIM Modulo Register (MTIM0_MOD)	8	R/W	00h	13.6.4/402
1C	MTIM Status and Control Register (MTIM1_SC)	8	R/W	10h	13.6.1/400
1D	MTIM Clock Configuration Register (MTIM1_CLK)	8	R/W	00h	13.6.2/401
1E	MTIM Counter Register (MTIM1_CNT)	8	R	00h	13.6.3/402
1F	MTIM Modulo Register (MTIM1_MOD)	8	R/W	00h	13.6.4/402

15.3.7 SCI Control Register 3 (SCIx_C3)

Address: Base address + 6h offset

Bit	7	6	5	4	3	2	1	0
Read	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_C3 field descriptions

Field	Description
7 R8	Ninth Data Bit for Receiver When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the msb of the buffered data in the SCI_D register. When reading 9-bit data, read R8 before reading SCI_D because reading SCI_D completes automatic flag clearing sequences that could allow R8 and SCI_D to be overwritten with new data.
6 T8	Ninth Data Bit for Transmitter When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the msb of the data in the SCI_D register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCI_D is written so T8 should be written, if it needs to change from its previous value, before SCI_D is written. If T8 does not need to change in the new value, such as when it is used to generate mark or space parity, it need not be written each time SCI_D is written.
5 TXDIR	TxD Pin Direction in Single-Wire Mode When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.
4 TXINV	Transmit Data Inversion Setting this bit reverses the polarity of the transmitted data output. **NOTE:** Setting TXINV inverts the TxD output for all cases: data bits, start and stop bits, break, and idle. 0 Transmit data not inverted. 1 Transmit data inverted.
3 ORIE	Overrun Interrupt Enable This bit enables the overrun flag (OR) to generate hardware interrupt requests. 0 OR interrupts disabled; use polling. 1 Hardware interrupt requested when OR is set.
2 NEIE	Noise Error Interrupt Enable This bit enables the noise flag (NF) to generate hardware interrupt requests. 0 NF interrupts disabled; use polling). 1 Hardware interrupt requested when NF is set.

Table continues on the next page...

((170 - 176) / 170) x 100 = 3.53%

For a 9-bit data and 2 stop bits character, data sampling of the stop bit takes the receiver 11 bit times x 16 RT cycles + 10 RT cycles = 186 RT cycles.

With the misaligned character shown in, the receiver counts 186 RT cycles at the point when the count of the transmitting device is 12 bit times x 16 RT cycles = 192 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit and 2 stop bits character with no errors is:

((186 - 192) / 186) x 100 = 3.23%

15.4.6 Additional SCI functions

The following sections describe additional SCI functions.

15.4.6.1 8- and 9-bit data modes

The SCI system, transmitter and receiver, can be configured to operate in 9-bit data mode by setting SCI_C1[M]. In 9-bit mode, there is a ninth data bit to the left of the most significant bit of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCI_C3. For the receiver, the ninth bit is held in SCI_C3[R8].

For coherent writes to the transmit data buffer, write to SCI_C3[T8] before writing to SCI_D.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to SCI_C3[T8] again. When data is transferred from the transmit data buffer to the transmit shifter, the value in SCI_C3[T8] is copied at the same time data is transferred from SCI_D to the shifter.

The 9-bit data mode is typically used with parity to allow eight bits of data plus the parity in the ninth bit, or it is used with address-mark wake-up so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

15.4.6.2 Stop mode operation

During all stop modes, clocks to the SCI module are halted.

No SCI module registers are affected in Stop3 mode.

16.3 Register Definition

The SPI has 8-bit registers to select SPI options, to control baud rate, to report SPI status, to hold an SPI data match value, and for transmit/receive data.

SPI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3098	SPI control register 1 (SPI0_C1)	8	R/W	04h	16.3.1/446
3099	SPI control register 2 (SPI0_C2)	8	R/W	00h	16.3.2/448
309A	SPI baud rate register (SPI0_BR)	8	R/W	00h	16.3.3/449
309B	SPI status register (SPI0_S)	8	R	20h	16.3.4/450
309D	SPI data register (SPI0_D)	8	R/W	00h	16.3.5/451
309F	SPI match register (SPI0_M)	8	R/W	00h	16.3.6/452

16.3.1 SPI control register 1 (SPIx_C1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.

Address: 3098h base + 0h offset = 3098h

Bit	7	6	5	4	3	2	1	0
Read Write	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

SPI0_C1 field descriptions

Field	Description
7 SPIE	SPI interrupt enable: for SPRF and MODF This bit enables the interrupt for SPI receive buffer full (SPRF) and mode fault (MODF) events. 0 Interrupts from SPRF and MODF are inhibited—use polling 1 Request a hardware interrupt when SPRF or MODF is 1
6 SPE	SPI system enable This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, the SPI is disabled and forced into an idle state, and all status bits in the S register are reset.

Table continues on the next page...

SPI1_C1 field descriptions (continued)

Field	Description
	When C2[MODFEN] is 1: In master mode, $\overline{SS}$ pin function is $\overline{SS}$ input for mode fault. In slave mode, $\overline{SS}$ pin function is slave select input. 1 When C2[MODFEN] is 0: In master mode, $\overline{SS}$ pin function is general-purpose I/O (not SPI). In slave mode, $\overline{SS}$ pin function is slave select input. When C2[MODFEN] is 1: In master mode, $\overline{SS}$ pin function is automatic $\overline{SS}$ output. In slave mode: $\overline{SS}$ pin function is slave select input.
0 LSBFE	LSB First (shifter direction) This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7 (or bit 15 in 16-bit mode). 0 SPI serial data transfers start with the most significant bit. 1 SPI serial data transfers start with the least significant bit.

17.3.2 SPI Control Register 2 (SPIx_C2)

This read/write register is used to control optional features of the SPI system.

Address: 30A0h base + 1h offset = 30A1h

Bit	7	6	5	4	3	2	1	0
Read Write	SPMIE	SPIMODE	Reserved	MODFEN	BIDIROE	Reserved	SPISWAI	SPC0
Reset	0	0	0	0	0	0	0	0

SPI1_C2 field descriptions

Field	Description
7 SPMIE	SPI Match Interrupt Enable This is the interrupt enable bit for the SPI receive data buffer hardware match (SPMF) function. 0 Interrupts from SPMF inhibited (use polling) 1 When SPMF is 1, requests a hardware interrupt
6 SPIMODE	SPI 8-bit or 16-bit mode This bit allows the user to select either an 8-bit or 16-bit SPI data transmission length. In master mode, a change of this bit aborts a transmission in progress, forces the SPI system into an idle state, and resets all status bits in the S register. Refer to the description of “Data Transmission Length” for details. 0 8-bit SPI shift register, match register, and buffers 1 16-bit SPI shift register, match register, and buffers
5 Reserved	This field is reserved. Do not write to this reserved bit.
4 MODFEN	Master Mode-Fault Function Enable

Table continues on the next page...

22.5.1 CRC Data 0 Register (CRC_D0)

D0 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 0h offset = 3060h

Bit	7	6	5	4	3	2	1	0
Read Write	DH0							
Reset	1	1	1	1	1	1	1	1

CRC_D0 field descriptions

Field	Description
DH0	CRC Data Bit 31:24

22.5.2 CRC Data 1 Register (CRC_D1)

D1 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 1h offset = 3061h

Bit	7	6	5	4	3	2	1	0
Read Write	D1							
Reset	1	1	1	1	1	1	1	1

- Provides robust check that program flow is faster than expected
- Early refresh attempts trigger a reset.

- Optional timeout interrupt to allow post-processing diagnostics
  - Interrupt request to CPU with interrupt vector for an interrupt service routine (ISR)
  - Forced reset occurs 128 bus clocks after the interrupt vector fetch.
- Configuration bits are write-once-after-reset to ensure watchdog configuration cannot be mistakenly altered.
- Robust write sequence for unlocking write-once configuration bits
  - Unlock sequence of writing 0xC520 and then 0xD928 within 16 bus clocks for allowing updates to write-once configuration bits
  - Software must make updates within 128 bus clocks after unlocking and before WDOG closing unlock window.

23.1.2 Block diagram

The following figure provides a block diagram of the WDOG module.

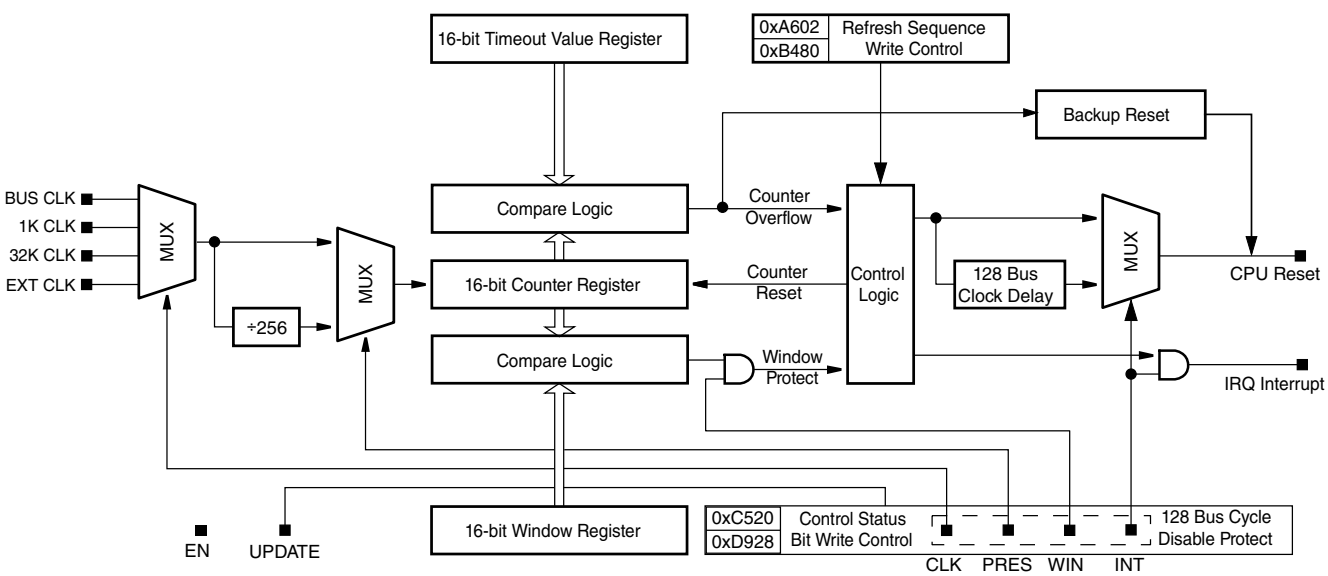


Figure 23-1. WDOG block diagram

DBG_CBL field descriptions

Field	Description
CB[7:0]	Comparator B Low The Comparator B Low compare bits control whether Comparator B will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

25.3.5 Debug Comparator C High Register (DBG_CCH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 4h offset = 3014h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CCH field descriptions

Field	Description
CC[15:8]	Comparator C High Compare Bits The Comparator C High compare bits control whether Comparator C will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.