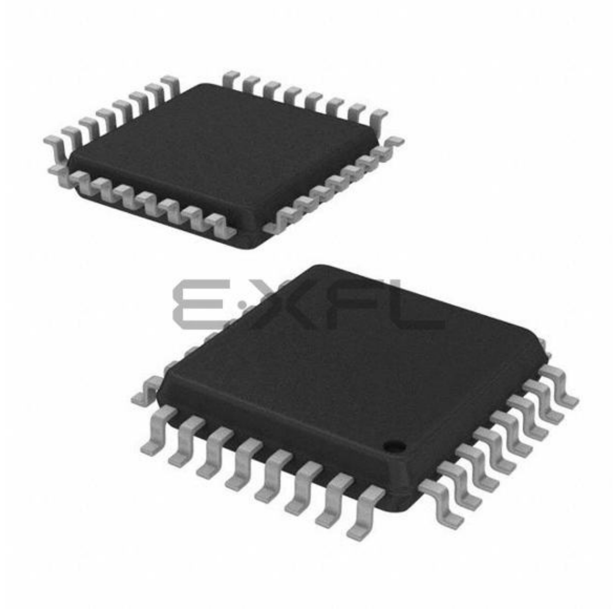
NXP USA Inc. - MC9S08PT60VLC Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pt60vlc

NVM_FERCNFG field descriptions

Field	Description
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 DFDIE	Double Bit Fault Detect Interrupt Enable The DFDIE bit controls interrupt generation when a double bit fault is detected during a flash block read operation. 0 DFDIF interrupt disabled. 1 An interrupt will be requested whenever the DFDIF flag is set.
0 SFDIE	Single Bit Fault Detect Interrupt Enable The SFDIE bit controls interrupt generation when a single bit fault is detected during a flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set. 1 An interrupt will be requested whenever the SFDIF flag is set.

4.6.6 Flash Status Register (NVM_FSTAT)

The FSTAT register reports the operational status of the flash and EEPROM module.

Address: 3020h base + 6h offset = 3026h

Bit	7	6	5	4	3	2	1	0
Read	CCIF	0	ACCERR	FPVIOL	MGBUSY	0	MGSTAT	
Write		▨			▨	▨	▨	
Reset	1	0	0	0	0	0	0	0

NVM_FSTAT field descriptions

Field	Description
7 CCIF	Command Complete Interrupt Flag The CCIF flag indicates that a flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress. 1 Flash command has completed.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 ACCERR	Flash Access Error Flag The ACCERR bit indicates an illegal access has occurred to the flash memory caused by either a violation of the command write sequence or issuing an illegal flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR.

Table continues on the next page...

IPC_SC field descriptions (continued)

Field	Description
	IPMPS register. Writing IPM with PULIPM setting when IPCE is already set, the IPM will restore the value pulled from the IPMPS register, not the value written to the IPM register.

5.4.2 Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS)

This register is used to store the previous interrupt priority mask level temporarily when the currently active interrupt is executed.

Address: 3Eh base + 1h offset = 3Fh

Bit	7	6	5	4	3	2	1	0
Read	IPM3		IPM2		IPM1		IPM0	
Write	▨		▨		▨		▨	
Reset	0	0	0	0	0	0	0	0

IPC_IPMPS field descriptions

Field	Description
7–6 IPM3	Interrupt Priority Mask pseudo stack position 3 This field is the pseudo stack register for IPM3. The most recent information is stored in IPM3.
5–4 IPM2	Interrupt Priority Mask pseudo stack position 2 This field is the pseudo stack register for IPM2. The most recent information is stored in IPM2.
3–2 IPM1	Interrupt Priority Mask pseudo stack position 1 This field is the pseudo stack register for IPM1. The most recent information is stored in IPM1.
IPM0	Interrupt Priority Mask pseudo stack position 0 This field is the pseudo stack register for IPM0. The most recent information is stored in IPM0.

5.4.3 Interrupt Level Setting Registers n (IPC_ILRS*n*)

This set of registers (ILRS0-ILRS9) contains the user specified interrupt level for each interrupt source, and indicates the number of the register (ILRSn is ILRS0 through ILRS9).

Address: 3Eh base + 3012h offset + (1d × i), where i=0d to 9d

Bit	7	6	5	4	3	2	1	0
Read Write	ILRn3		ILRn2		ILRn1		ILRn0	
Reset	0	0	0	0	0	0	0	0

Chapter 7
Parallel input/output

7.1 Introduction

This device has eight sets of I/O ports, which include up to 57 general-purpose I/O pins.

Not all pins are available on all devices. See Table 2-1 to determine which functions are available for a specific device.

Many of the I/O pins are shared with on-chip peripheral functions, as shown in Table 2-1. The peripheral modules have priority over the I/O, so when a peripheral is enabled, the associated I/O functions are disabled.

After reset, the shared peripheral functions are disabled so that the pins are controlled by the parallel I/O except PTA4 and PTA5 that are default to BKGD/MS and $\overline{\text{RESET}}$ function. All of the parallel I/O are configured as high-impedance (Hi-Z). The pin control functions for each pin are configured as follows:

- input disabled (PTxIEn = 0),
- output disabled (PTxOEn = 0), and
- internal pullups disabled (PTxPEn = 0).

Additionally, the parallel I/O that support high drive capability are disabled (HDRVE = 0x00) after reset.

The following three figures show the structures of each I/O pin.

PORT_PTBOE field descriptions (continued)

Field	Description
	0 Output Disabled for port B bit 5. 1 Output Enabled for port B bit 5.
4 PTBOE4	Output Enable for Port B Bit 4 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 4. 1 Output Enabled for port B bit 4.
3 PTBOE3	Output Enable for Port B Bit 3 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 3. 1 Output Enabled for port B bit 3.
2 PTBOE2	Output Enable for Port B Bit 2 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 2. 1 Output Enabled for port B bit 2.
1 PTBOE1	Output Enable for Port B Bit 1 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 1. 1 Output Enabled for port B bit 1.
0 PTBOE0	Output Enable for Port B Bit 0 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 0. 1 Output Enabled for port B bit 0.

7.7.12 Port C Output Enable Register (PORT_PTCOE)

Address: 0h base + 30B2h offset = 30B2h

Bit	7	6	5	4	3	2	1	0
Read Write	PTCOE7	PTCOE6	PTCOE5	PTCOE4	PTCOE3	PTCOE2	PTCOE1	PTCOE0
Reset	0	0	0	0	0	0	0	0

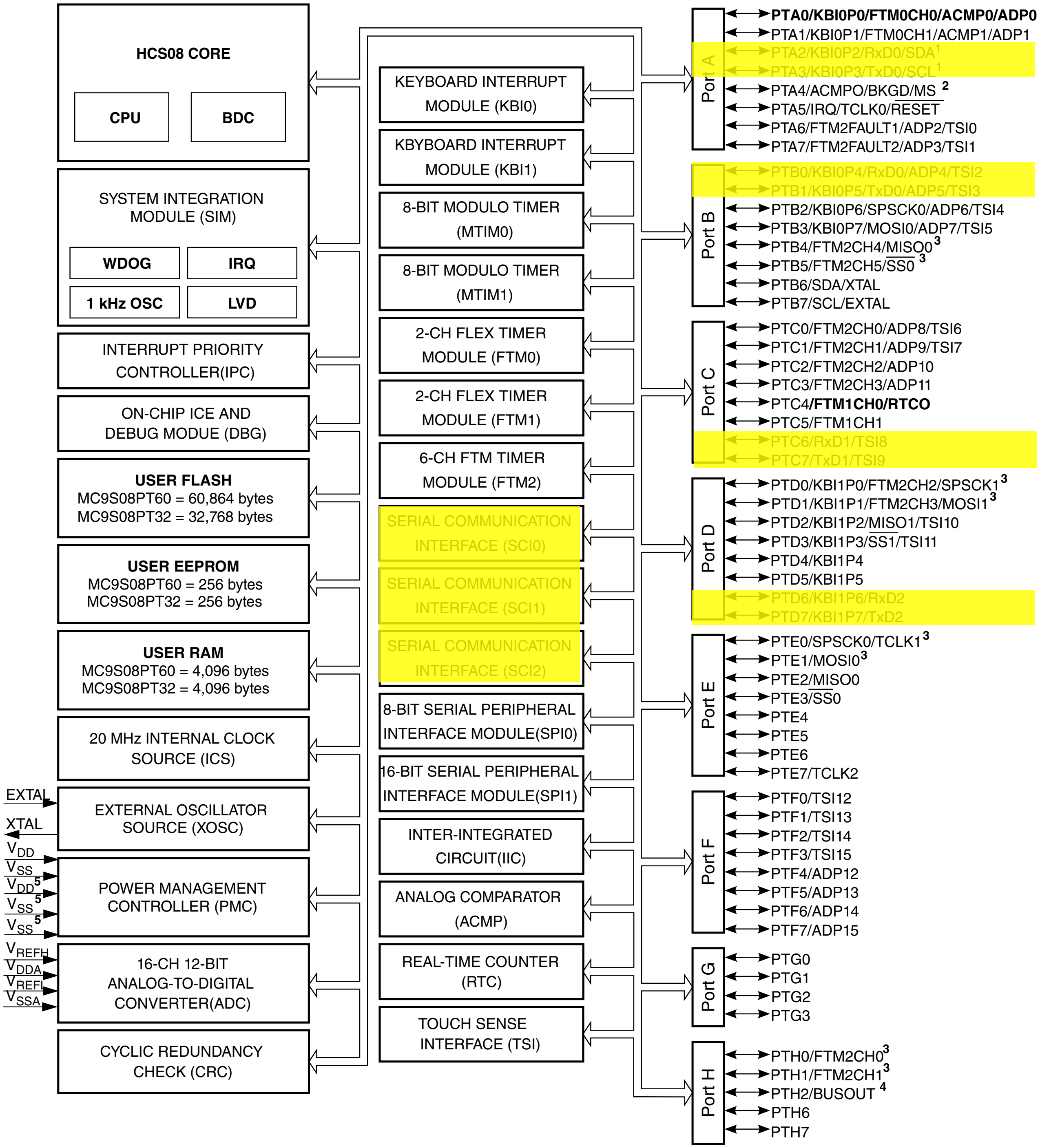
PORT_PTCOE field descriptions

Field	Description
7 PTCOE7	Output Enable for Port C Bit 7 This read/write bit enables the port C pin as an output.

Table continues on the next page...

PORT_PTCIE field descriptions

Field	Description
7 PTCIE7	Input Enable for Port C Bit 7 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 7. 1 Input enabled for port C bit 7.
6 PTCIE6	Input Enable for Port C Bit 6 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 6. 1 Input enabled for port C bit 6.
5 PTCIE5	Input Enable for Port C Bit 5 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 5. 1 Input enabled for port C bit 5.
4 PTCIE4	Input Enable for Port C Bit 4 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 4. 1 Input enabled for port C bit 4.
3 PTCIE3	Input Enable for Port C Bit 3 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 3. 1 Input enabled for port C bit 3.
2 PTCIE2	Input Enable for Port C Bit 2 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 2. 1 Input enabled for port C bit 2.
1 PTCIE1	Input Enable for Port C Bit 1 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 1. 1 Input enabled for port C bit 1.
0 PTCIE0	Input Enable for Port C Bit 0 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 0. 1 Input enabled for port C bit 0.


HCS08 CORE
CPU
BDC
SYSTEM INTEGRATION MODULE (SIM)
WDOG
IRQ
1 kHz OSC
LVD
INTERRUPT PRIORITY CONTROLLER(IPC)
ON-CHIP ICE AND DEBUG MODUE (DBG)
USER FLASH
MC9S08PT60 = 60,864 bytes
MC9S08PT32 = 32,768 bytes
USER EEPROM
MC9S08PT60 = 256 bytes
MC9S08PT32 = 256 bytes
USER RAM
MC9S08PT60 = 4,096 bytes
MC9S08PT32 = 4,096 bytes
20 MHz INTERNAL CLOCK SOURCE (ICS)
EXTAL
XTAL
EXTERNAL OSCILLATOR SOURCE (XOSC)
VDD
VSS
VDD[5]
VSS[5]
VSS[5]
POWER MANAGEMENT CONTROLLER (PMC)
VREFH
VDDA
VREFL
VSSA
16-CH 12-BIT ANALOG-TO-DIGITAL CONVERTER(ADC)
CYCLIC REDUNDANCY CHECK (CRC)
KEYBOARD INTERRUPT MODULE (KBI0)
KBYBOARD INTERRUPT MODULE (KBI1)
8-BIT MODULO TIMER (MTIM0)
8-BIT MODULO TIMER (MTIM1)
2-CH FLEX TIMER MODULE (FTM0)
2-CH FLEX TIMER MODULE (FTM1)
6-CH FTM TIMER MODULE (FTM2)
SERIAL COMMUNICATION INTERFACE (SCI0)
SERIAL COMMUNICATION INTERFACE (SCI1)
SERIAL COMMUNICATION INTERFACE (SCI2)
8-BIT SERIAL PERIPHERAL INTERFACE MODULE(SPI0)
16-BIT SERIAL PERIPHERAL INTERFACE MODULE(SPI1)
INTER-INTEGRATED CIRCUIT(IIC)
ANALOG COMPARATOR (ACMP)
REAL-TIME COUNTER (RTC)
TOUCH SENSE INTERFACE (TSI)
Port A
PTA0/KBI0P0/FTM0CH0/ACMP0/ADP0
PTA1/KBI0P1/FTM0CH1/ACMP1/ADP1
PTA2/KBI0P2/RxD0/SDA[1]
PTA3/KBI0P3/TxD0/SCL[1]
PTA4/ACMPO/BKGD/MS [2]
PTA5/IRQ/TCLK0/RESET
PTA6/FTM2FAULT1/ADP2/TSI0
PTA7/FTM2FAULT2/ADP3/TSI1
Port B
PTB0/KBI0P4/RxD0/ADP4/TSI2
PTB1/KBI0P5/TxD0/ADP5/TSI3
PTB2/KBI0P6/SPSCK0/ADP6/TSI4
PTB3/KBI0P7/MOSI0/ADP7/TSI5
PTB4/FTM2CH4/MISO0[3]
PTB5/FTM2CH5/SS0 [3]
PTB6/SDA/XTAL
PTB7/SCL/EXTAL
Port C
PTC0/FTM2CH0/ADP8/TSI6
PTC1/FTM2CH1/ADP9/TSI7
PTC2/FTM2CH2/ADP10
PTC3/FTM2CH3/ADP11
PTC4/FTM1CH0/RTCO
PTC5/FTM1CH1
PTC6/RxD1/TSI8
PTC7/TxD1/TSI9
Port D
PTD0/KBI1P0/FTM2CH2/SPSCK1[3]
PTD1/KBI1P1/FTM2CH3/MOSI1[3]
PTD2/KBI1P2/MISO1/TSI10
PTD3/KBI1P3/SS1/TSI11
PTD4/KBI1P4
PTD5/KBI1P5
PTD6/KBI1P6/RxD2
PTD7/KBI1P7/TxD2
Port E
PTE0/SPSCK0/TCLK1[3]
PTE1/MOSI0[3]
PTE2/MISO0
PTE3/SS0
PTE4
PTE5
PTE6
PTE7/TCLK2
Port F
PTF0/TSI12
PTF1/TSI13
PTF2/TSI14
PTF3/TSI15
PTF4/ADP12
PTF5/ADP13
PTF6/ADP14
PTF7/ADP15
Port G
PTG0
PTG1
PTG2
PTG3
Port H
PTH0/FTM2CH0[3]
PTH1/FTM2CH1[3]
PTH2/BUSOUT [4]
PTH6
PTH7

1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 can provide ultra-high source/sink current up to 20 mA.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-6. Device block diagram highlighting SCI modules and pins

10.5 HCS08 V6 Opcodes

The HCS08 V6 Core has 254 one-byte opcodes and 47 two-byte opcodes, totaling 301 opcodes. For a more detailed description of the HCS08 V6 instructions please refer to the Instruction Set Summary section.

10.6 Special Operations

The CPU performs a few special operations that are similar to instructions but do not have opcodes like other CPU instructions. This section provides additional information about these operations.

10.6.1 Reset Sequence

Reset can be caused by a power-on-reset (POR) event, internal conditions such as the COP (computer operating properly) watchdog, or by assertion of an external active-low reset pin. When a reset event occurs, the CPU immediately stops whatever it is doing (the MCU does not wait for an instruction boundary before responding to a reset event).

The reset event is considered concluded when the sequence to determine whether the reset came from an internal source is done and when the reset pin is no longer asserted. At the conclusion of a reset event, the CPU performs a 6-cycle sequence to fetch the reset vector from $FFFE and $FFFF and to fill the instruction queue in preparation for execution of the first program instruction.

10.6.2 Interrupt Sequence

When an interrupt is requested, the CPU completes the current instruction before responding to the interrupt. At this point, the program counter is pointing at the start of the next instruction, which is where the CPU should return after servicing the interrupt. The CPU responds to an interrupt by performing the same sequence of operations as for a software interrupt (SWI) instruction, except the address used for the vector fetch is determined by the highest priority interrupt that is pending when the interrupt sequence started.

The CPU sequence for an interrupt is:

FTMx_C*n*VH field descriptions

Field	Description
VAL_H	Channel Value High Byte Captured FTM counter value of the input capture function or the match value for the output modes

12.3.10 Channel Value Low (FTMx_C*n*VL)

See the description for the Channel Value High register.

Address: Base address + 7h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read Write	VAL_L							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*VL field descriptions

Field	Description
VAL_L	Channel Value Low Byte Captured FTM counter value of the input capture function or the match value for the output modes

12.3.11 Counter Initial Value High (FTMx_CNTINH)

The Counter Initial Value registers contain the high and low bytes of the initial value for the FTM counter.

Writing to either byte latches the value into a buffer. The registers are updated with the value of their write buffer.

When BDM is active, the write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the counter initial value register are written while BDM is active. Any write to the counter initial value registers bypasses the buffer latches and writes directly to the counter initial value register while BDM is active.

The first time that the FTM clock is selected (first write to change the CLKS bits to a non-zero value), FTM counter starts with the value 0x0000. To avoid this behavior, before the first write to select the FTM clock, write the new value to the Counter Initial Value registers and then initialize the FTM counter by writing any value to CNT).

FTMx_COMBINEn field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 FAULTEN	Fault Control Enable Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
5 SYNCEN	Synchronization Enable Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
4 DTEN	Deadtime Enable Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
3 DECAP	Dual Edge Capture Mode Captures Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when MODE[FTMEN] = 1 and DECAPEN = 1. DECAP bit is cleared automatically by hardware if dual edge capture one-shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.
2 DECAPEN	Dual Edge Capture Mode Enable Enables the dual edge capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA, and ELS(n+1)B:ELS(n+1)A bits in dual edge capture mode according to the table Mode, Edge, and Level Selection in the description of the CnSC register. This field applies only when MODE[FTMEN] = 1. DECAPEN is write protected, this bit can be written only if MODE[WPDIS] = 1. 0 The dual edge capture mode in this pair of channels is disabled. 1 The dual edge capture mode in this pair of channels is enabled.
1 COMP	Complement of Channel (n) Enables complementary mode for the combined channels. In complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.

Table continues on the next page...

12.3.22 Fault Mode Status (FTMx_FMS)

This register contains the fault detection flags, write protection enable bit, and the logic OR of the enable fault inputs.

Address: Base address + 25h offset

Bit	7	6	5	4	3	2	1	0
Read	FAULTF	WPEN	FAULTIN	0	FAULTF3	FAULTF2	FAULTF1	FAULTF0
Write	0				0	0	0	0
Reset	0	0	0	0	0	0	0	0

FTMx_FMS field descriptions

Field	Description
7 FAULTF	Fault Detection Flag Represents the logic OR of the individual FAULTFn bits. Clear FAULTF by reading the FMS register while FAULTF is set and then writing a 0 to FAULTF while there is no existing fault condition at the enabled fault inputs. Writing a 1 to FAULTF has no effect. If another fault condition is detected in an enabled fault input before the clearing sequence is completed, the sequence is reset so FAULTF remains set after the clearing sequence is completed for the earlier fault condition. FAULTF is also cleared when FAULTFn bits are cleared individually. 0 No fault condition was detected. 1 A fault condition was detected.
6 WPEN	Write Protection Enable The WPEN bit is the negation of the WPDIS bit. WPEN is set when 1 is written to it. WPEN is cleared when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPEN has no effect. 0 Write protection is disabled. Write protected bits can be written. 1 Write protection is enabled. Write protected bits cannot be written.
5 FAULTIN	Fault Inputs Represents the logic OR of the enabled fault input after its filter, if its filter is enabled, when fault control is enabled. 0 The value of the fault input is 0. 1 The value of the fault input is 1.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FAULTF3	Fault Detection Flag 3 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected in the fault input. Clear FAULTF by reading the FMS register while FAULTFn is set and then writing a 0 to FAULTFn FAULTF while there is no existing fault condition at the fault input n. Writing a 1 to FAULTFn has no effect. FAULTFn bit is also cleared when FAULTF bit is cleared.

Table continues on the next page...

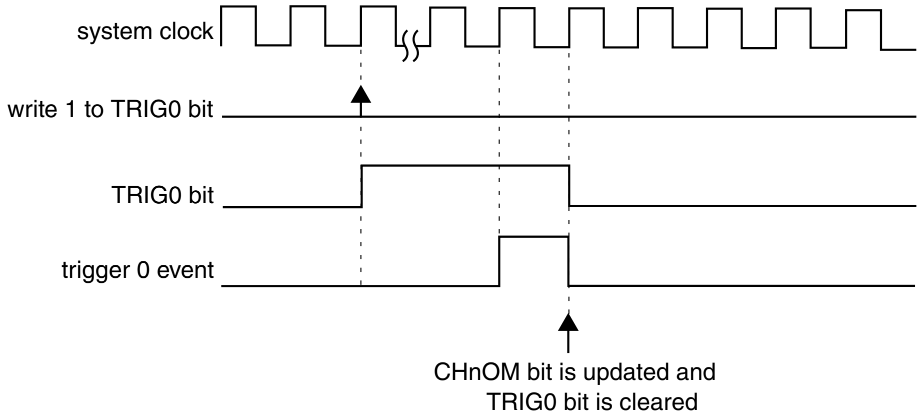


Figure 12-232. CHnOM synchronization when (SYNCHOM = 1), (PWMSYNC = 0), and a hardware trigger was used

- If SYNCHOM = 1 and PWMSYNC = 1, then this synchronization is made on the next enabled hardware trigger event. The trigger enable bit (TRIGn) is cleared when the enabled hardware trigger n event is detected. See the following figure.

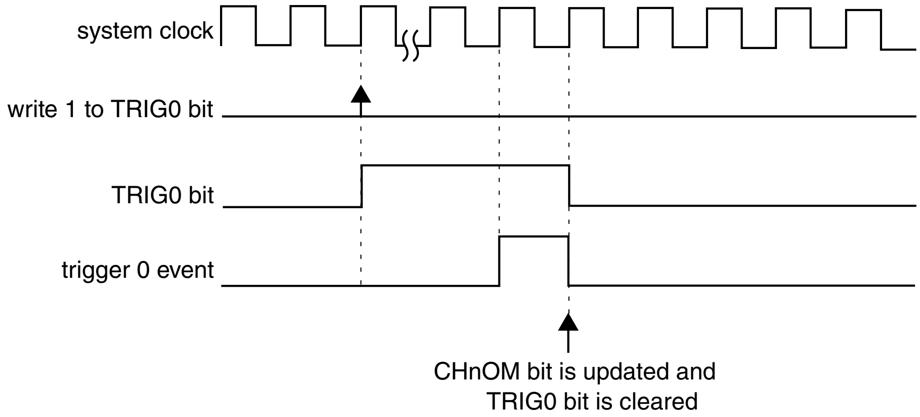


Figure 12-233. CHnOM Synchronization when (SYNCHOM = 1), (PWMSYNC = 1), and a hardware trigger was used

12.4.11.7 FTM counter synchronization

The FTM counter synchronization occurs when the FTM counter is updated with the value of the CNTINH:L registers and the channel outputs are forced to their initial value as defined by the channel configuration.

- If REINIT = 0, then this synchronization is made when the FTM counter changes from MODH:L to CNTINH:L.
- If REINIT = 1 and PWMSYNC = 0, then this synchronization is made on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared. See the following figure.

12.4.11.8 Summary of PWM synchronization

The following table shows the summary of PWM synchronization.

Table 12-246. Summary of PWM synchronization

Register or bit	PWMSYNC	REINIT	SYNCHOM	CNTMAX	CNTMIN	SYNCEN	Description
CNTINH:L	X	X	X	X	X	X	Changes take effect after the second byte is written. Effect is seen after the next TOF or PWM synchronization.
MODH:L	0	0	X	1	0	X	MODH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled hardware or software trigger has occurred.
	0	0	X	0	1	X	MODH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled hardware or software trigger has occurred.
	0	1	X	X	X	X	MODH:L are updated with their write buffer contents when the enabled hardware or software trigger occurs.
	1	X	X	1	0	X	MODH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled software trigger has occurred.
	1	X	X	0	1	X	MODH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled software trigger has occurred.
CnVH:L	0	0	X	1	0	1	CnVH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled hardware or software trigger has occurred.
	0	0	X	0	1	1	CnVH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled hardware or software trigger has occurred.
	0	1	X	X	X	1	CnVH:L are updated with their write buffer contents when the enabled hardware or software trigger occurs.

Table continues on the next page...

When a rising edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n) capture buffer. The channel (n) capture buffer value is transferred to C(n)VH:L registers when a falling edge occurs in the channel (n) input signal. C(n)VH:L registers have the FTM counter value when the previous rising edge occurred, and the channel (n) capture buffer has the FTM counter value when the last rising edge occurred.

When a negative edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n+1) capture buffer. The channel (n+1) capture buffer value is transferred to C(n+1)VH:L registers when the first byte of C(n)VH:L registers is read.

In the following figure, the read of C(n)VH returns the FTM counter high byte value when the event 1 occurred, and the read of C(n+1)VL returns the FTM counter low byte value when the event 1 occurred. The read of C(n+1)VL returns the FTM counter low byte value when the event 2 occurred, and the read of C(n+1)VH returns the FTM counter high byte value when the event 2 occurred.

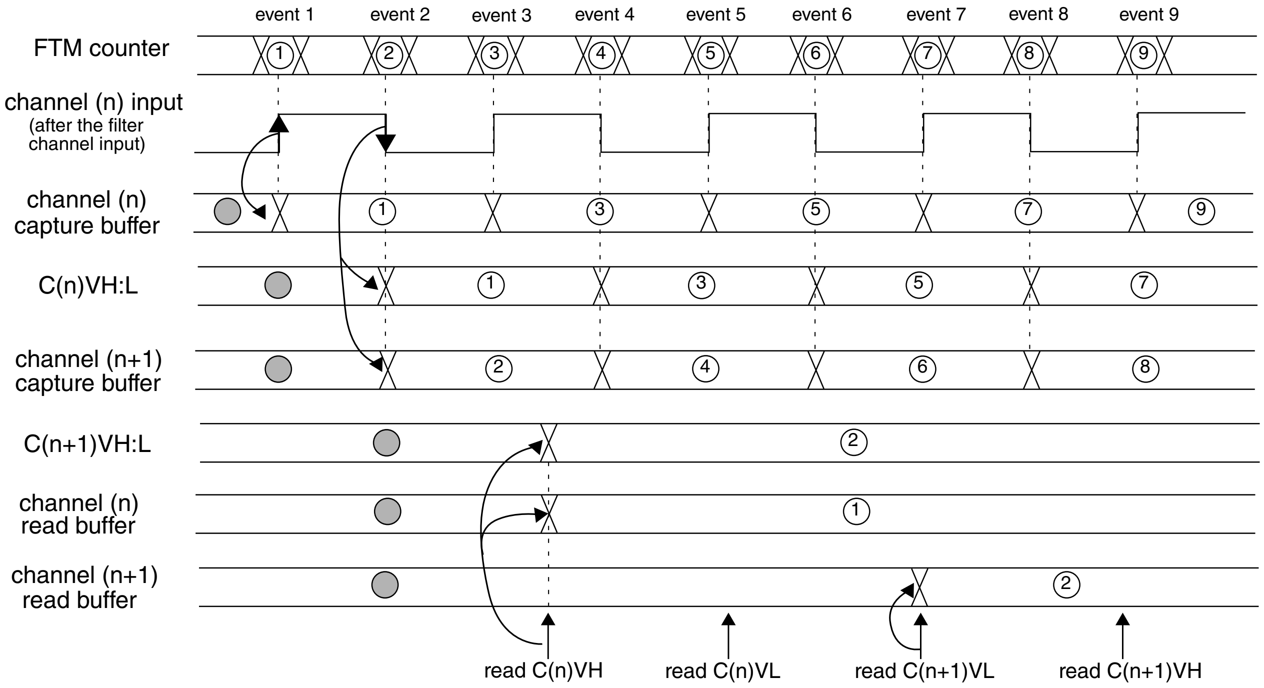


Figure 12-258. Dual edge capture mode read coherency mechanism

C(n)VH:L registers must be read prior to C(n+1)VH:L registers in dual edge capture one-shot and continuous modes for the read coherency mechanism works properly. Either the high or low bytes of C(n)VH:L and C(n+1)VH:L registers can be accessed first; however, the C(n)VH:L registers must be read prior to the C(n+1)VH:L registers in dual edge capture oneshot and continuous modes for the read coherency mechanism to work properly.

15.2 SCI signal descriptions

The SCI signals are shown in the table found here.

Table 15-1. SCI signal descriptions

Signal	Description	I/O
RxD	Receive data	I
TxD	Transmit data	I/O

15.2.1 Detailed signal descriptions

The detailed signal descriptions of the SCI are shown in the following table.

Table 15-2. SCI—Detailed signal descriptions

Signal	I/O	Description	
RxD	I	Receive data. Serial data input to receiver.	
		State meaning	Whether RxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Sampled at a frequency determined by the module clock divided by the baud rate.
TxD	I/O	Transmit data. Serial data output from transmitter.	
		State meaning	Whether TxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Driven at the beginning or within a bit time according to the bit encoding method along with other configuration settings. Otherwise, transmissions are independent of reception timing.

15.3 Register definition

The SCI has 8-bit registers to control baud rate, select SCI options, report SCI status, and for transmit/receive data.

Refer to the direct-page register summary in the memory chapter of this document or the absolute address assignments for all SCI registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

- Bus busy detection
- General call recognition
- 10-bit address extension
- Support for *System Management Bus (SMBus) Specification, version 2*
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support

18.1.2 Modes of operation

The I2C module's operation in various low power modes is as follows:

- Run mode: This is the basic mode of operation. To conserve power in this mode, disable the module.
- Wait mode: The module continues to operate when the core is in Wait mode and can provide a wakeup interrupt.
- Stop mode: The module is inactive in Stop3 mode for reduced power consumption, except that address matching is enabled in Stop3 mode. The STOP instruction does not affect the I2C module's register states.

18.1.3 Block diagram

The following figure is a functional block diagram of the I2C module.

19.3.2 Status and Control Register 2 (ADC_SC2)

The ADC_SC2 register controls the compare function, conversion trigger, and conversion active of the ADC module.

Address: 10h base + 1h offset = 11h

Bit	7	6	5	4	3	2	1	0
Read	ADACT	ADTRG	ACFE	ACFGT	FEMPTY	FFULL		
Write							0	
Reset	0	0	0	0	1	0	0	0

ADC_SC2 field descriptions

Field	Description
7 ADACT	Conversion Active Indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress. 1 Conversion in progress.
6 ADTRG	Conversion Trigger Select Selects the type of trigger used for initiating a conversion. Two types of trigger are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADC_SC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input. 0 Software trigger selected. 1 Hardware trigger selected.
5 ACFE	Compare Function Enable Enables the compare function. 0 Compare function disabled. 1 Compare function enabled.
4 ACFGT	Compare Function Greater Than Enable Configures the compare function to trigger when the result of the conversion of the input being monitored is greater than or equal to the compare value. The compare function defaults to triggering when the result of the compare of the input being monitored is less than the compare value. 0 Compare triggers when input is less than compare level. 1 Compare triggers when input is greater than or equal to compare level.
3 FEMPTY	Result FIFO empty 0 Indicates that ADC result FIFO have at least one valid new data. 1 Indicates that ADC result FIFO have no valid new data.
2 FFULL	Result FIFO full

Table continues on the next page...

19.6.2.4 Code width and quantization error

The ADC quantizes the ideal straight-line transfer function into 4096 steps (in 12-bit mode). Each step ideally has the same height (1 code) and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N bit converter (in this case N can be 8, 10 or 12), defined as 1LSB, is:

$$1\,\mathrm{lsb} = (V_{\mathrm{REFH}} - V_{\mathrm{REFL}}) \,/\, 2^N$$

There is an inherent quantization error due to the digitization of the result. For 8-bit or 10-bit conversions the code transitions when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2 lsb in 8- or 10-bit mode. As a consequence, however, the code width of the first (0x000) conversion is only 1/2 lsb and the code width of the last (0xFF or 0x3FF) is 1.5 lsb.

For 12-bit conversions the code transitions only after the full code width is present, so the quantization error is -1 lsb to 0 lsb and the code width of each step is 1 lsb.

19.6.2.5 Linearity errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system must be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error (E_{ZS}) (sometimes called offset) — This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2 lsb in 8-bit or 10-bit modes and 1 lsb in 12-bit mode). If the first conversion is 0x001, the difference between the actual 0x001 code width and its ideal (1 lsb) is used.
- Full-scale error (E_{FS}) — This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5 lsb in 8-bit or 10-bit modes and 1LSB in 12-bit mode). If the last conversion is 0x3FE, the difference between the actual 0x3FE code width and its ideal (1 lsb) is used.
- Differential non-linearity (DNL) — This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.

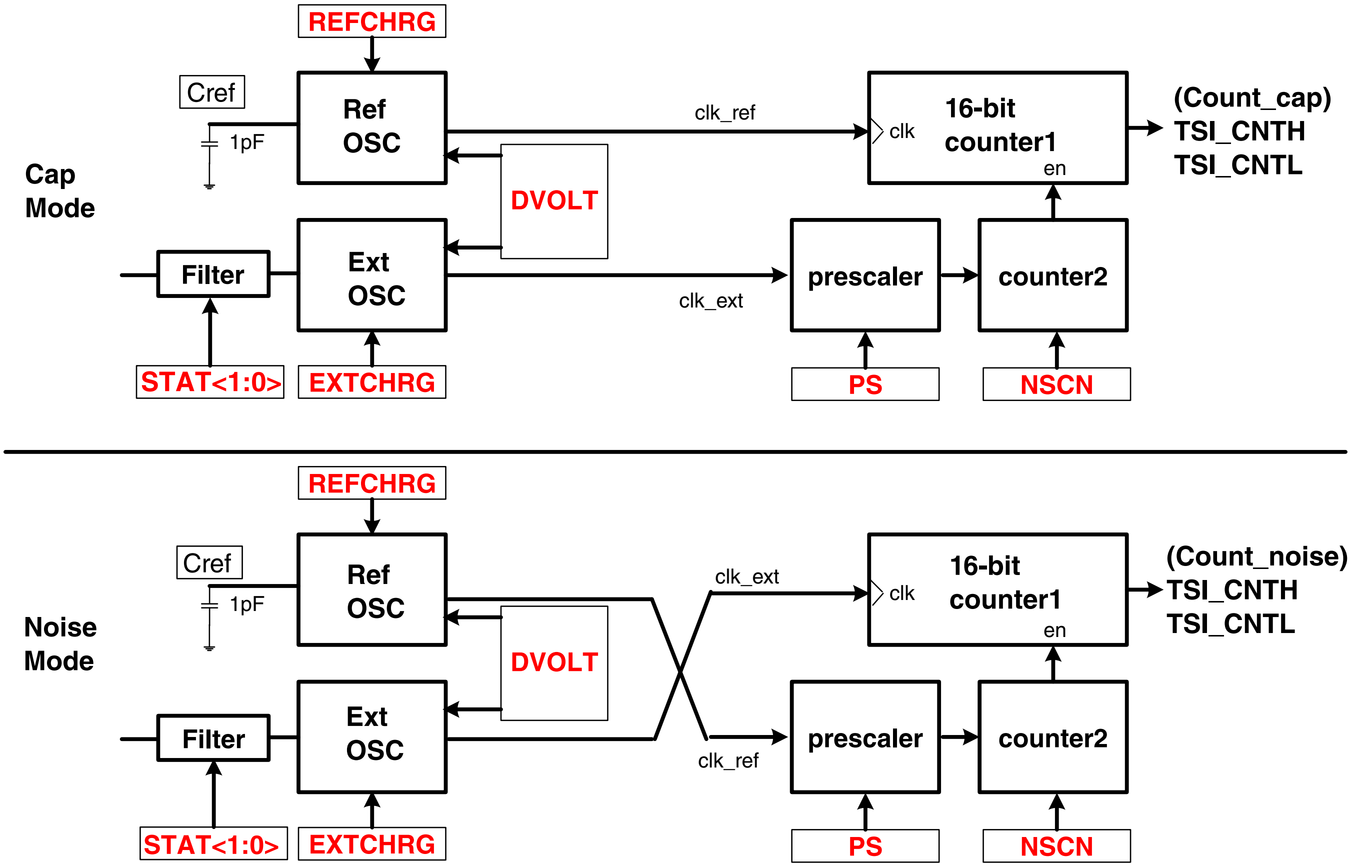


Figure 21-13. TSI noise detection mode block diagram

25.3.6 Debug Comparator C Low Register (DBG_CCL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 5h offset = 3015h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[7:0]							
Reset	0	0	0	0	0	0	0	0

DBG_CCL field descriptions

Field	Description
CC[7:0]	Comparator C Low The Comparator C Low compare bits control whether Comparator C will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

25.3.7 Debug FIFO High Register (DBG_FH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 6h offset = 3016h

Bit	7	6	5	4	3	2	1	0
Read	F[15:8]							
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FH field descriptions

Field	Description
F[15:8]	FIFO High Data Bits The FIFO High data bits provide access to bits [15:8] of data in the FIFO. This register is not used in event only modes and will read a $00 for valid FIFO words.

25.3.8 Debug FIFO Low Register (DBG_FL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 7h offset = 3017h

Bit	7	6	5	4	3	2	1	0
Read	F[7:0]							
Write	▨							
Reset	0	0	0	0	0	0	0	0

DBG_FL field descriptions

Field	Description
F[7:0]	FIFO Low Data Bits The FIFO Low data bits contain the least significant byte of data in the FIFO. When reading FIFO words, read DBGFX and DBGFH before reading DBGFL because reading DBGFL causes the FIFO pointers to advance to the next FIFO location. In event-only modes, there is no useful information in DBGFX and DBGFH so it is not necessary to read them before reading DBGFL.