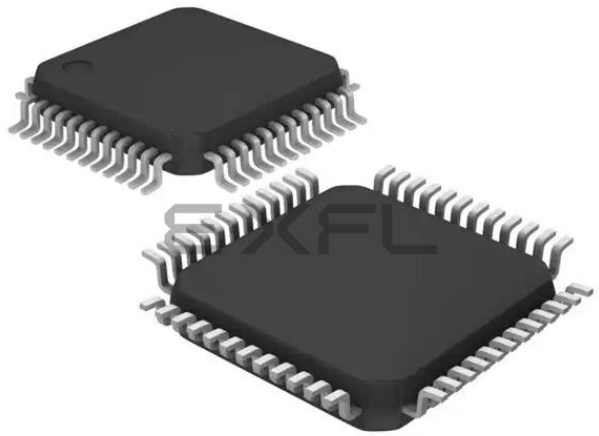

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Details	
Product Status	Active
Core Processor	8051/52
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e227alg

PIN DESCRIPTION, continued

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
P1.0–P1.7	I/O S H	High	**PORT 1**: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P1.0, ADC0, T2 P1.1, ADC1, BRAKE P1.2, ADC2, RXD1 P1.3, ADC3, TXD1 P1.4, ADC4 P1.5, ADC5 P1.6, ADC6 P1.7, ADC7
P2.0-P2.5	I/O S	Tri-state	**PORT 2**: 8-bit, bi-directional I/O port. This port also provides the upper address bits for accesses to external memory. P2.6 to P2.7 can be software configured as I2C serial ports. P2.0 to P2.5 also provides PWM0 to PWM5 outputs. P2.0, A8, PWM0 P2.1, A9, PWM1 P2.2, A10, PWM2 P2.3, A11, PWM3 P2.4, A12, PWM4 P2.5, A13, PWM5 P2.6, A14, SCL P2.7, A15, SDA **Note:** P2.6 and P2.7 are permanent open drain pins. When access to external memory beyond 16K region, user requires to add external pull-up registers (up to 2Kohm) on these pins. This will result in slight increase in current consumption.
P2.6-P2.7	I/O D S	High-Z	
P3.0-P3.7	I/O S H	High	**PORT 3**: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P3.0, RXD P3.1, TXD P3.2, /INT0 P3.3, /INT1 P3.4, T0, IC0, QEA P3.5, T1, IC1, QEB P3.6, /WR P3.7, /RD

7. SPECIAL FUNCTION REGISTERS

The W79E22X SERIES uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E22X SERIES contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses.

F8	EIP	EIE1	EIP1	CCL0 /PCNTL	CCH0 /PCNTH	CCL1 /PLSCNTL	CCH1 /PLSCNTH	INTCTRL
F0	B			SPCR	SPSR	SPDR	I2CSADEN	EIPH
E8	EIE	I2CON	I2ADDR	NVMADDRH	I2DAT	I2STATUS	I2CLK	I2TIMER
E0	ACC	ADCCON	ADCH	ADCL		PDTC1	PDTC0	PWMCON4
D8	WDCON	PWMPL	PWM0L	NVMADDRL	PWMCON1	PWM2L	PWM6L	PWMCON3
D0	PSW	PWMPH	PWM0H	NVMDAT	QEICON	PWM2H	PWM6H	WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4L
C0	SCON1	SBUF1	T3MOD	T3CON	PMR	FSPLT	ADCPS	TA
B8	IP	SADEN	SADEN1	POVM	POVD	PIO	PWMEN	PWM4H
B0	P3	P5			RCAP3L	RCAP3H	EIP1H	IPH
A8	IE	SADDR	SADDR1		SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN	CAPCON0	CAPCON1	P4	CCL2 /MAXCNTL	CCH2 /MAXCNTH
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH	NVMCON	CHPCON
90	P1	EXIF	P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKCON1
80	P0	SP	DPL	DPH	TL3	TH3		PCON

Table 7-1: Special Function Register Location Table

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB								SYMBOL	RESET
INTCTRL	INTERRUPT CONTROL REGISTER	FFH	-	-	INT5CT1	INT5CT0	INT4CT1	INT4CT0	INT3CT1	INT3CT0		xx00 0000B
CCH1 /PLSCNTH	CAPTURE COUNTER HIGH 1 REGISTER	FEH	CCH1.7 /PLSCNTH.7	CCH1.6 /PLSCNTH.6	CCH1.5 /PLSCNTH.5	CCH1.4 /PLSCNTH.4	CCH1.3 /PLSCNTH.3	CCH1.2 /PLSCNTH.2	CCH1.1 /PLSCNTH.1	CCH1.0 /PLSCNTH.0		0000 0000B
CCL1 /PLSCNTL	CAPTURE COUNTER LOW 1 REGISTER	FDH	CCL1.7 /PLSCNTL.7	CCL1.6 /PLSCNTL.6	CCL1.5 /PLSCNTL.5	CCL1.4 /PLSCNTL.4	CCL1.3 /PLSCNTL.3	CCL1.2 /PLSCNTL.2	CCL1.1 /PLSCNTL.1	CCL1.0 /PLSCNTL.0		0000 0000B
CCH0 /PCNTH	CAPTURE COUNTER HIGH 0 REGISTER	FCH	CCH0.7 /PCNTH.7	CCH0.6 /PCNTH.6	CCH0.5 /PCNTH.5	CCH0.4 /PCNTH.4	CCH0.3 /PCNTH.3	CCH0.2 /PCNTH.2	CCH0.1 /PCNTH.1	CCH0.0 /PCNTH.0		0000 0000B
CCL0 /PCNTL	CAPTURE COUNTER LOW 0 REGISTER	FBH	CCL0.7 /PCNTL.7	CCL0.6 /PCNTL.6	CCL0.5 /PCNTL.5	CCL0.4 /PCNTL.4	CCL0.3 /PCNTL.3	CCL0.2 /PCNTL.2	CCL0.1 /PCNTL.1	CCL0.0 /PCNTL.0		0000 0000B
EIP1	EXTENDED INTERRUPT PRIORITY 1	FAH	-	-	PNVMI	PCPTF	PT3	PBKF	PPWMF	PSPI		xx00 0000B
EIE1	INTERRUPT ENABLE 1	F9H	-	-	ENVM	ECPTF	ET3	EBK	EPWM	ESPI		xx00 0000B
EIP	EXTENDED INTERRUPT PRIORITY	F8H	(FF) PS1	(FE) PX5	(FD) PX4	(FC) PWDI	(FB) PX3	(FA) PX2	(F9) -	(F8) PI2C		0000 00x0B
EIPH	EXTENDED INTERRUPT HIGH PRIORITY	F7H	PS1H	PX5H	PX4H	PWDIH	PX3H	PX2H	-	PI2CH		0000 00x0B
I2CSADEN	I2C SLAVE ADDRESS MASK	F6H	I2CSADEN.7	I2CSADEN.6	I2CSADEN.5	I2CSADEN.4	I2CSADEN.3	I2CSADEN.2	I2CSADEN.1	I2CSADEN.0		1111 1110B
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0		xxxx xxxxB
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-		0000 0xxxB
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0		0000 0100B
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)		0000 0000B
I2TIMER	I2C TIMER COUNTER REGISTER	EFH	-	-	-	-	-	ENTI	DIV4	TIF		xxxx x000B
I2CLK	I2C CLOCK RATE	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0		0000 0000B
I2STATUS	I2C STATUS REGISTER	EDH										1111 1000B
I2DAT	I2C DATA	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0		0000 0000B
NVMADDRH	NVM HIGH BYTE ADDRESS	EBH	-	-	-	-	-	NVMADDRH.10	NVMADDRH.9	NVMADDRH.8		xxxx x000B
I2ADDR	I2C SLAVE ADDRESS	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC		0000 0000B
I2CON	I2C CONTROL REGISTER	E9H	-	ENS	STA	STO	SI	AA	I2CIN	-		X000 000xB
EIE	EXTENDED INTERRUPT ENABLE	E8H	(EF) ES1	(EE) EX5	(ED) EX4	(EC) EWDI	(EB) EX3	(EA) EX2	(E9)	(E8) EI2C		0000 00x0B
PWMCON4	PWM CONTROL REGISTER 4	E7H	PWMEOM	PWMOOM	PWM6OM	PWM7OM	-	-	-	BKF		0000 xxx0B
PDTC0	DEAD TIME CONTROL REGISTER 0	E6H	PDTC0.7	PDTC0.6	PDTC0.5	PDTC0.4	PDTC0.3	PDTC0.2	PDTC0.1	PDTC0.0		0000 0000B
PDTC1	DEAD TIME CONTROL REGISTER 1	E5H	PDTC1.7	PDTC1.6	PDTC1.5	PDTC1.4	PDTC1.3	PDTC1.2	PDTC1.1	PDTC1.0		0000 0000B
ADCL	ADC CONVERTER RESULT LOW BYTE	E3H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0		00xx xxxxB

P4.1 BASE ADDRESS HIGH BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P41AH Address: 97h

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial Port mode select bit 0 or Framing Error Flag: This bit is controlled by the SMOD0 bit in the PCON register. (SM0) See table below. (FE) This bit indicates an invalid stop bit. It must be manually cleared by software.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Serial Port Clock or Multi-Processor Communication. (Mode 0) This bit controls the serial port clock. If set to zero, the serial port runs at a divide-by-12 clock of the oscillator. This is compatible with the standard 8051/52. If set to one, the serial clock is a divide-by-4 clock of the oscillator. (Mode 1) If SM2 is set to one, RI is not activated if a valid stop bit is not received. (Modes 2 / 3) This bit enables multi-processor communication. If SM2 is set to one, RI is not activated if RB8, the ninth data bit, is zero.
4	REN	Receive enable: 1: Enable serial reception. 0: Disable serial reception.
3	TB8	(Modes 2 / 3) This is the 9th bit to transmit. This bit is set by software.
2	RB8	(Mode 0) No function. (Mode 1) If SM2 = 0, RB8 is the stop bit that was received. (Modes 2 / 3) This is the 9th bit that was received.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or at the beginning of the stop bit in the other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or halfway through the stop bits in the other modes during serial reception. However, SM2 can restrict this behavior. This bit can only be cleared by software.

SM1, SM0: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Continued

BIT	NAME	FUNCTION
1-0	CCLD.1-0	Reload trigger select. CCLD1 / CCLD0 / Description 0 / 0 / Timer 3 overflow (default) 0 / 1 / Reload by capture 0 block 1 / 0 / Reload by capture 1 block 1 / 1 / Reload by capture 2 block

CAPTURE CONTROL 1 REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	ENF2	ENF1	ENF0	CPTF2	CPTF1/	CPTF0

Mnemonic: CAPCON1 Address: A4h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	ENF2	Enable filter for capture input 2.
4	ENF1	Enable filter for capture input 1.
3	ENF0	Enable filter for capture input 0.
2	CPTF2	Input capture/reload 2 interrupt flag.
1	CPTF1/DIRF	Input Capture 2 flag share the same bit with DIRF flag. **IC mode** - Input capture/reload 1 interrupt flag. **QEI mode** - Direction changed interrupt flag. Bit is set by hardware when direction index (DIR) changes state and direction change interrupt is requested if it is enabled. DIRF is cleared by software.
0	CPTF0/QEIF	Input Capture 0 flag share the same bit with QEI flag. **IC mode** – Input capture/reload 0 interrupt flag. **QEI mode** - QEI interrupt flag. 1. In free-counting mode, if Pulse Counter overflows or underflows. 2. In compare-counting mode, if Pulse Counter overflows from Maximum Count to zero or underflows from zero to Maximum Count.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-2	P4	GPIO.
1	P4	GPIO. Alternate function T2EX/IC2 for Timer 2 external trigger/Input Capture 2 respectively.
0	P4	GPIO. Alternate function STADC. External start ADC trigger input.

	ALTERNATE FUNCTION
P5.1	PWM7 output function
P5.0	PWM6 output function

TIMER 3 RELOAD LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP3L.7	RCAP3L.6	RCAP3L.5	RCAP3L.4	RCAP3L.3	RCAP3L.2	RCAP3L.1	RCAP3L.0

Mnemonic: RCAP3L Address: B4h

BIT	NAME	FUNCTION
7-0	RCAP3L	Timer 3 Reload LSB: This register is LSB of a 16 bit reload value when timer 3 is configured in reload mode. It served also as a compare register when timer 3 is configured as compare mode (see CMP/RL3 bit).

TIMER 3 RELOAD MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP3H.7	RCAP3H.6	RCAP3H.5	RCAP3H.4	RCAP3H.3	RCAP3H.2	RCAP3H.1	RCAP3H.0

Mnemonic: RCAP3H Address: B5h

BIT	NAME	FUNCTION
7-0	RCAP3H	Timer 3 Reload MSB: This register is MSB of a 16 bit reload value when timer 3 is configured in reload mode. It served also as a compare register when timer 3 is configured as compare mode (see CMP/RL3 bit).

EXTENDED INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	-	-	PNVMIH	PCPTFH	PT3H	PBKFH	PPWMFH	PSPIH

Mnemonic: EIP1 Address: B6h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	PNVMIH	NVM interrupt High priority. PNVMIH = 1 sets it to highest priority level.
4	PCPTFH	Capture/reload Interrupt High priority. PCPTFH = 1 sets it to highest priority level.
3	PT3H	Timer 3 Interrupt High priority. PT3H = 1 sets it to highest priority level.
2	PBKFH	PWM Brake Interrupt High priority. PBKFH = 1 sets it to highest priority level.
1	PPWMFH	PWM period Interrupt High priority. PPWMFH = 1 sets it to highest priority level.
0	PSPIH	SPI Interrupt High Priority. PSPIH = 1 sets it to highest priority level.

INTERRUPT HIGH PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PT2H	PSHH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IPH Address: B7h

14. PULSE-WIDTH-MODULATED (PWM) OUTPUTS

14.1 PWM Features

The PWM block supports the following features;

- Four 12-bit PWM channels or complementary pairs:
  - 4 independent PWM outputs: PWM0, PWM2, PWM4 & PWM6.
  - 4 complementary PWM pairs with insertion of programmable dead-time: (PWM0,PWM1), (PWM2,PWM3), (PWM4,PWM5), (PWM6,PWM7)
- Three operation mode:
  Edge aligned mode, Center aligned mode and Single shot mode.
- Programmable dead-time insertion between paired PWMs.
- Output override control for Electrically Commutated Motor operation.
- Hardware/software brake protection.
- Support 2 independent interrupts:
  - Interrupt request when up/down counter comparison matched or underflow.
  - Interrupt request when external brake asserted.
- Flexible operation in debug mode.
- High Source/Sink current.

The outputs for PWM0 to PWM7 are on P2[5:0] (PWM[5:0]) and P5[1:0] (PWM [7:6]) respectively. After CPU reset, the internal output of each PWM channel depends on the output controls and polarity settings. The interval between successive outputs is controlled by a 12–bit up/down counter which uses the oscillator frequency with configurable internal clock prescaler as its input. The PWM counter clock, has the frequency as the clock source $F_{PWM} = F_{OSC}$/Prescaler. The following Figure 14-1: PWM Block Diagram below is the block diagram for PWM.

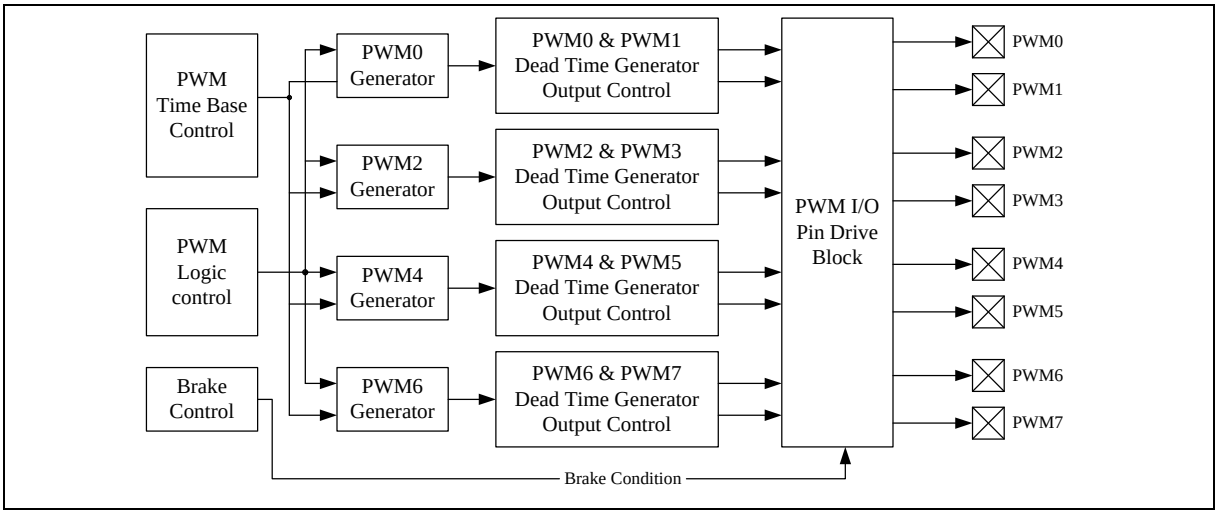

Figure 14-1: PWM Block Diagram

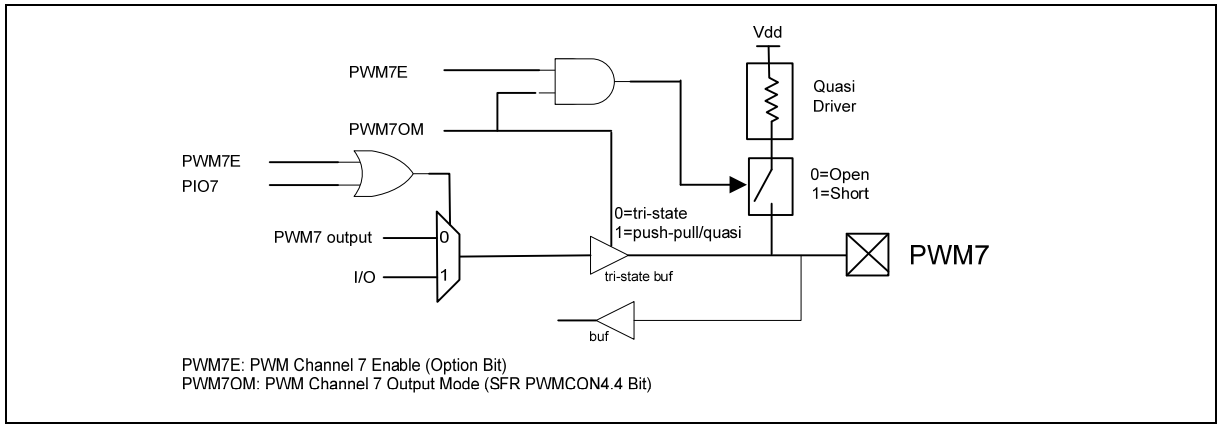

Figure 14-6: PWM7 I/O pin

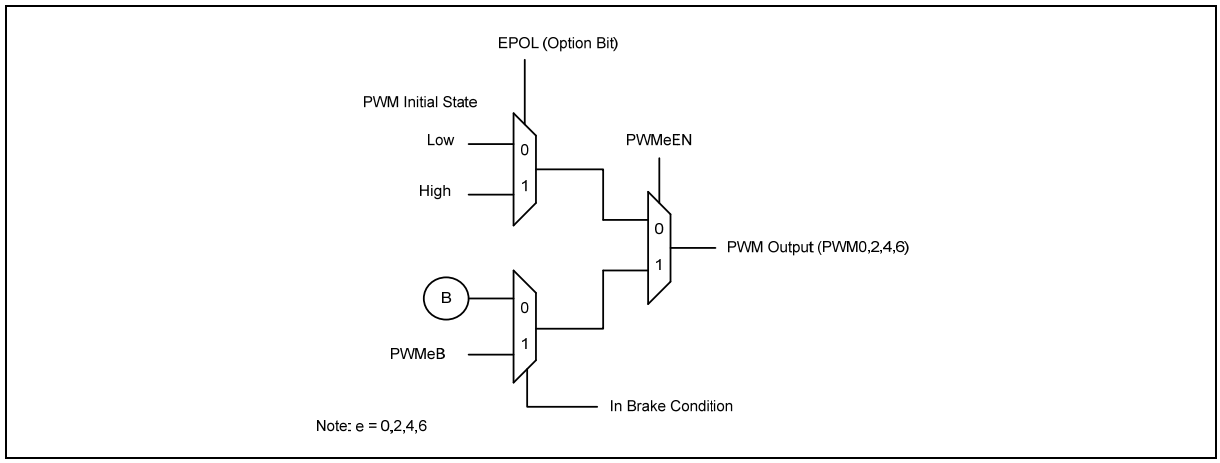

Figure 14-7: Even PWM Output

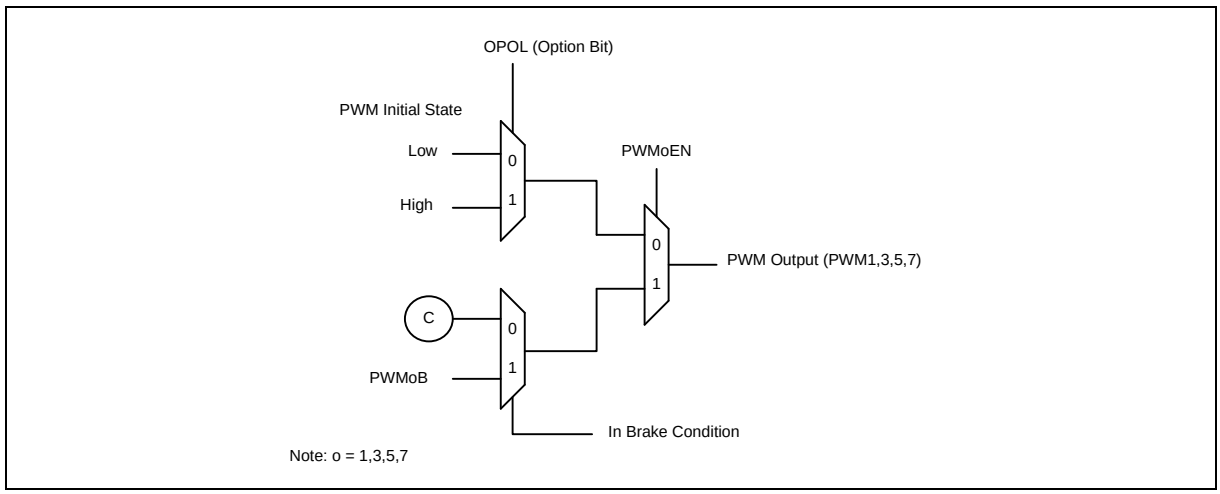

Figure 14-8: Odd PWM Output

14.10 Smart Fault Detector

This is a brake detection logic that is new to support external brake conditions that already exist. A dedicated SFR FSPLT is added for this function. The SFR consists of smart fault detector control and status bits. It basically consists of a clock divider, 8 bits counter, comparator and 4 selectable compare values. The following diagram show the general block diagram.

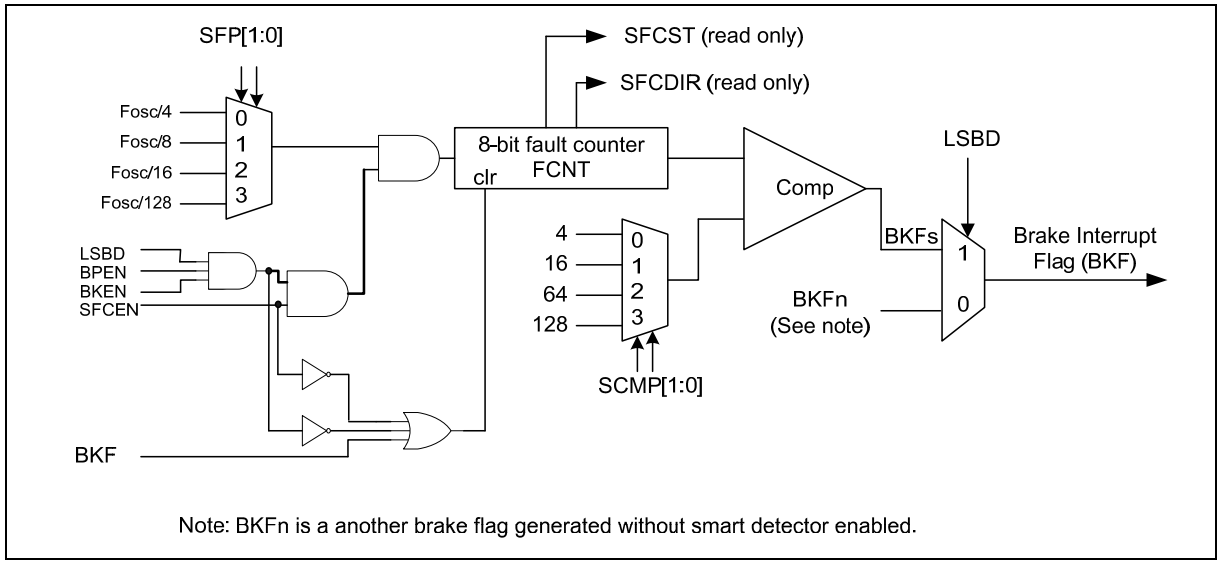

Figure 14-25: Smart Fault Detector

The smart fault detector is enabled when bit LSBD = 1 (FSPLT.0). This logic detects low level brake pin. The 8 bits counter is enabled by SFCEN bit located in SFR FSPLT.3. The counter is clock by Fosc divider selectable by SFP1-0 control bits (FSPLT.5-4). The comparator compares the 8 bits counter value with the compare value selectable with SCMP1-0 (FSPLT1-0).

Upon initial detection of low level at brake pin, the 8 bits counter will be active. This will cause the counter to increment. While the counter is active and there is high level detected at brake pin, the counter will decrement. See next figure for timing diagram. When the counter value reaches compare value, BKF will be asserted.

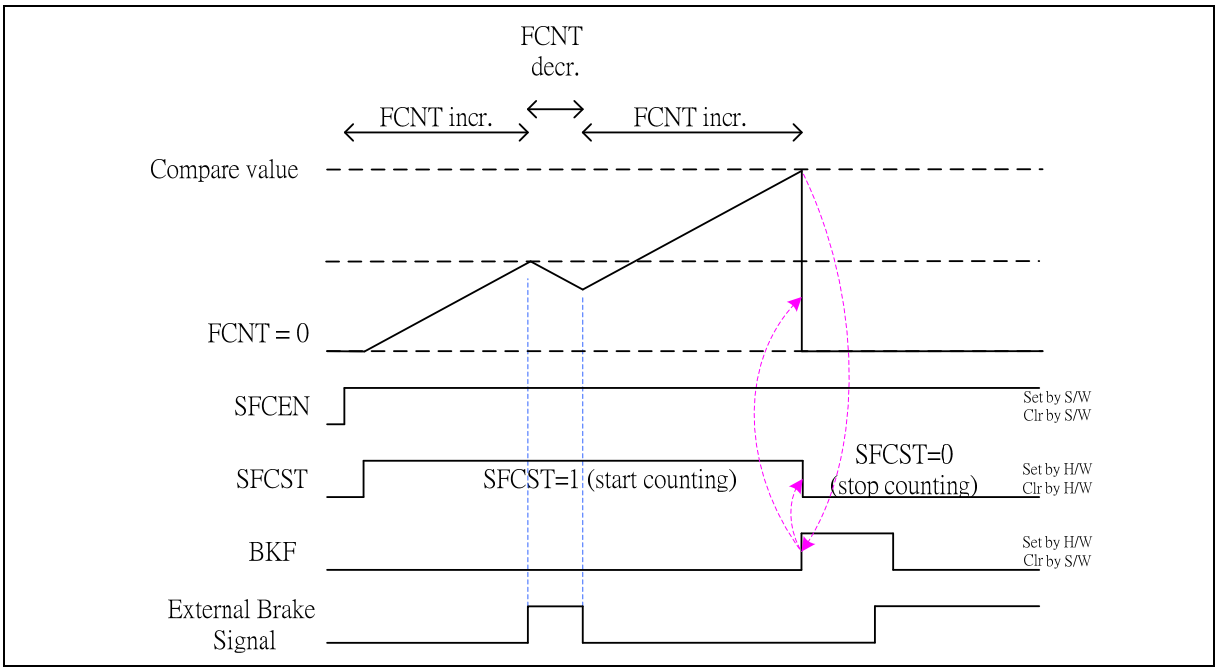

Figure 14-26: Smart Fault Detector timing diagram

The smart fault detector consists of 2 status bits; SFCST and SFCDIR. A SFCST show status of 8 bits counter is active or in-active, while SFCDIR shows the counter's counting direction. When SFCST = 0, SFCDIR keeps its' state.

The s/w can manually disable and clear the 8 bits counter, by clearing SFCEN to 0.

The following tables show the tabulate accumulated low level Brake time with various Fosc/x dividers and compares value, at 40MHz and 20MHz.

FOSC/X	1/4	1/8	1/16	1/128
SCMP[1:0]	10,000,000	5,000,000	2,500,000	312,500
4	0.40us	0.80us	1.60us	12.80us
16	1.60us	3.20us	6.40us	51.20us
64	6.40us	12.80us	25.60us	204.80us
128	12.80us	25.60us	51.20us	409.60us

Table 14-5: Example the accumulated low level time at 40 MHz

FOSC/X	1/4	1/8	1/16	1/128
SCMP[1:0]	5,000,000	2,500,000	1,250,000	156,250
4	0.80us	1.60us	3.20us	25.60us
16	3.20us	6.40us	12.80us	102.40us
64	12.80us	25.60us	51.20us	409.60us
128	25.60us	51.20us	102.40us	819.20us

Table 14-6: Example the accumulated low level time at 20 MHz

Figure 16-1 Serial Port Mode 0

The serial port receives data when REN is 1 and RI is zero. The shift clock (TxD) is activated, and the serial port latches data on the rising edge of the shift clock. The external device should, therefore, present data on the falling edge of the shift clock. This process continues until all eight bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock, which stops reception until RI is cleared by the software.

16.2 Mode 1

In Mode 1, full-duplex asynchronous communication is used. Frames consist of ten bits transmitted on TXD and received on RXD. The ten bits consist of a start bit (0), eight data bits (LSB first), and a stop bit (1). When receiving, the stop bit goes into RB8 in SCON. The baud rate in this mode is 1/16 or 1/32 of the Timer 1 overflow, and since Timer 1 can be set to a wide range of values, a wide variation of baud rates is possible.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed at C1 following the next rollover. After all eight bits are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the tenth rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted immediately, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in eight data bits, the stop bit is received. Then, if;

1. RI is 0, and
2. SM2 is 0 or the received stop bit is 1,

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame is lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD.

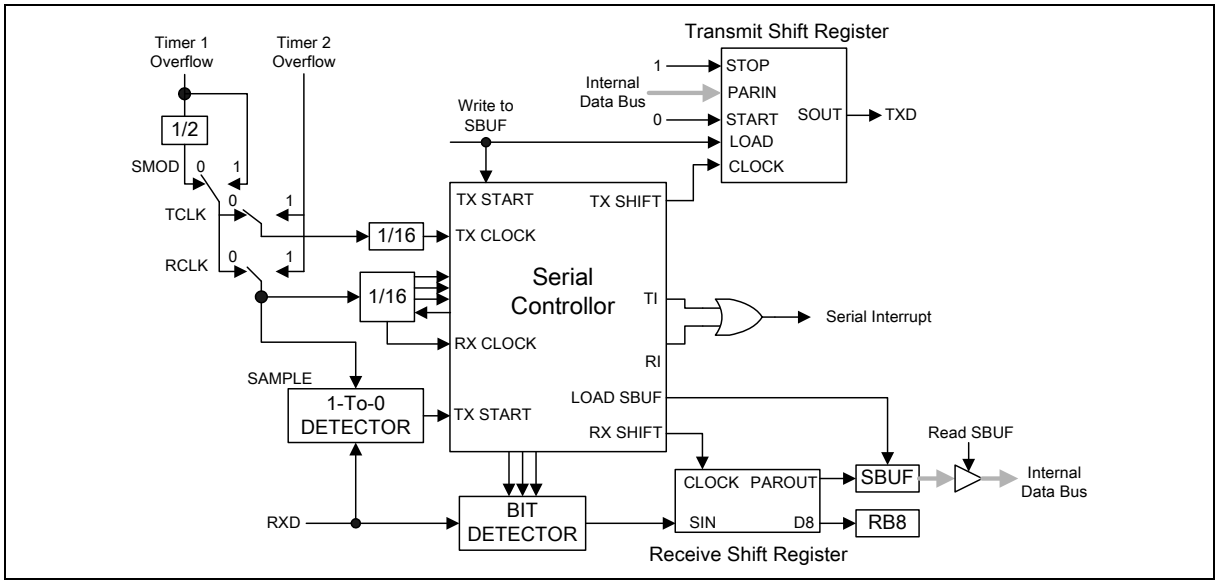

Figure 16-2 Serial Port Mode 1

17. I2C SERIAL PORTS

The I2C bus uses two wires (SCL and SDA) to transfer information between devices connected to the bus. The main features of the I2C bus are:

– Bi-directional data transfer between masters and slaves.

– Multi-master bus (no central master).

– Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.

– Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

– Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

– The I2C bus may be used for test and diagnostic purposes.

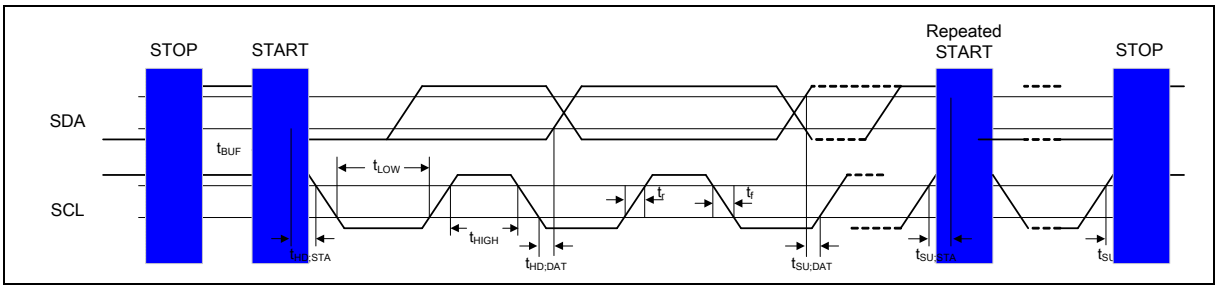

Figure 17-1: I2C Bus Timing

The device's on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register (I2STATUS) reflects the status of the I2C bus.

The I2C port, SCL and SDA are at P2.6 and P2.7. When the I/O pins are used as I2C port, user must set the pins to logic high in advance. When I2C port is enabled by setting ENS to high, the internal states will be controlled by I2CON and I2C logic hardware. Once a new status code is generated and stored in I2STATUS, the I2C interrupt flag (SI) will be set automatically. If both EA and EI2C are also in logic high, the I2C interrupt is requested. The 5 most significant bits of I2STATUS stores the internal state code, the lowest 3 bits are always zero and the content keeps stable until SI is cleared by software.

17.1 SIO Port

The SIO port is a serial I/O port, which supports all transfer modes from and to the I2C bus. The SIO port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The CPU interfaces to the SIO port through the seven special function registers. The detail description of these registers can be found in the I2C Control registers section. The SIO H/W interfaces to the I2C bus via two pins: SDA (P2.7, serial data line) and SCL (P2.6, serial clock line). Pull up resistor is needed for Pin P2.6 and P2.7 for I2C operation as these are 2 open drain pins.

17.2 The I2C Control Registers

The I2C has 1 control register (I2CON) to control the transmit/receive flow, 1 data register (I2DAT) to buffer the Tx/Rx data, 1 status register (I2STATUS) to catch the state of Tx/Rx, recognizable slave address register for slave mode use and 1 clock rate control block for master mode to generate the variable baud rate.

18. SERIAL PERIPHERAL INTERFACE (SPI)

18.1 General descriptions

This device consists of SPI block to support high speed serial communication. It's capable of supporting data transfer rates 5Mbit/s. This device's SPI support the following features;

- Master and slave mode.
- Slave select output.
- Programmable serial clock's polarity and phase.
- Receive double buffered data register.
- LSB first enable.
- Write collision detection.
- Transfer complete interrupt.

18.2 Block descriptions

The Figure 18-1 shows SPI block diagram. It provides an overview of SPI architecture in this device. The main blocks of SPI are the register blocks, control logics, baud rate control and pin control logics;

a. Shift register and read data buffer. It is single buffered in the transmit direction and double buffered in the receive direction. Transmit data cannot be written to the shifter until the previous transfer is complete. Receive logics consist of parallel read data buffer so the shifter is free to accept a second data, as the first received data will be transferred to the read data buffer.
b. SPI Control block. This provide control functions to configure the device for SPI enable, master or slave, clock phase and polarity, LSB access first selection, and Slave Select output enable.
c. Baud rate control. These control logics divide CPU clock to 4 different selectable clocks 1/8, 1/32, 1/128 and 1/2/256. Its' selection is controllable through SPR [1:0] bits.

SPR1	SPR0	DIVIDER	BAUD RATE
0	0	8	5MHz
0	1	32	1.25MHz
1	0	128	312.50kHz
1	1	256	156.25kHz

Table 18-1 SPI Baud Rate Selection (F_{OSC} @ 40MHz)

d. SPI registers. There are three SPI registers to support its operations, they are;
   - SPI control registers (SPCR)
   - SPI status registers (SPSR)
   - SPI data register (SPDR)

   These registers provide control, status, data storage functions and baud rate selection control. Detail bits descriptions are found at SFR section. When using SPI pull-up must be apply at bit PUP0 = 1.
e. Pin control logic. Controls behavior of SPI interface pins.

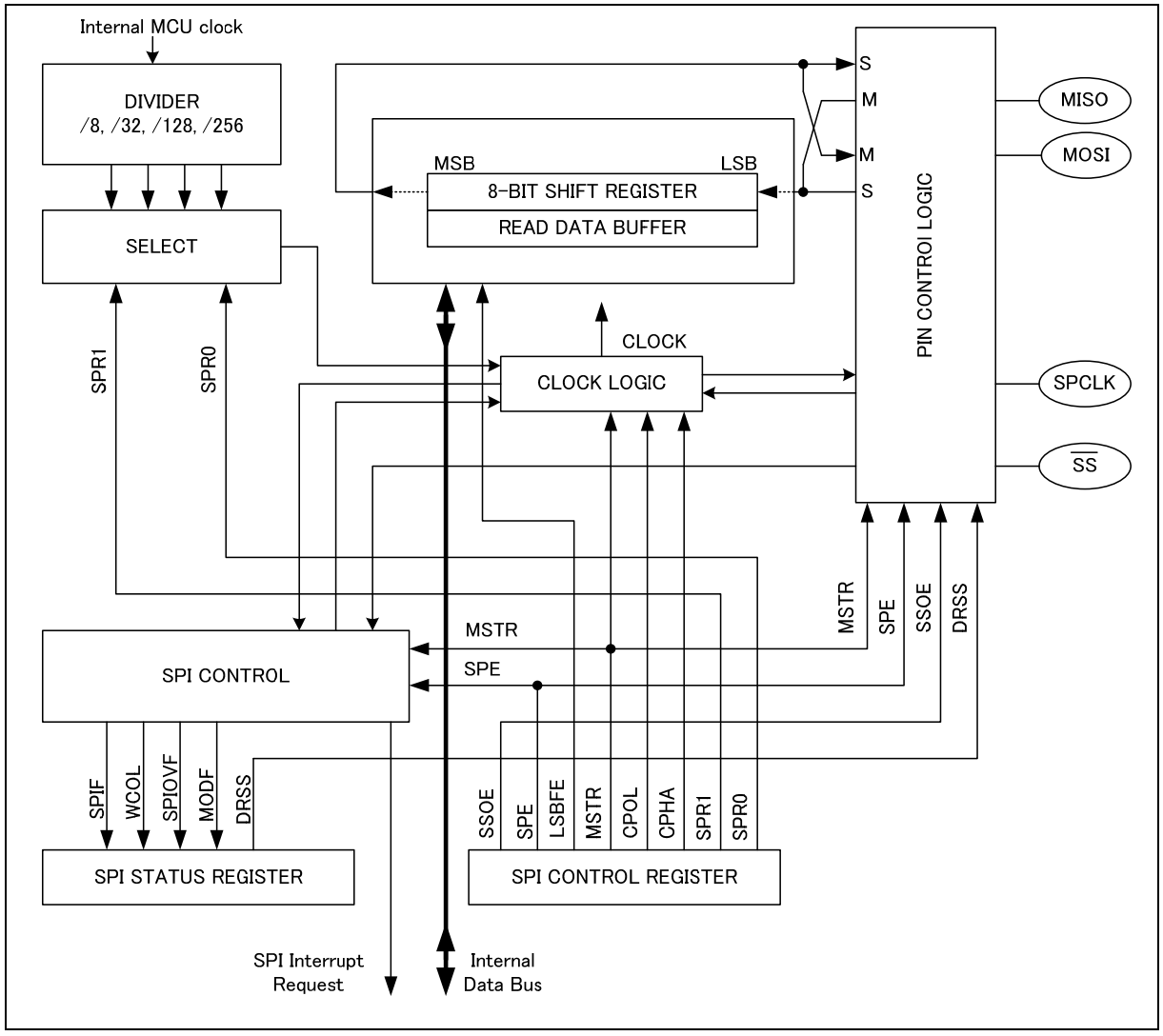

Figure 18-1: SPI block diagram

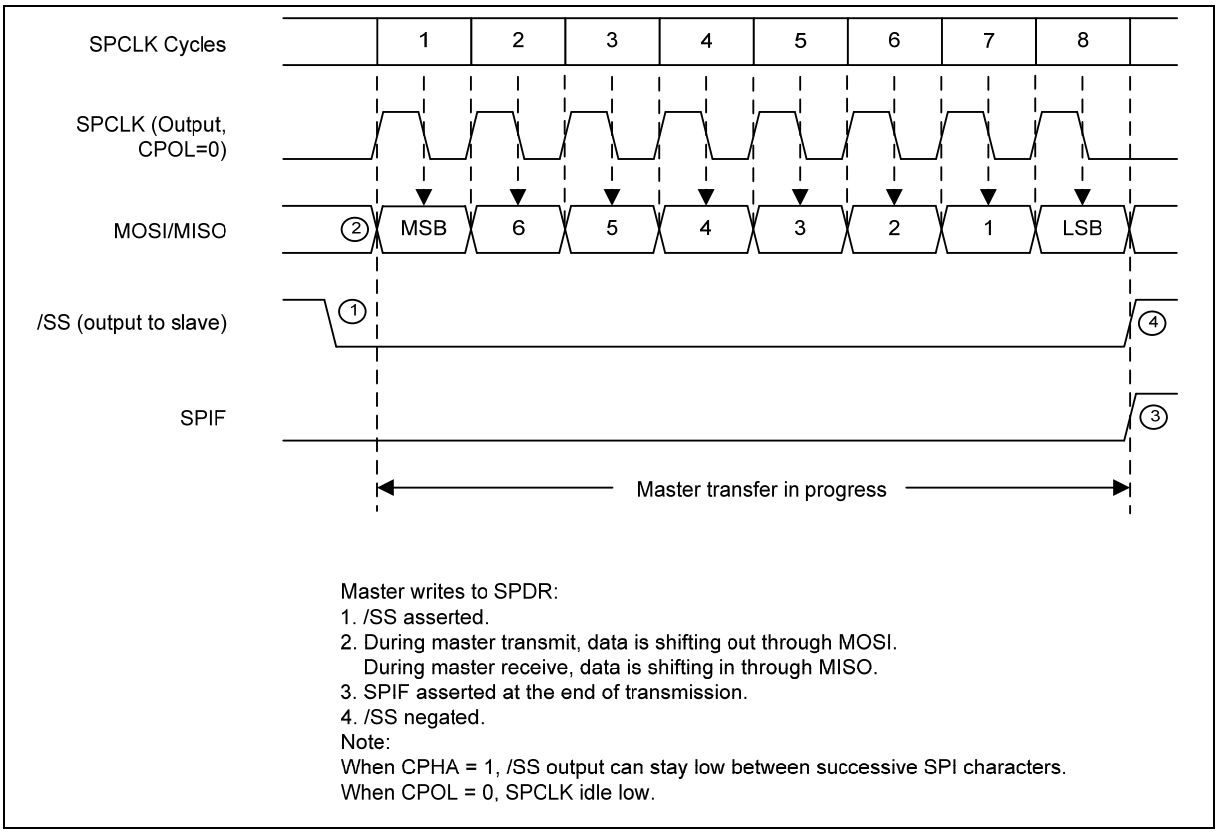

Figure 18-4: Master Mode Transmission (CPOL = 0, CPHA = 1)

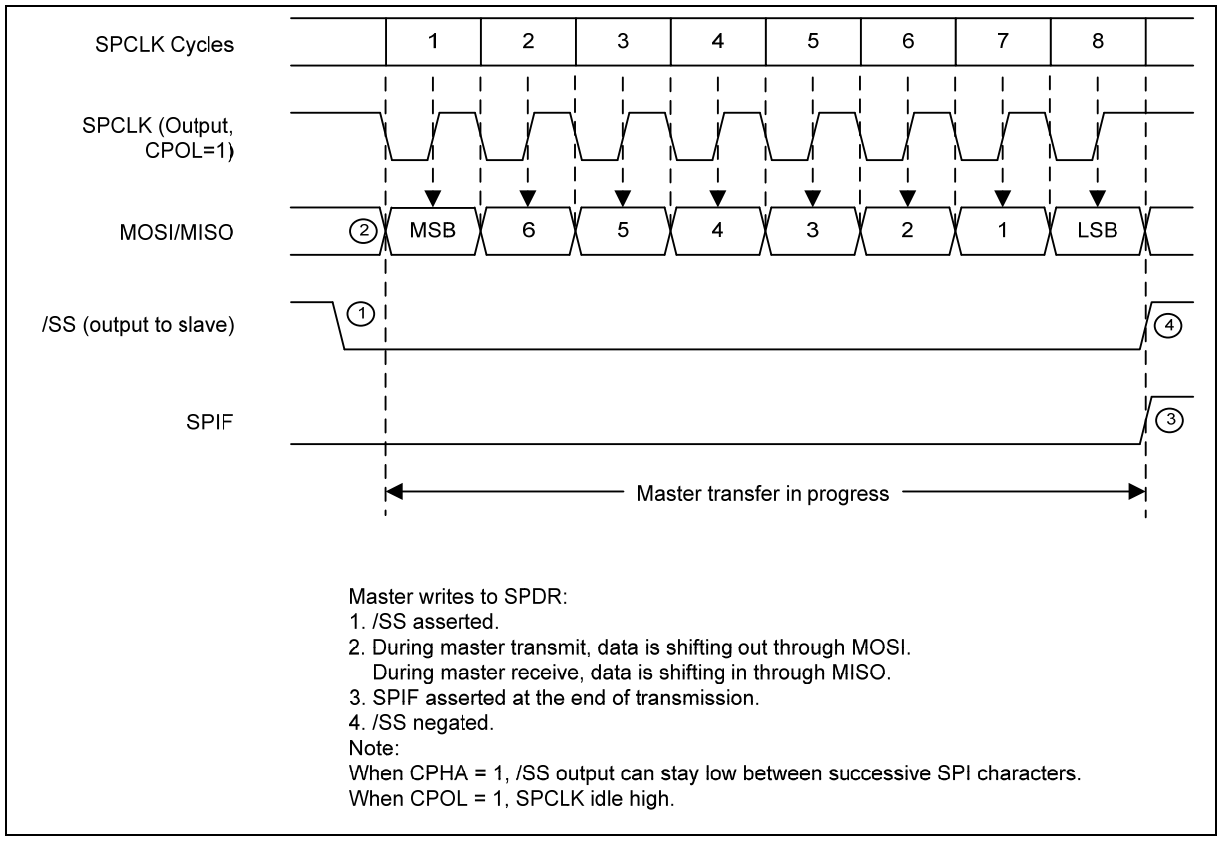

Figure 18-5: Master Mode Transmission (CPOL = 1, CPHA = 1)

18.3.2 Slave Mode

When in slave mode, the SPCLK pin becomes input and it will be clock by another master SPI device. The $\overline{SS}$ pin also becomes input. Similarly, before data transmissions occurs, and remain low until the transmission completed. If $\overline{SS}$ goes high, the SPI is forced into idle state. If the $\overline{SS}$ is forced to high at the middle of transmission, the transmission will be aborted and the receiving shifter buffer will be high and goes into idle states.

Data flows from master to slave on MOSI pin and flows from slave to master on MISO pin. The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices.

A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

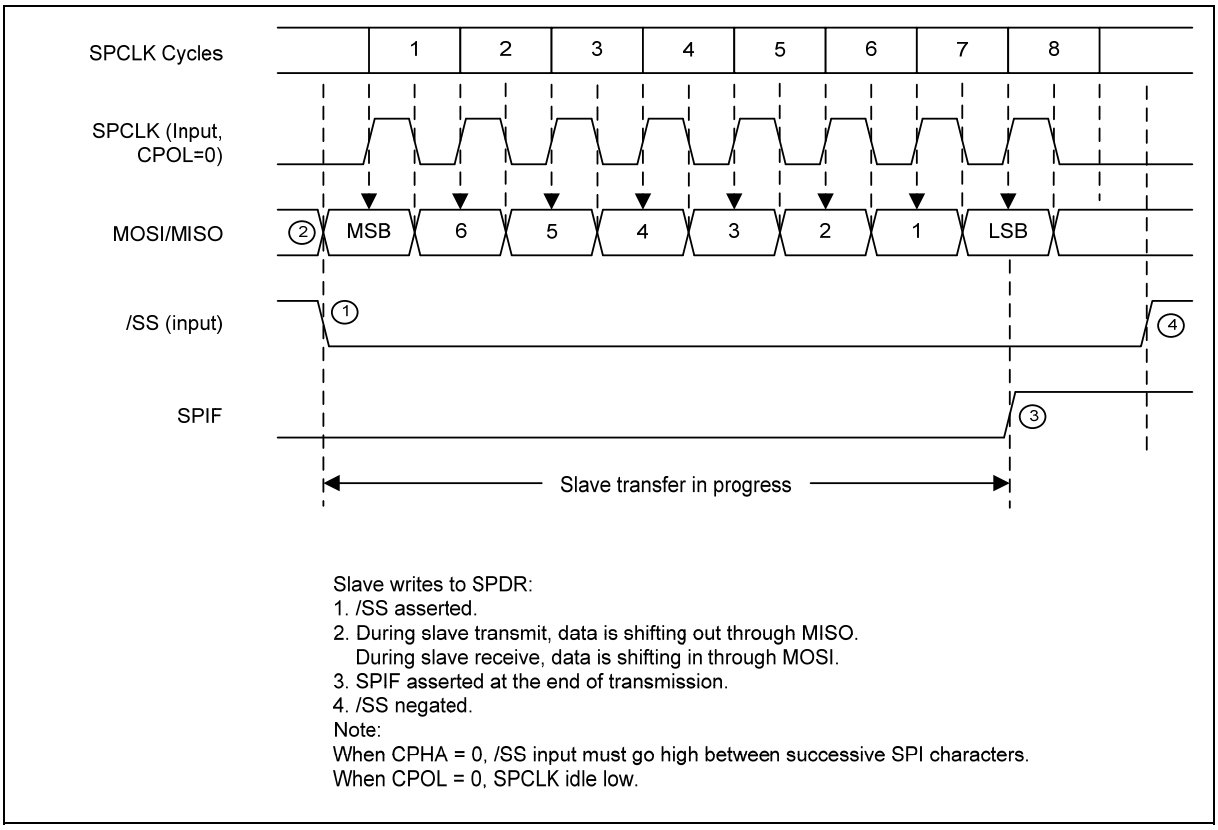

Figure 18-6: Slave Mode Transmission (CPOL = 0, CPHA = 0)

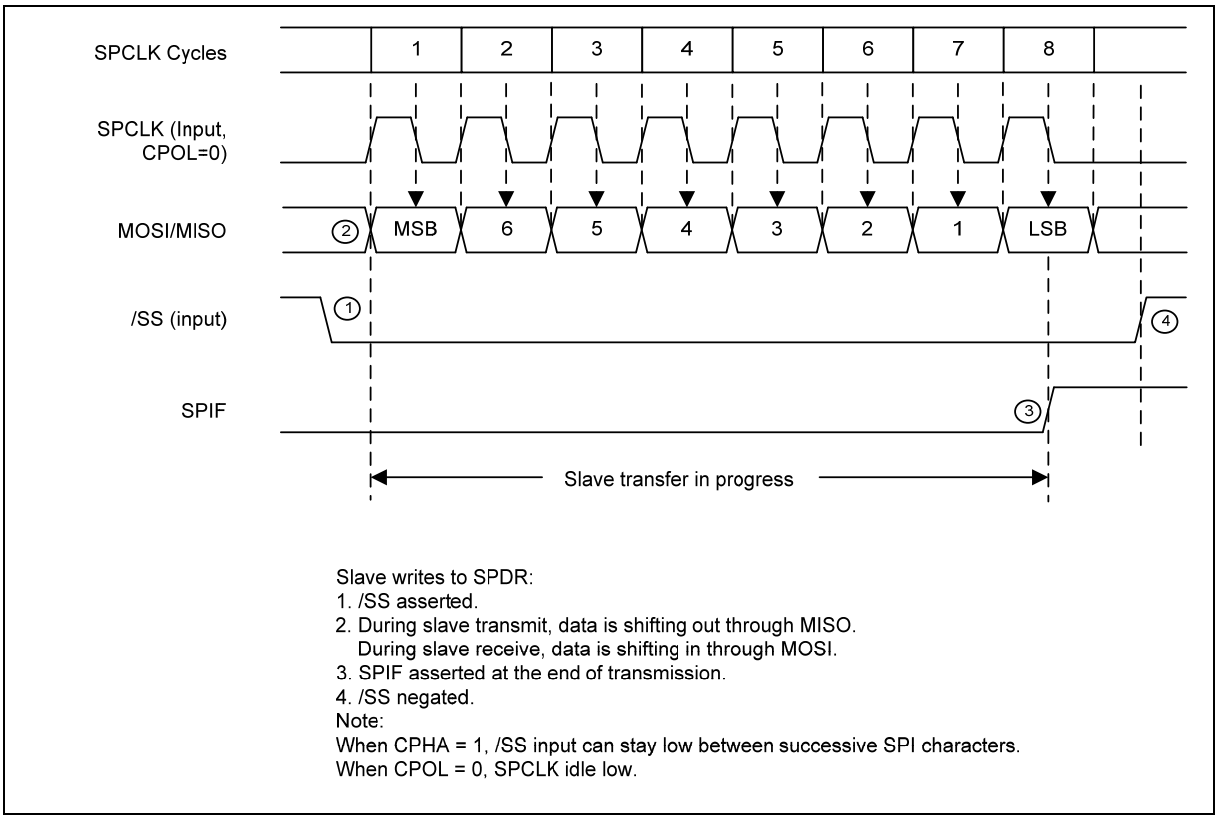

Figure 18-8: Slave Mode Transmission (CPOL = 0, CPHA = 1)

18.3.6 Programmable serial clock's phase and polarity

The clock polarity CPOL control bit selects active high or active low SPCLK clock, and has no significant effect on the transfer format. The clock phase CPHA control bit selects one of two different transfer protocols by sampling data on odd numbered SPCLK edges or on even numbered SPCLK edges. Thus, both these bits enable selection of four possible clock formats to be used by SPI system.

The clock phase and polarity should be identical for the master SPI device and the communicating slave device.

When CPHA equals 0, the $\overline{SS}$ line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is low, a write collision error results. When CPHA equals 1, the $\overline{SS}$ line can remain low between successive transfers. The figures from

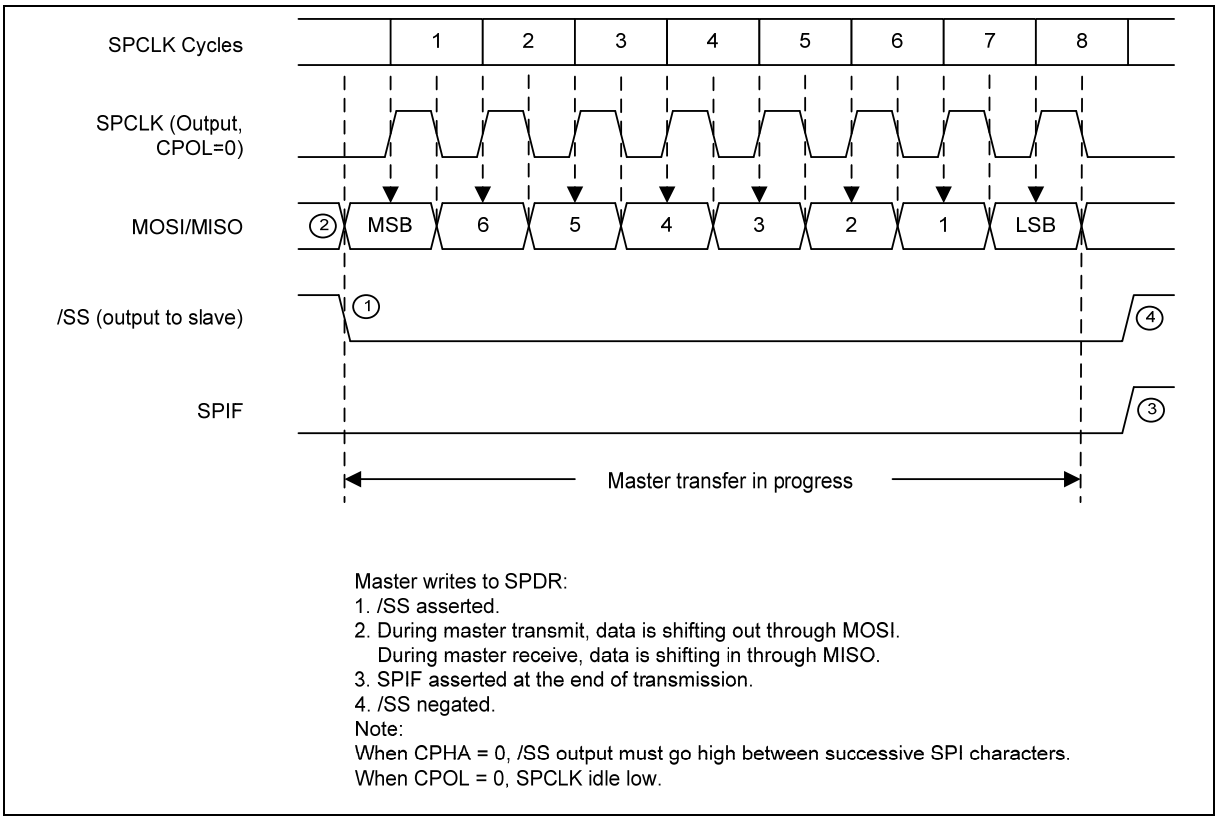

Figure 18-2 to

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