Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051/52
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e227apg

INSTRUCTIONS		ENNVM = 1 NVM SIZE = SRAM (1K)	
		ADDR ≤ 1K	ADDR > 1K
Read access	MOVX A, @DPTR (Read)	NVM[1]	Ext memory[1]
	MOVX A, @R0 (Read)	NVM[2]	NOP
	MOVX A, @R1 (Read)	NVM[2]	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory[1]
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-2: W79E225 MOVX read/write access destination

INSTRUCTIONS		ENNVM = 1 NVM SIZE = SRAM (2K)	
		ADDR ≤ 2K	ADDR > 2K
Read access	MOVX A, @DPTR (Read)	NVM[1]	Ext memory[1]
	MOVX A, @R0 (Read)	NVM[2]	NOP
	MOVX A, @R1 (Read)	NVM[2]	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory[1]
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-3: W79E226/227 MOVX read/write access destination

Note:

1. A15~A0=DPTR
2. A15~A8=XRAMAH

Continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB SYMBOL								RESET
CCH2/MAXCNTH	INPUT CAPTURE 2 HIGH REGISTER/ MAXIMUM COUNTER HIGH REGISTER	A7h	CCH2.7 /MAXCNTH.7	CCH2.6 MAXCNTH.6	CCH2.5 /MAXCNTH.5	CCH2.4 /MAXCNTH.4	CCH2.3 /MAXCNTH.3	CCH2.2 /MAXCNTH.2	CCH2.1 /MAXCNTH.1	CCH2.0 /MAXCNTH.0	0000 0000B
CCL2/MAXCNTL	INPUT CAPTURE 2 LOW REGISTER/ MAXIMUM COUNTER LOW REGISTER	A6h	CCL2.7 /MAXCNTL.7	CCL2.6 /MAXCNTL.6	CCL2.5 /MAXCNTL.5	CCL2.4 /MAXCNTL.4	CCL2.3 /MAXCNTL.3	CCL2.2 /MAXCNTL.2	CCL2.1 /MAXCNTL.1	CCL2.0 /MAXCNTL.0	0000 0000B
P4	PORT 4	A5H	-	-	-	-	P4.3	P4.2	T2EX/IC2	STADC	xxxx 1111B
CAPCON1	CAPTURE CONTROL 1 REGISTER	A4H	-	-	ENF2	ENF1	ENF0	CPTF2	CPTF1/ DIRF	CPTF0/ QEIF	xx00 0000B
CAPCON0	CAPTURE CONTROL 0 REGISTER	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD1	CCLD0	0000 0000B
P4CSIN	P4 CS SIGN	A2H	P43INV	P42INV	P41INV	P40INV	-	PWDNH	RMWFP	P0UP	0000 x000B
XRAMAH	RAM HIGH BYTE ADDRESS	A1H	-	-	-	-	-	A10	A9	A8	0000 0000B
P2	PORT 2	A0H	(A7) A15/ SDA	(A6) A14/ SCL	(A5) A13/ PWM5	(A4) A12/ PWM4	(A3) A11/ PWM3	(A2) A10/ PWM2	(A1) A9/ PWM1	(A0) A8/ PWM0	1111 1111B
CHPCON	ON CHIP PROGRAMMING CONTROL	9FH	SWRST/ REBOOT	-	LD/AP	-	-	-	LDSEL	ENP	0000 0000B
NVMCON	NVM CONTROL	9EH	EER	EWR	EnNVM	-	-	-	-	NVMF	000x xxx0B
P43AH	HI ADDR. COMPARATOR OF P4.3	9DH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P43AL	LO ADDR. COMPARATOR OF P4.3	9CH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P42AH	HI ADDR. COMPARATOR OF P4.2	9BH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P42AL	LO ADDR. COMPARATOR OF P4.2	9AH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	xxxx xxxxB
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	HI ADDR. COMPARATOR OF P4.1	97H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P41AL	LO ADDR. COMPARATOR OF P4.1	96H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P40AH	HI ADDR. COMPARATOR OF P4.0	95H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P40AL	LO ADDR. COMPARATOR OF P4.0	94H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P4CONB	P4 CONTROL REGISTER B	93H	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0	0000 0000B
P4CONA	P4 CONTROL REGISTER A	92H	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0	0000 0000B
EXIF	EXTERNAL INTERRUPT FLAG	91H	IE5	IE4	IE3	IE2	-	-	-	-	0000 xxxxB
P1	PORT 1	90H	(97) ADC7	(96) ADC6	(95) ADC5	(94) ADC4	(93) TXD1/ ADC3	(92) RXD1/ ADC2	(91) ADC1/ Brake	(90) T2/ ADC0	1111 1111B
CKCON1	CLOCK CONTROL 1	8FH	-	-	-	-	-	-	CCDIV1	CCDIV0	0000 0000B
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8032 16-bit data pointer.

TIMER 3 LSB

Bit:	7	6	5	4	3	2	1	0
	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0

Mnemonic: TL3 Address: 84h

BIT	NAME	FUNCTION
7-0	Timer 3 LSB	LSB of Timer3

TIMER 3 MSB

Bit:	7	6	5	4	3	2	1	0
	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0

Mnemonic: TH3 Address: 85h

BIT	NAME	FUNCTION
7-0	Timer 3 MSB	MSB of Timer3

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD0	Framing Error Detection Enable. When SMOD0 is set to 1, then SCON.7 (SCON1.7) now indicates a Frame Error and acts as the FE (FE_1) flag. When SMOD0 is 0, then SCON.7 (SCON1.7) acts as per the standard 8032 function.
5-4	-	Reserved.
3-2	GF1-0	These two bits are general purpose user flags.
1	PD	Setting this bit causes the device to go into the POWERDOWN mode. In this mode all the clocks are stopped and program execution is frozen.
0	IDL	Setting this bit causes the device to go into the IDLE mode. In this mode the clock to the CPU is stopped, so program execution is frozen, but the clock to the serial ports, timer, PWM, ADC, SPI and interrupt blocks is not stopped, and these blocks continue operating unhindered.

BIT	NAME	FUNCTION
7-6	SCMP [1:0]	Smart fault compare value selector (read/write): 00 = 4 01 = 16 10 = 64 11 = 128
5-4	SFP[1:0]	Smart fault sampling frequency selector (read/write): 00 = FOSC/4 01 = FOSC/8 10 = FOSC/16 11 = FOSC/128
3	SFCEN	Smart fault/brake counter enable (read/write): 0 = Disable, and clear internal smart fault counter. 1 = Enable smart fault detector.
2	SFCST	Smart fault/brake counter status (read only): 0 = Counter is non-active. 1 = Counter is active.
1	SFCDIR	Smart fault/brake counters direction status (read only): 0 = Down counting. 1 = Up counting.
0	LSBD	Low level smart brake detector: 0 = Disable low level smart brake detector. 1 = Enable low level smart brake detector. It will be cleared by software.

ADC PIN SELECT

Bit:	7	6	5	4	3	2	1	0
	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0

Mnemonic: ADCPS Address: C6h

BIT	NAME	FUNCTION
7-0	ADCPS	ADC input pin select. There are 8 ADC input pins shared with P1.0~P1.7. Its' functions are controlled by the bit value in ADCPS. Set the bit to switch the corresponding pin to ADC input port; clear the bit to disable the pin to perform ADC input port. The reset value is 00H.

BIT	CORRESPONDING PIN	BIT	CORRESPONDING PIN
ADCPS.0	P1.0	ADCPS.4	P1.4
ADCPS.1	P1.1	ADCPS.5	P1.5
ADCPS.2	P1.2	ADCPS.6	P1.6
ADCPS.3	P1.3	ADCPS.7	P1.7

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION

BIT	NAME	FUNCTION
7~0	NVMDAT.7~NVMDAT.0	The NVM data write register. The read NVM data is by MOVX instruction.

QEI CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	DISIDX	DIR	QEIM1	QEIM0	QEIEN

Mnemonic: QEICON Address: D4h

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	DISIDX	Disable Input Capture 2 edge detection function: 0 = Enable IC2 edge detection function (default). 1 = Disable IC2 edge detection function. This bit is effective when QEIEN=1.
3	DIR	Direction index of motion detection bit: 1 = Forward (Up-counting). 0 = Backward (Down-counting). This bit is writable and readable.
2-1	QEIM[1:0]	QEI mode select bits: QEIM1 / QEIM0 / Descriptions 0 / 0 / X4 free-counting mode 0 / 1 / X2 free-counting mode 1 / 0 / X4 compare-counting mode 1 / 1 / X2 compare-counting mode
0	QEIEN	Input module mode select bit: 0 = Input module performs Input Capture Functions. (Default value). 1 = Input module works as QEI.

PWM 2 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM2.11	PWM2.10	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~4	-	Reserved
3~0	PWM2.11 ~PWM2.8	PWM 2 Register bit 11~8.

PWM 6 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM6.11	PWM6.10	PWM6.9	PWM6.8

Mnemonic: PWM6H Address: D6h

BIT	NAME	FUNCTION

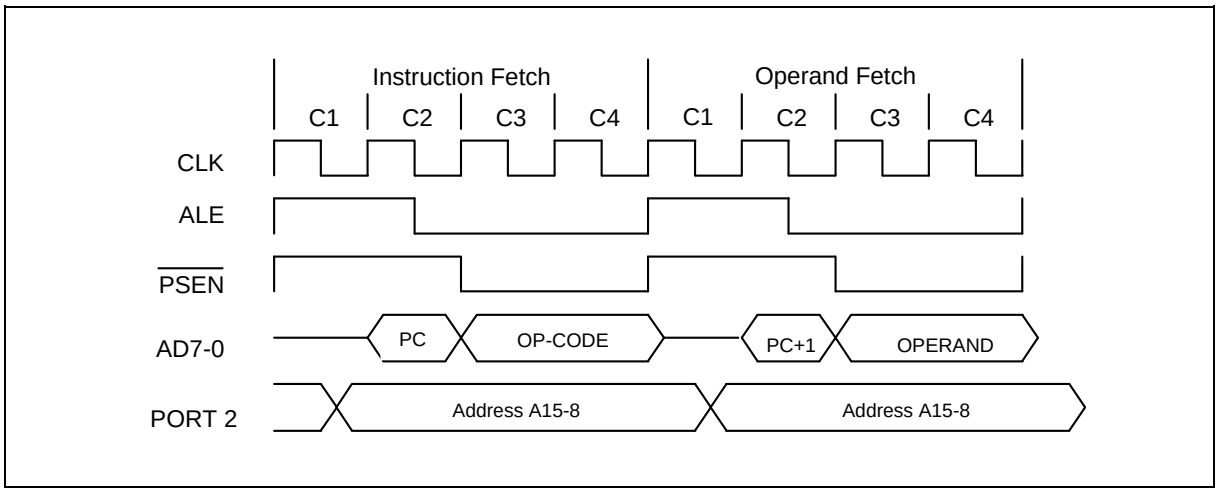


Figure 8-2: Two Cycles Instruction Timing

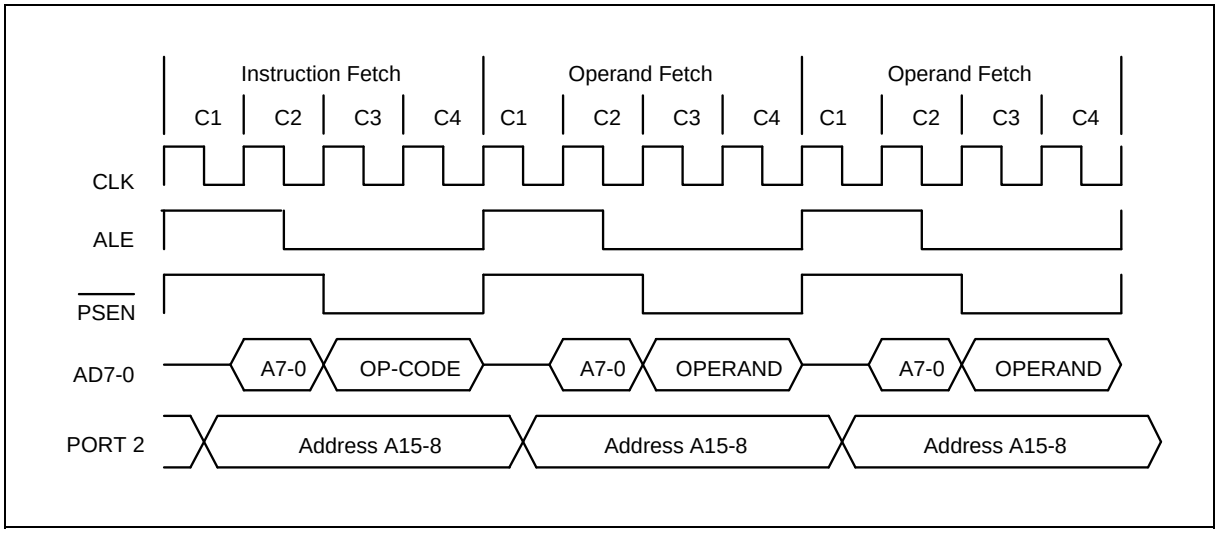


Figure 8-3: Three Cycles Instruction Timing

9. POWER MANAGEMENT

The W79E22X SERIES provides idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections.

9.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer, PWM, ADC and Serial ports blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and $\overline{\text{PSEN}}$ pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the device is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

9.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{\text{PSEN}}$ pins are pulled low (if PWDNH=0). The port pins output the values held by their respective SFRs.

The device will exit the Power Down mode with a reset or by an external interrupt pin enabled (external interrupts 0 and 1). An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The device can be waken up from the Power Down mode by forcing an external interrupt pin activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then either a low-level or a falling-edge at external interrupt pin will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

10.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state and makes Port 0 float (as it does not have on-chip pull-up resistors). The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2 V, the minimum operating voltage for the RAM. If VDD falls below 2 V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depends on the source of the reset. The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is cleared to 0 on a Power-on reset and unaffected by other resets. All the bits in this SFR have unrestricted read access. POR, WDIF, EWT and RWT bits require Timed Access (TA) procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description. Table below lists the different reset values for WDCON due to different sources of reset.

WDCON	Watch-Dog Control	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	x0xx 0000B External reset x0xx 0100B Watchdog reset x1xx 0000B Power on reset

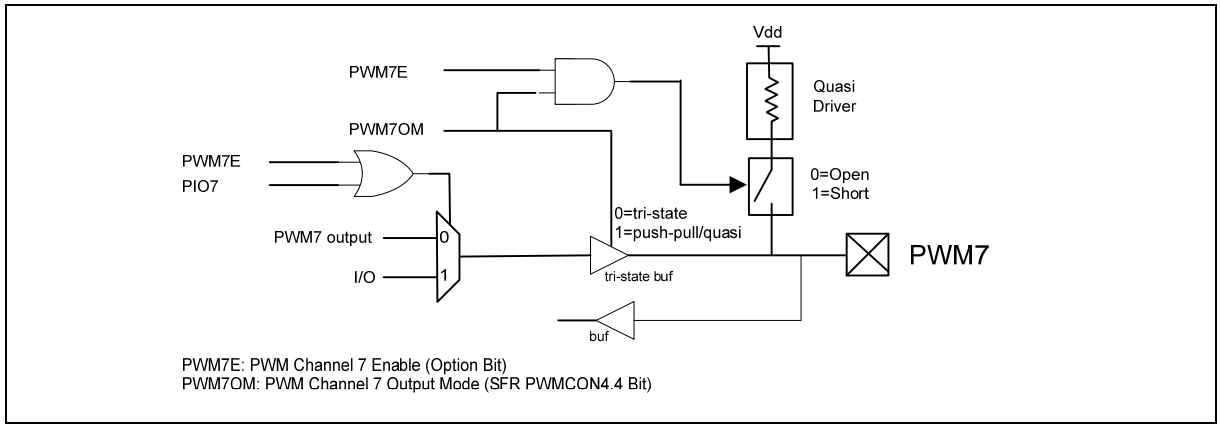


Figure 14-6: PWM7 I/O pin

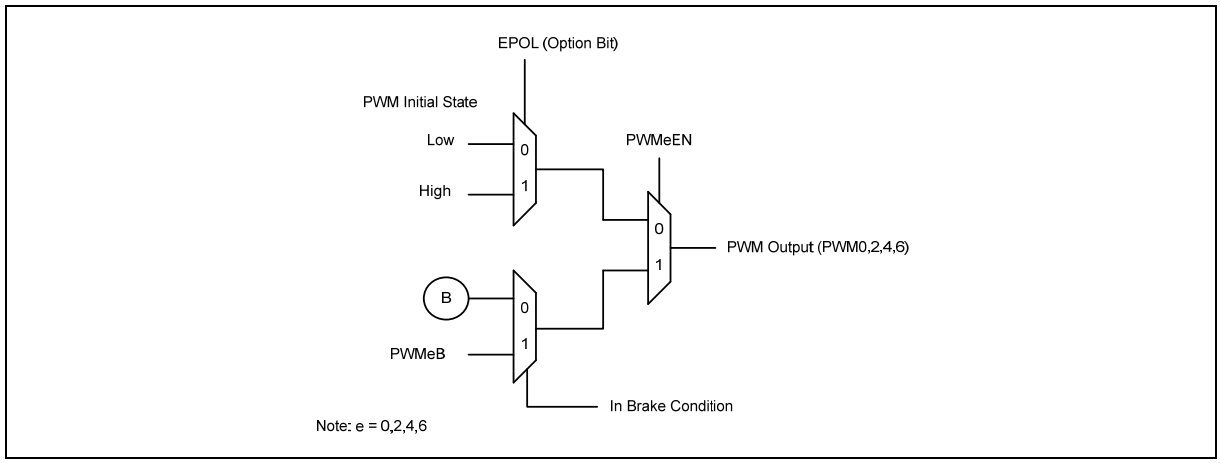


Figure 14-7: Even PWM Output

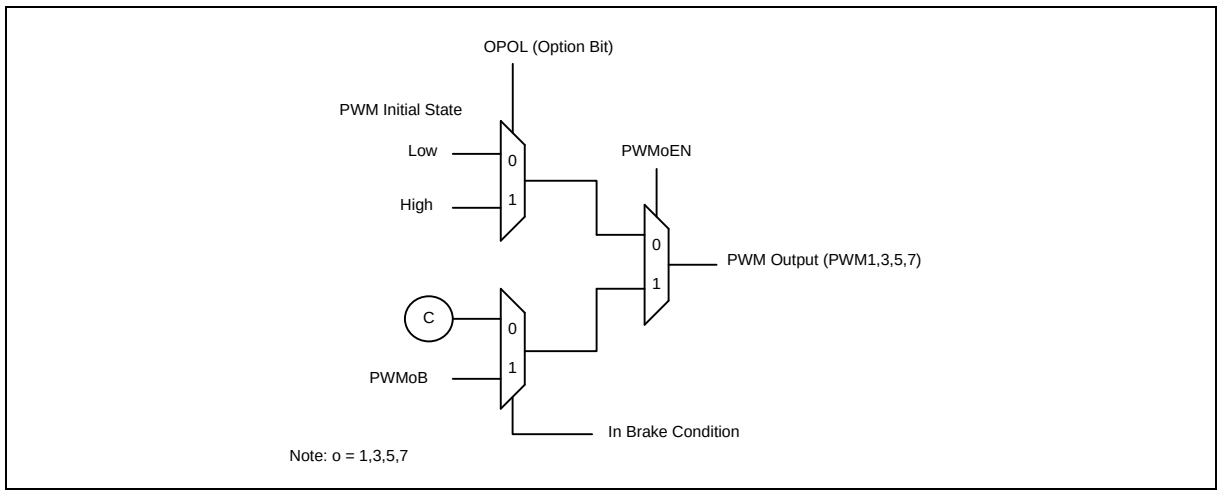


Figure 14-8: Odd PWM Output

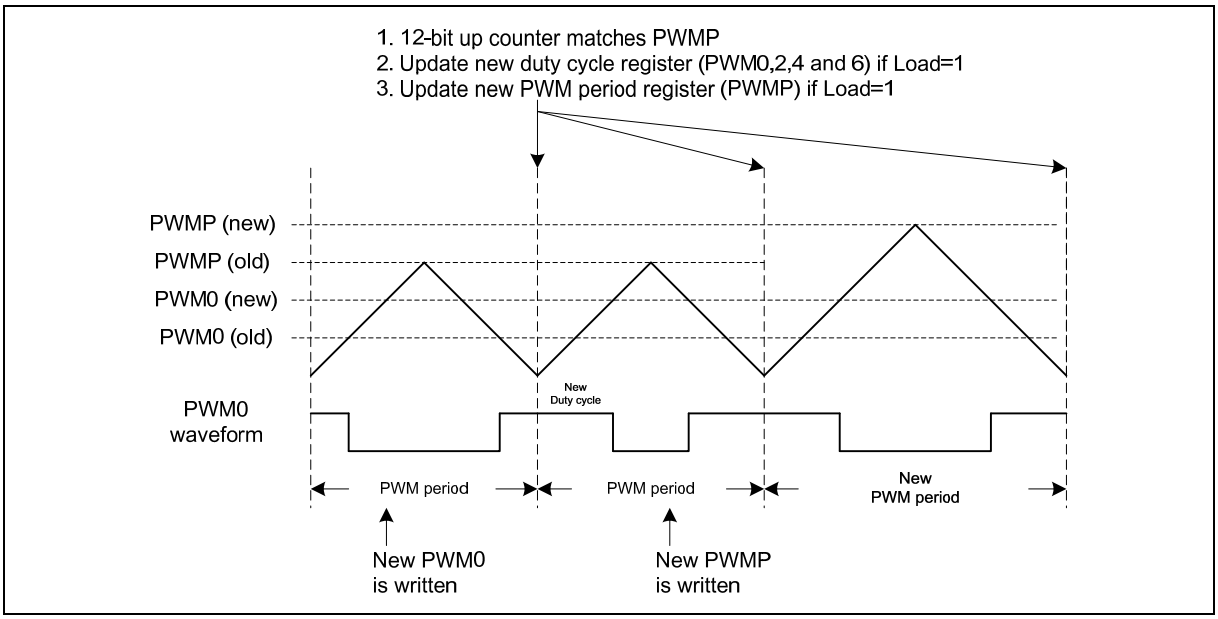


Figure 14-20: Center-Aligned Mode

Center-aligned PWM signals are produced by the module when the PWM time base is configured in an Up/Down Counting mode (see Figure 14-20). The counter will start counting-up from 0 to match the value of PWM0 (old); this will cause the toggling of the PWM0 output to low. The CPU reset states determine the starts value of PWM0 waveform at starts of counter lies on the polarity setting located in the Option bits. At this time the new PWM0 is written to the register. Counter continue to count and match with the PWMP (old). Upon reaching this states counter is configured automatically to down counting and toggle the PWM0 output when counter matches the PWM0 (old) value. Interrupt request when up/down counter underflow. Once the counter reaches 0 it will update the duty cycle register with Load = 1. Up-counting is continues with the matching at PWM0 (new) follow by a low toggle at the PWM0 output. By this time the PWMP buffer is still consist of the PWMP (old) value. A new PWMP is written. So the counter will still matches with this value and continues with down counting and matched the PWM0 (new) and toggle the PWM0 output.

Again updates on the PWM period register is reflected on the 3rd cycle of the diagram by starts counting from 0 to match the PWM0 (new) and toggle at the PWM0 output to low. Counter is continuing up-counting, upon reaching the PWMP (new) it is matched. Then counter is down counting automatically to match at the PWM0 (new) to get a toggle high at PWM0 output.

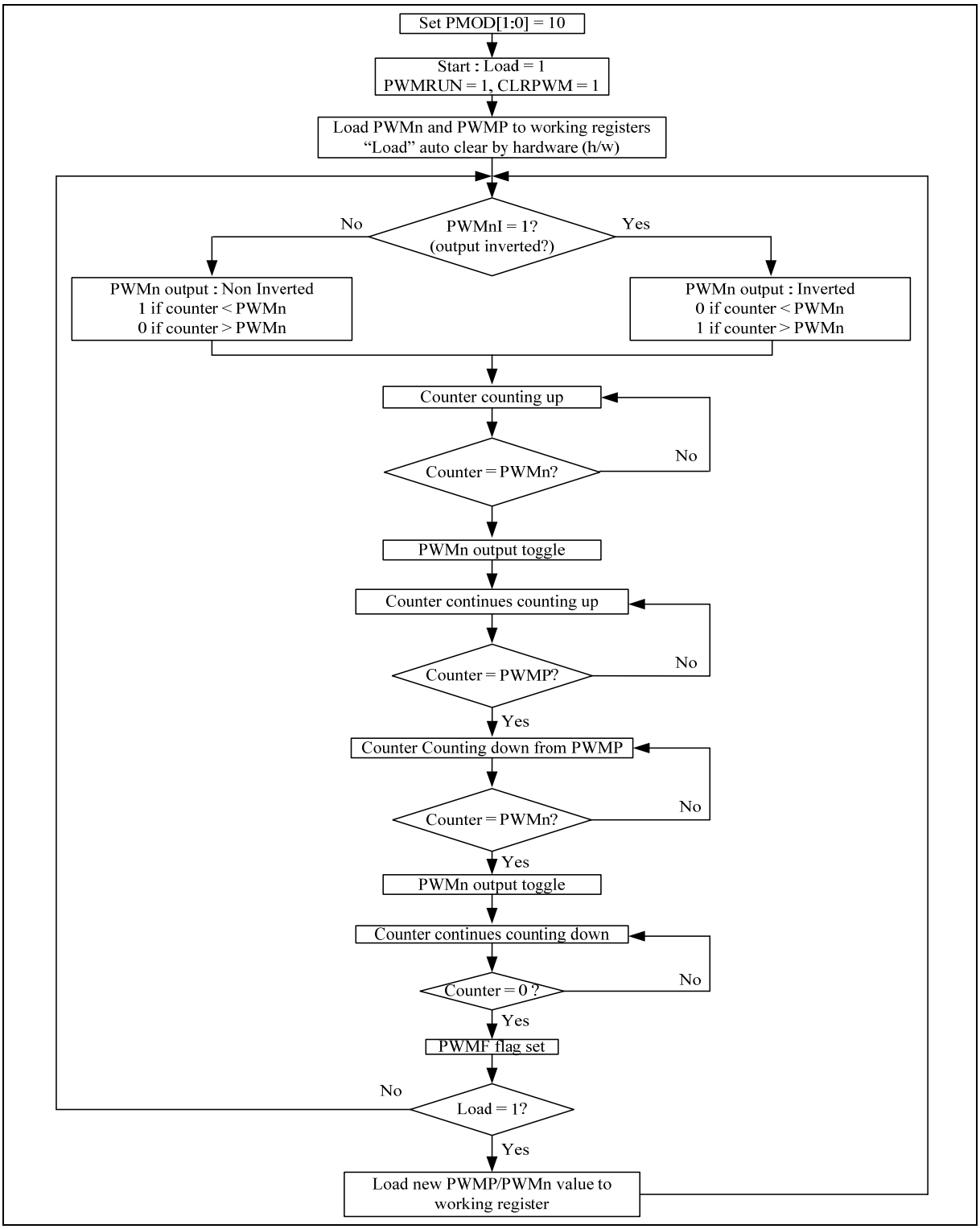


Figure 14-21: Center-aligned Flow Diagram

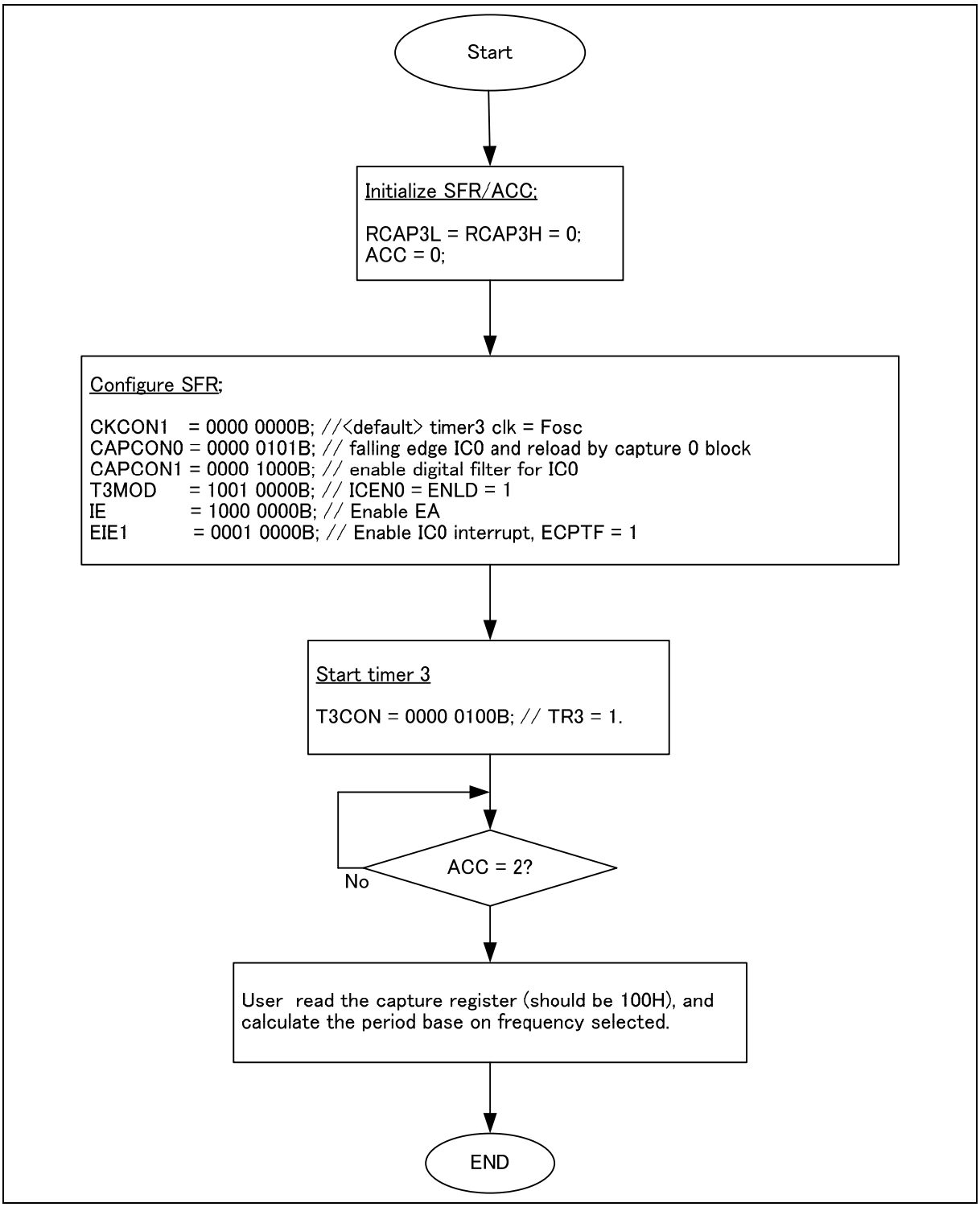


Figure 15-5: Program flow for measurement with IC0 between pulses with falling edge detection (ACC is incremented in interrupt service routine).

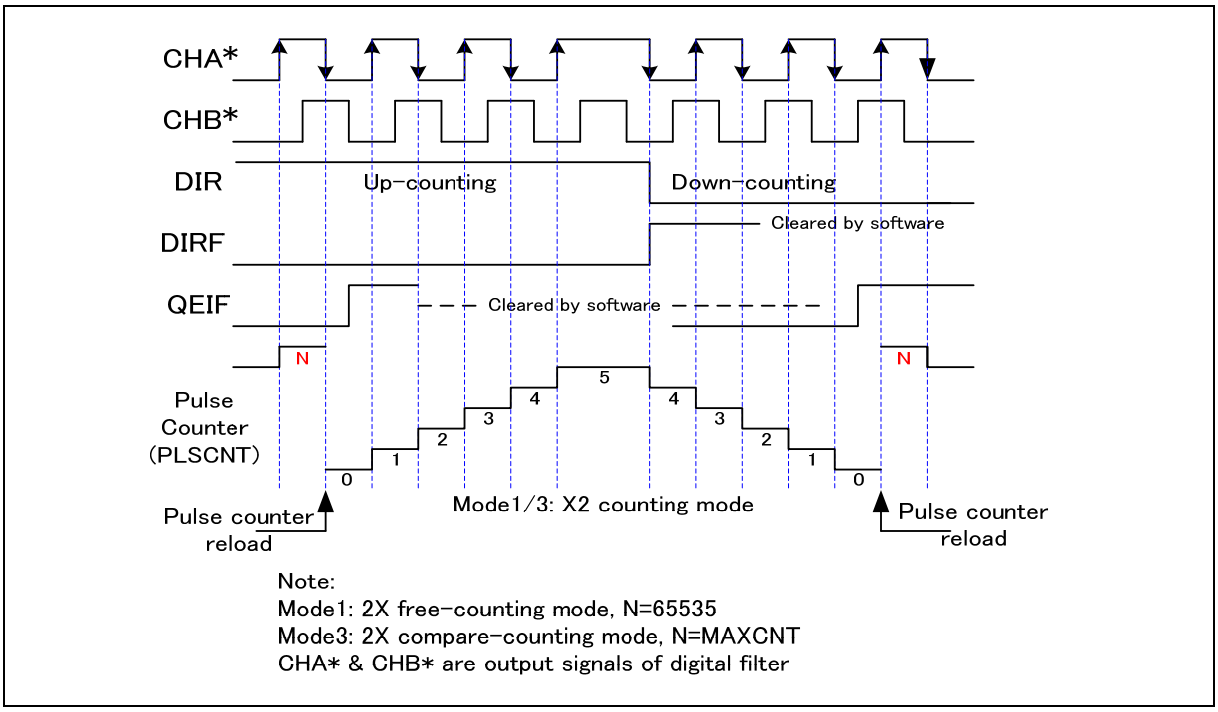


Figure 15-13: X2 Counting Mode

QEI x2 Counting mode is selected by setting the QEI Mode Select bits (QEIM1:QEIM0) to '01b' or '11b'. In this mode, the QEI logic detects every edge on the QEA input only. Every rising and falling edge on the QEA signal clocks the pulse counter.

15.2.5 Up-Counting

Under the forward direction the DIR bit is 1 when up-counting. Software needs to clear the QEIF flag. For the free-counting mode counter will counts until it matches 65535 and next edges on the forward direction will set the QEIF high and reset the PLSCNT to zero. For compare-counting mode counter counts until the MAXCNT value and reload the counter to zero and starts counting up. Changes of direction trigger a down-count and PLSCNT decreasing in counter value. For X2 mode, only CHA edge will set QEIF while for X4 mode both CHA and CHB edges will set QEIF.

15.2.6 Down-Counting

A change of direction will causes the counter to down-count for x2/x4 counting mode. It is indicated with the DIR bit as 0 and DIRF flag is set to 1. At this stage the PLSCNT will starts to down-count from the MAXCNT value for compare-counting mode and while in free-counting mode it will starts to down-count from 65535. The pulse counter will reload with MAXCNT when it down counts to zero in compare-counting mode and sets QEIF to high in the next edge. In free-counting mode the counter will count to 16 bits value before it reload the pulse counter with the value 65535 and set the QEIF high in the next edge. For X2 mode, only CHA edge will set QEIF while for X4 mode both CHA and CHB edges will set QEIF.

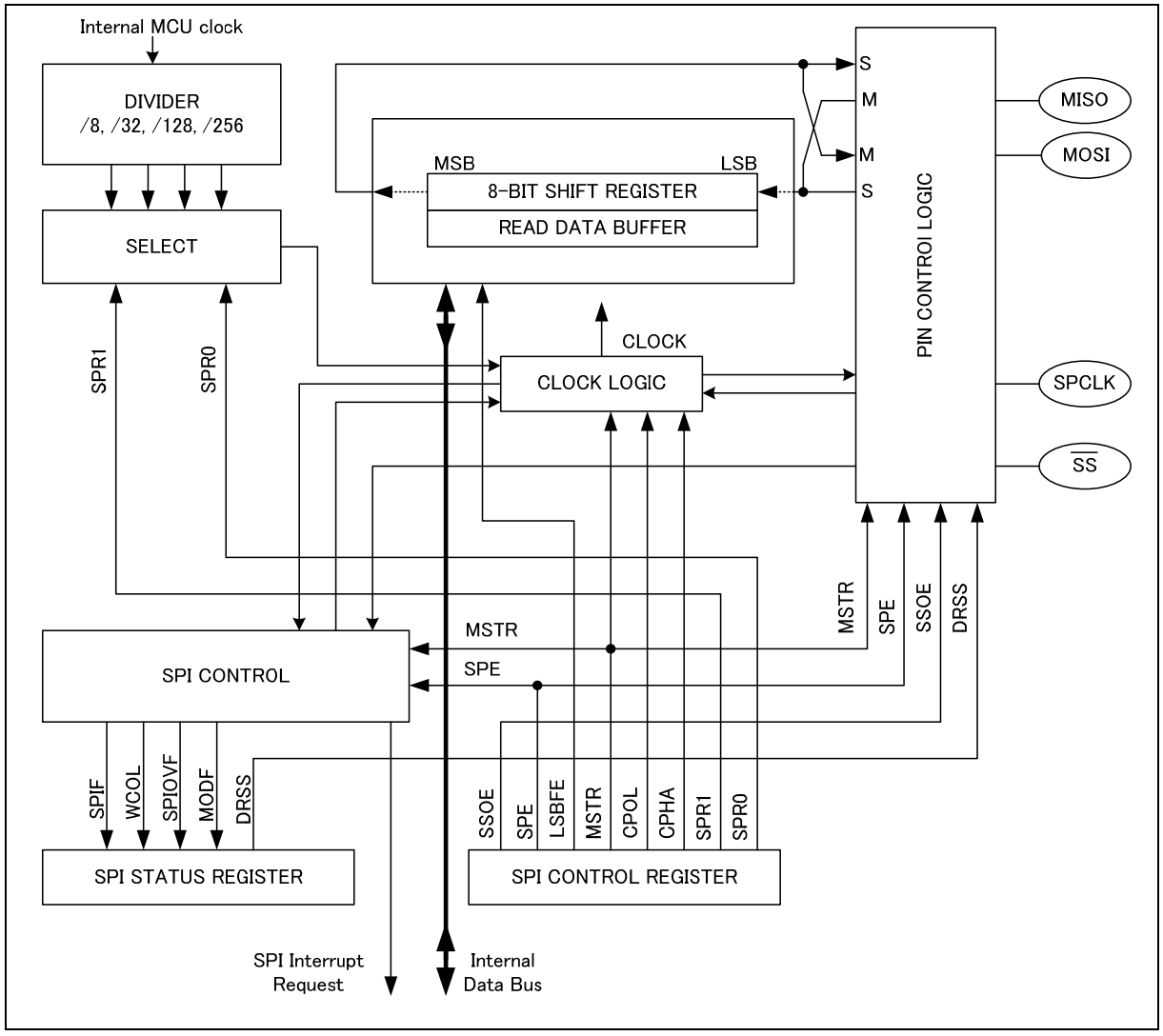


Figure 18-1: SPI block diagram

18.3 Functional descriptions

18.3.1 Master mode

The device can configure the SPI to operate as a master or as a slave, through MSTR bit. When the MSTR bit is set, master mode is selected, when MSTR bit is cleared, slave mode is selected. During master mode, only master SPI device can initiate transmission. A transmission begins by writing to the master SPDR register. The bytes begin shifting out on MOSI pin under the control of SPCLK. The master places data on MOSI line a half-cycle before SPCLK edge that the slave device uses to latch the data bit. The $\overline{SS}$ must stay low before data transactions and stay low for the duration of the transactions.

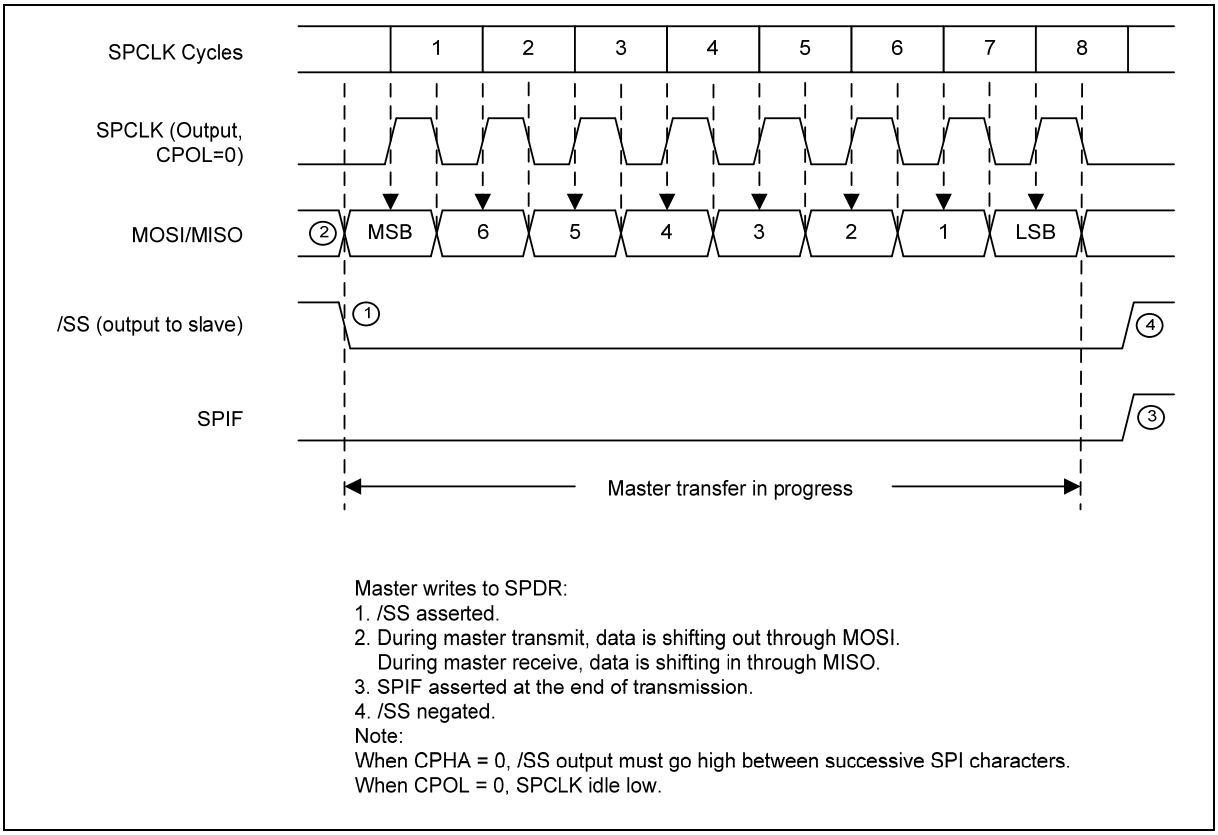


Figure 18-2: Master Mode Transmission (CPOL = 0, CPHA = 0)

DRSS	SSOE	MASTER MODE	SLAVE MODE
0	0	$\overline{SS}$ input (With Mode Fault)	$\overline{SS}$ Input (Not affected by SSOE)
0	1	Reserved	$\overline{SS}$ Input (Not affected by SSOE)
1	0	$\overline{SS}$ General purpose I/O (No Mode Fault)	$\overline{SS}$ Input (Not affected by SSOE)
1	1	$\overline{SS}$ output (No Mode Fault)	$\overline{SS}$ Input (Not affected by SSOE)

During master mode (with SSOE=DRSS= 0), mode fault will be set if $\overline{SS}$ pin is detected low. When mode fault is detected hardware will clear MSTR bit and SPE bit in the meantime it will also generated interrupt request, if ESPI is enabled.

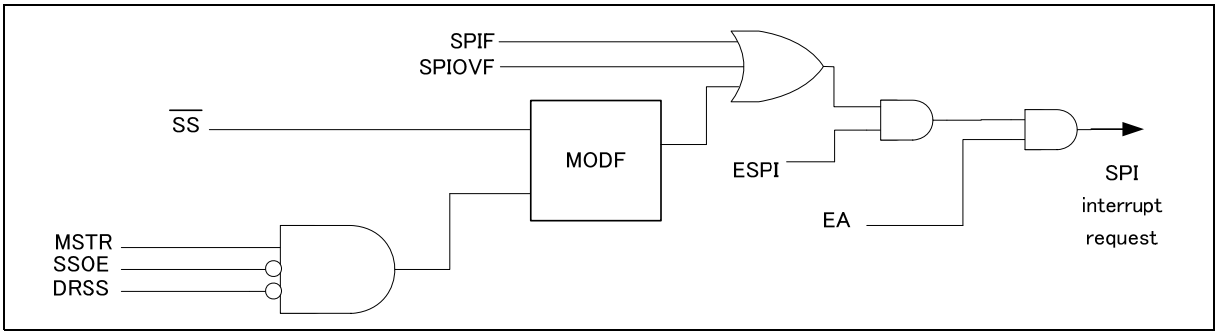


Figure 18-10: SPI interrupt request

18.3.5 SPI I/O pins mode

When SPI is disabled (SPE = 0) the corresponding I/O is following the original setting and act as a normal I/O. In the case of SPI is enabled (SPE = 1) the SPI pins I/O mode follow the below table. For $\overline{SS}$ pin it is always at Quasi-bidirectional mode whether it is configured as master or slave.

	MISO	MOSI	CLK	/SS
Master	Input	Output	Output	Output*: DRSS=0,SSOE=0 Input: DRSS=1, SSOE=1
Slave	Output** during /SS = Low Else Input mode	Input	Input	Input

Input = Quasi-bidirectional mode

Output = Push-pull mode

Output* = this output mode in /SS is Quasi-bidirectional output mode. Master needs to detect mode fault during master outputs /SS low.

Output** = In SLAVE mode, MISO is in output mode only during the time of $\overline{SS}$ =Low, otherwise it must keep in input mode (Quasi-bidirectional).

DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Source Current P2.0~P2.5, P5.0~P5.1 (PUSH-PULL Mode) PWM pins	I_{SR11}	-22	-31	-42	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-6	-9	-13		V_{DD} = 2.7V, V_S = 2.0V
Source Current P1, P2, P3, P4, P5 (Quasi-bidirectional mode)	I_{SR21}	-200	-300	-430	uA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-50	-82	-115		V_{DD} =2.7V, V_S = 2.0V
Sink Current P2.0~P2.5, P5.0~P5.1 (PUSH-PULL Mode)	I_{SK11}	18	22	32	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK12}	10	15	25		V_{DD} = 2.7V, V_S = 0.45V
Sink Current P0,P1,P2, P3,P4,P5 (Quasi-bidirectional mode)	I_{SK21}	4	5	6	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK22}	3	3.5	5		V_{DD} = 2.7V, V_S = 0.45V
Output Low Voltage P2.0~P2.5, P5.0~P5.1 (PUSH-PULL Mode)	V_{OL11}	-	0.35	-	V	V_{DD} = 4.5V, I_{OL} = 20 mA
	V_{OL12}	-	0.07	-		V_{DD} = 2.7V, I_{OL} = 3.2 mA
Output Low Voltage P0, P1, P2, P3, P4, P5 (Quasi-bidirectional Mode)	V_{OL21}	-	0.35	-	V	V_{DD} = 4.5V, I_{OL} = 4.0 mA
	V_{OL22}	-	0.35	-		V_{DD} = 2.7V, I_{OL} = 3.0 mA
Output High Voltage P2.0~P2.5, P5.0~P5.1 (PUSH-PULL Mode)	V_{OH11}	-	3.3	-	V	V_{DD} = 4.5V, I_{OH} = -20mA
	V_{OH12}	-	2.5	-		V_{DD} = 2.7V, I_{OH} =-3.2mA
Output High Voltage P1, P2, P3, P4, P5, P6, P7 (Quasi-bidirectional Mode)	V_{OH21}	-	4.1	-	V	V_{DD} = 4.5V, I_{OH} =-100uA
	V_{OH22}	-	2.52	-		V_{DD} = 2.7V, I_{OH} = -30uA
Sink current [*2] P0, P2, ALE, /PSEN	Isk31	3	5	8	mA	V_{DD}=4.5V, Vs = 0.45V
	Isk32	2.5	3.5	6	mA	V_{DD}=2.7V, Vs = 0.45V
Source current [*2] P0, P2, ALE, /PSEN	Isr31	-6	-7.5	-9	mA	V_{DD}=4.5V, Vs = 2.4V
	Isr32	-1	-2	-3	mA	V_{DD}=2.7V, Vs = 2.0V

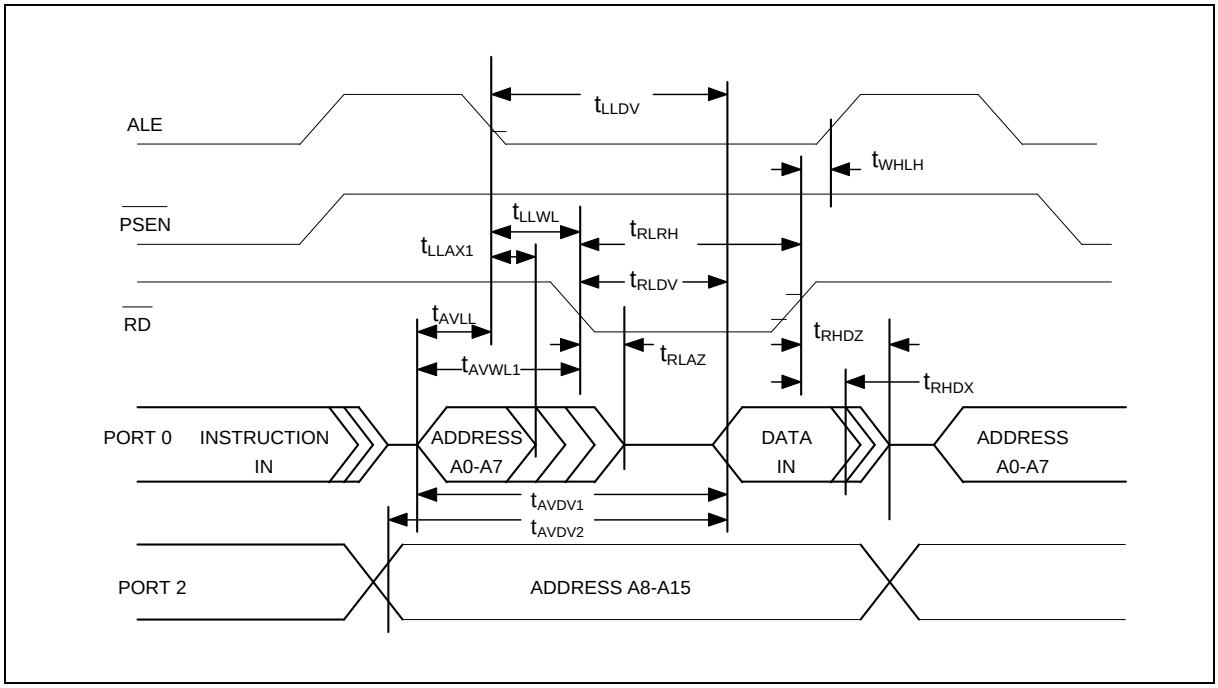
Notes: *1. RST pin is a Schmitt trigger input. RST has internal pull-low resistors about 60kΩ.

*2. P0, P2, ALE and /PSEN are tested in the external access mode.

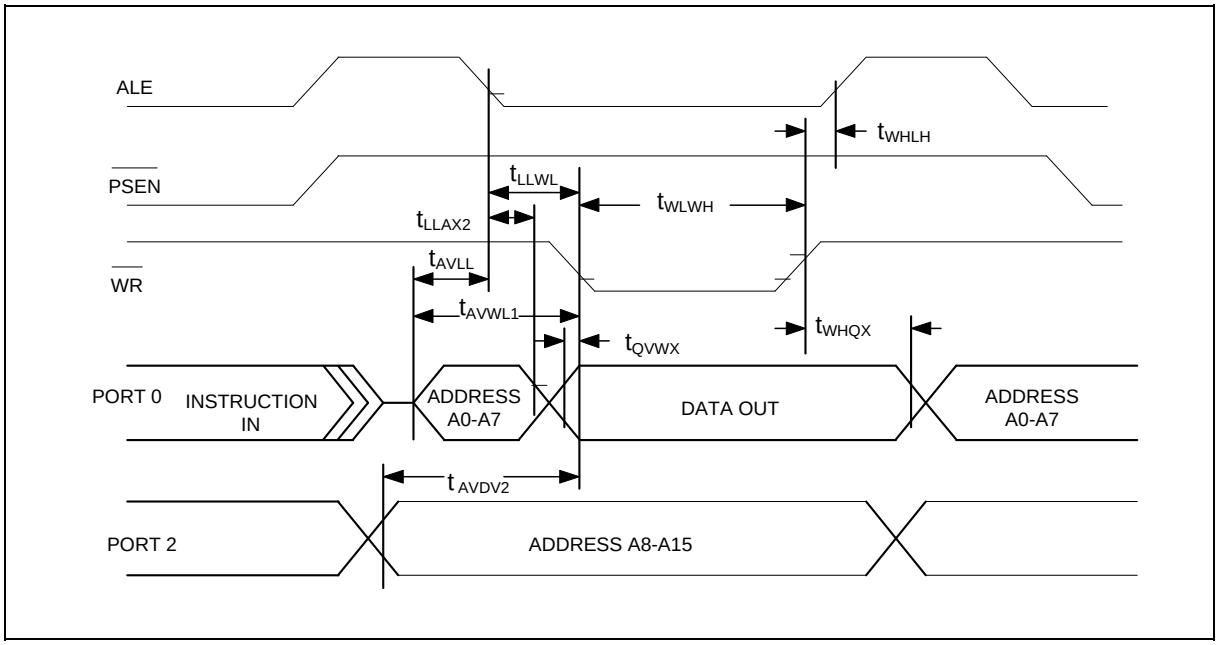
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4, P5 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

24.7 Data Memory Read Cycle

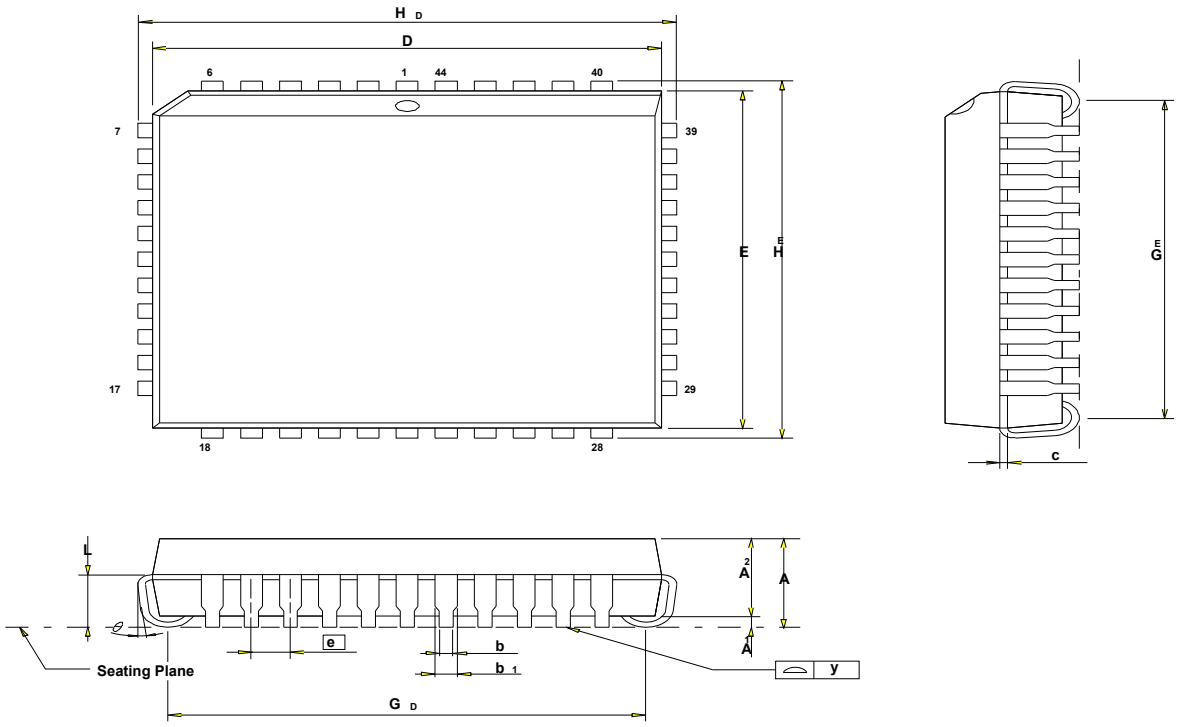


24.8 Data Memory Write Cycle



26. PACKAGE DIMENSION

26.1 44L PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.185	——	——	4.70
A_1	0.020	——	——	0.51	——	——
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	——	——	0.004	——	——	0.10

27. APPLICATION NOTE

In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W79E22X SERIES Flash EPROM microcontroller. In this example, microcontroller will boot from APFlash bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64 KB APFlash. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDFlash bank. The loader program erases the 64 KB APFlash then reads the new code data from external SRAM buffer (or through other interfaces) to update the APFlash.

If the customer uses the reboot mode to update his program, please enable this b3 or b4 of security bits from the writer. Please refer security bits for detail description.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of APFlash program: Program will scan the P1.0. If P1.0 = 0, enters in-system
;* programming mode for updating the content of APFlash code else executes the current ROM code.
;* XTAL = 24 MHz
;*****************************************************************************************************************
.chip 8052
.RAMCHK OFF
.symbols

CHPCON      EQU         9FH
TA          EQU         C7H
SFRAL       EQU         ACH
SFRAH       EQU         ADH
SFRFD       EQU         AEH
SFRCN       EQU         AFH

ORG    0H
LJMP   100H                          ; JUMP TO MAIN PROGRAM
   ;*************************************************************************
   ;*  TIMER0 SERVICE VECTOR ORG = 000BH
   ;*************************************************************************
ORG    00BH
CLR    TR0                           ; TR0 = 0, STOP TIMER0
MOV    TL0, R6
MOV    TH0,R7
RETI
   ;*************************************************************************
   ;*  APFlash MAIN PROGRAM
   ;*************************************************************************
ORG    100H
```