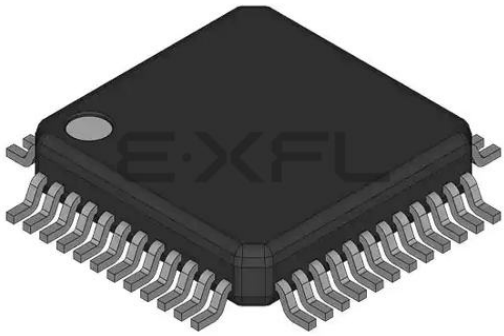

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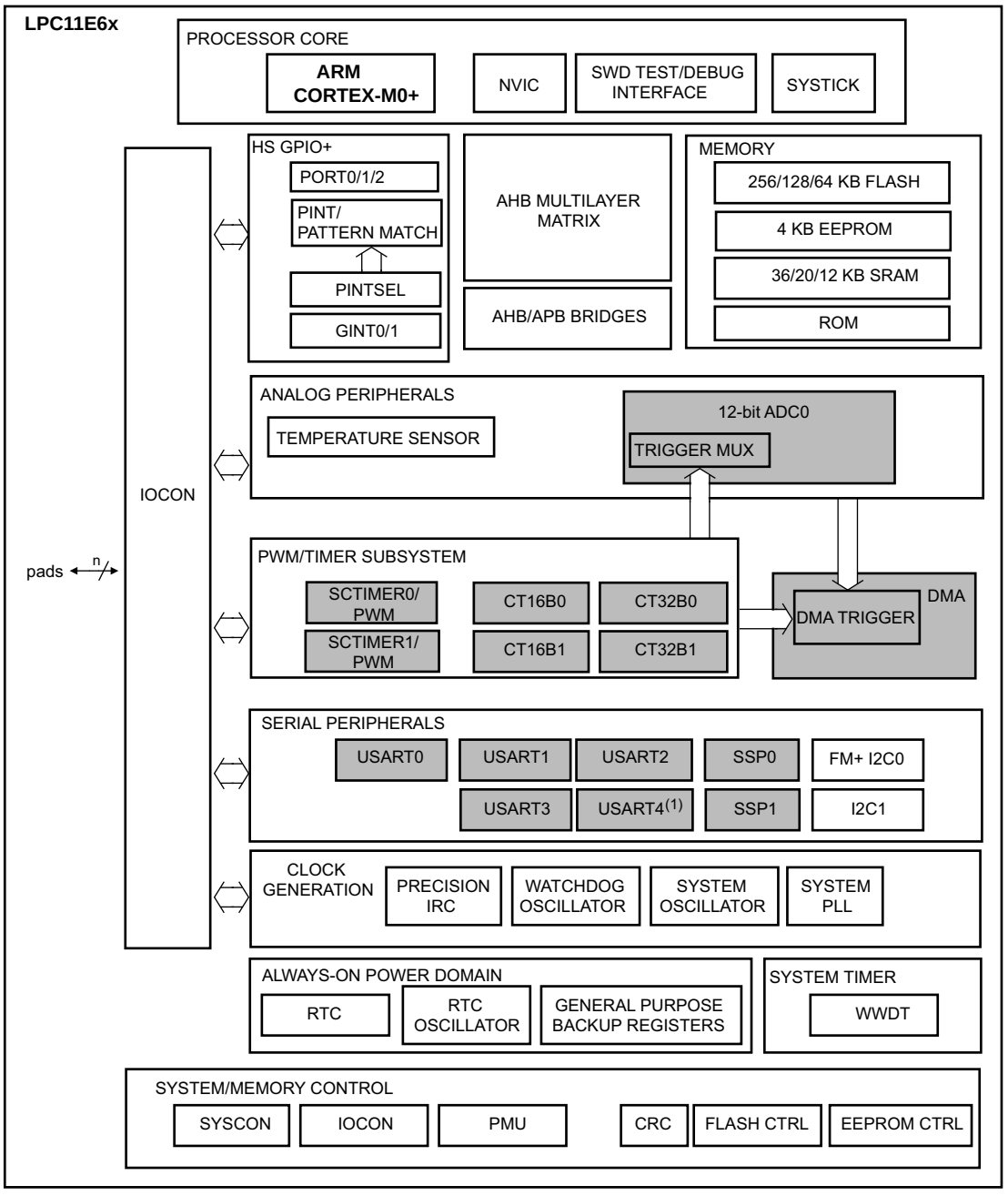
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=lpc11e66jbd48e

6. Block diagram



aaa-011045

Gray-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

(1) Available on LQFP100 packages only.

Fig 3. LPC11E6x block diagram

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO0_7	24	30	45 [5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
					I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART.
					-	**R_5 —** Reserved.
					IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58 [6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
					IO	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R_6 —** Reserved.
PIO0_9	27	38	59 [6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
					IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
					O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60 [6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					IO	**PIO0_10 —** General-purpose digital input/output pin.
					IO	**SSP0_SCK —** Serial clock for SSP0.
					O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64 [3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
					IO	**PIO0_11 —** General-purpose digital input/output pin.
					AI	**ADC_9 —** A/D converter, input channel 9.
					O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66 [3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
					IO	**PIO0_12 —** General-purpose digital input/output pin.
					AI	**ADC_8 —** A/D converter, input channel 8.
					I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
TDO/PIO0_13	32	45	68 [3]	I; PU	IO	**TDO —** Test Data Out for JTAG interface. In boundary scan mode only.
					IO	**PIO0_13 —** General-purpose digital input/output pin.
					AI	**ADC_7 —** A/D converter, input channel 7.
					O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I	**U1_RXD —** Receiver input for USART1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO1_16	-	-	96 [6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
					IO	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R_25 —** Reserved.
PIO1_17	-	-	34 [6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
					I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
					I	**U0_RXD —** Receiver input for USART0.
					-	**R_26 —** Reserved.
PIO1_18	-	-	43 [6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
					I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					O	**U0_TXD —** Transmitter output for USART0.
					-	**R_27 —** Reserved.
PIO1_19	-	64	4 [6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
					O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
					-	**R_28 —** Reserved.
PIO1_20	13	18	29 [6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
					IO	**SSP1_SCK —** Serial clock for SSP1.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56 [6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
					IO	**SSP1_MISO —** Master In Slave Out for SSP1.
					I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80 [3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
					IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
					I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					AI	**ADC_4 —** A/D converter, input channel 4.
					-	**R_29 —** Reserved.
PIO1_23	18	23	35 [6]	I; PU	IO	**PIO1_23 —** General-purpose digital input/output pin.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					IO	**SSP1_SSEL —** Slave select for SSP1.
					O	**U2_TXD —** Transmitter output for USART2.
PIO1_24	22	28	42 [6]	I; PU	IO	**PIO1_24 —** General-purpose digital input/output pin.
					O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
					IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).

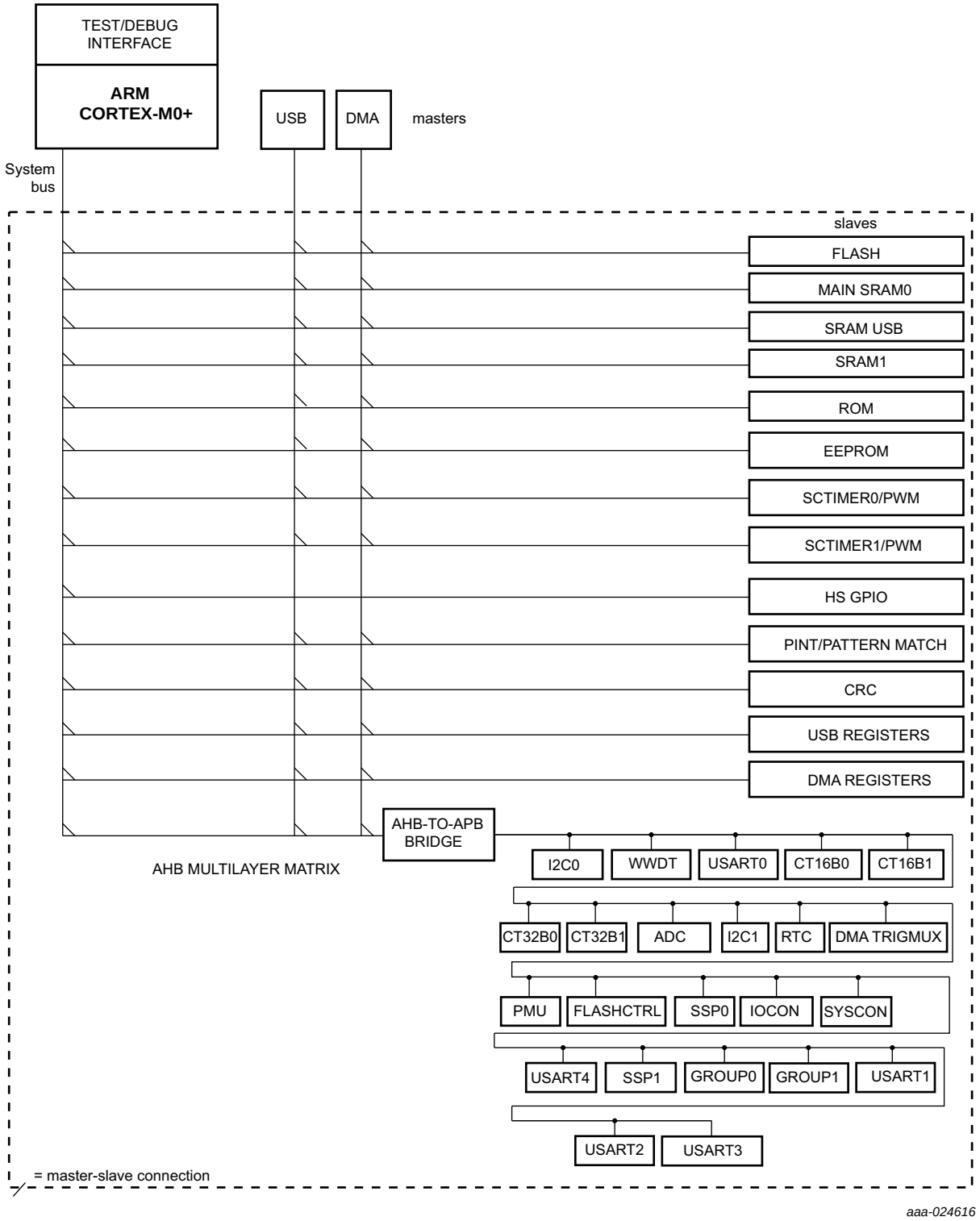


Fig 7. AHB multilayer matrix

8.18.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.18.1.1 Features

- Each SCTimer/PWM supports:
  - 5 match/capture registers.
  - 6 events.
  - 8 states.
  - 4 inputs and 4 outputs.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to four single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.

- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed V_{DDA} voltage level).
- Burst conversion mode for single or multiple inputs.

8.23 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C) for typical samples. The temperature sensor is approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up and after switching the input channels of the ADC, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.24 Clocking and power control

8.24.1 Clock generation

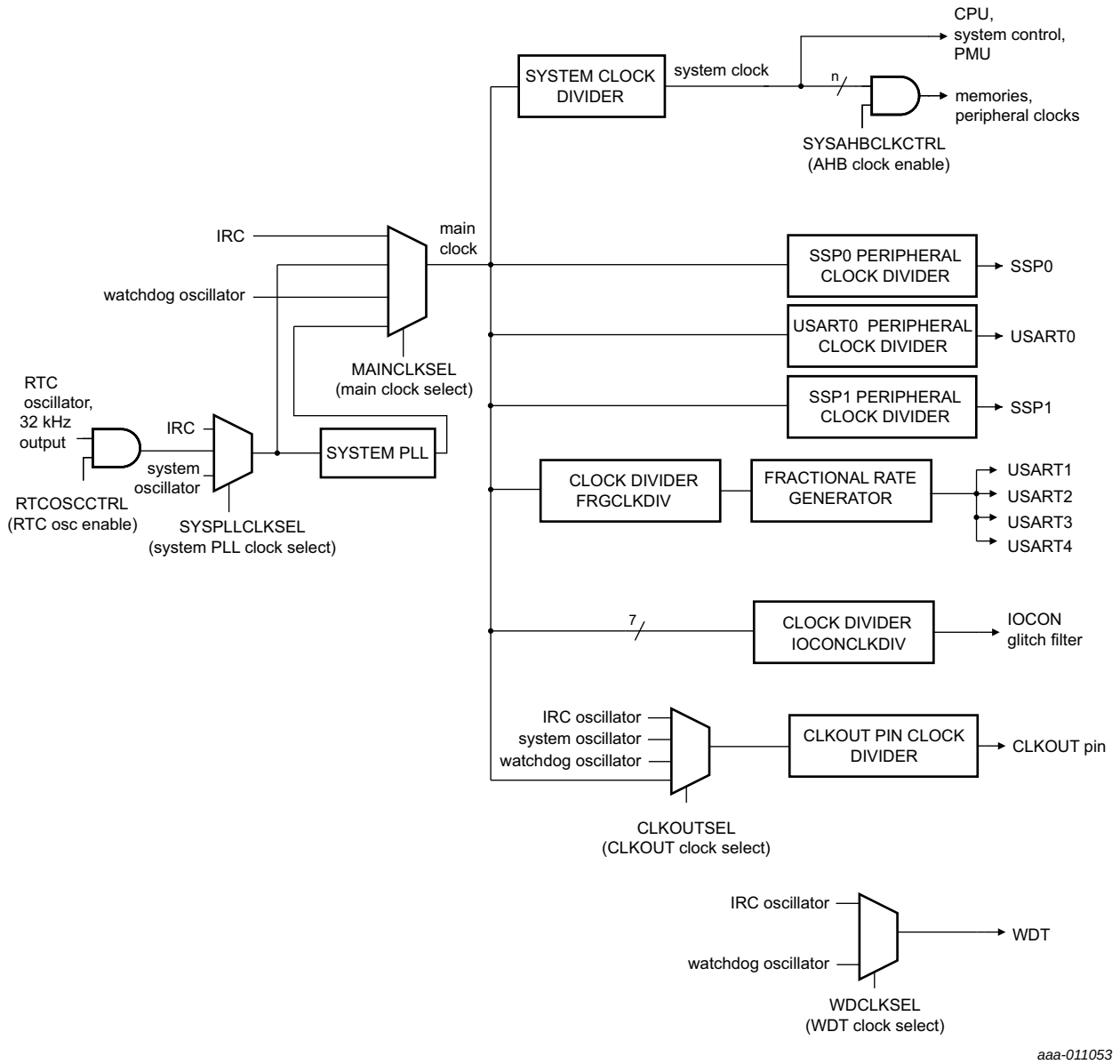


Fig 10. Clock generation

8.24.2 Power domains

The LPC11E6x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is available and $V_{DD} \geq$ VBAT + 0.3 V.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

The system oscillator has a wake-up time of approximately 500 µs.

8.24.3.3 WatchDog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 14).

8.24.3.4 RTC oscillator

The low-power RTC oscillator provides a 1 Hz clock and a 1 kHz clock to the RTC and a 32 kHz clock output that can be used to obtain the main clock (see Figure 10).

8.24.4 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

8.24.5 Clock output

The LPC11E6x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

8.24.6 Wake-up process

The LPC11E6x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

8.24.7 Power control

The LPC11E6x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

The LPC11E6x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Power-down mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.24.7.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the always-on RTC power domain. The LPC11E6x can wake up from Deep power-down mode via the WAKEUP pin or a wake-up signal generated by the RTC interrupt.

The LPC11E6x can be blocked from entering Deep power-down mode by setting a lock bit in the PMU block. Blocking the Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the WAKEUP pin is used in the application, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH while the part is in deep power-down mode. To wake up from deep power-down mode, pull the WAKEUP pin LOW. In addition, pull the RESET pin HIGH to prevent it from floating while in Deep power-down mode.

8.25 System control

8.25.1 Reset

Reset has four sources on the LPC11E6x: the RESET pin, the WatchDog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The RESET pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values. The internal reset status is reflected on the RSTOUT pin.

In Deep power-down mode, an external pull-up resistor is required on the RESET pin.

The RESET pin is operational in active, sleep, deep-sleep, and power-down modes if the RESET function is selected in the IOCON register for pin PIO0_0 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and also wakes up the part if in sleep, deep-sleep or power-down mode. The RESET pin is not functional in Deep power-down mode.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x/Ex user manual*.

8.26 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11E6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[16]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[16]	−10	−50	−85	μA
		$V_{DD} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[17]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN	[19]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT	[19]	−0.5	-	3.6	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[20]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	[20]	-	-	2.5	pF
		pins with digital functions only	[20]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

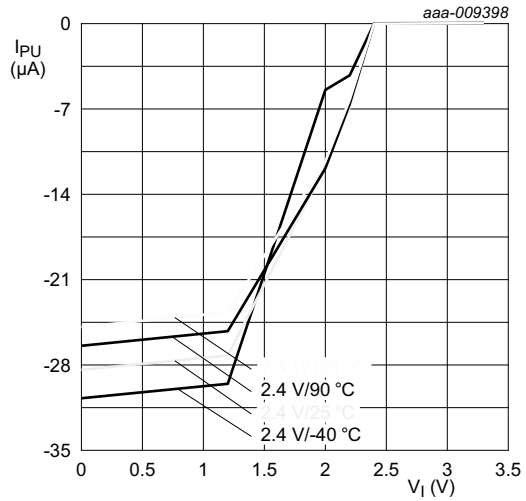
[12] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[13] Including voltage on outputs in tri-state mode.

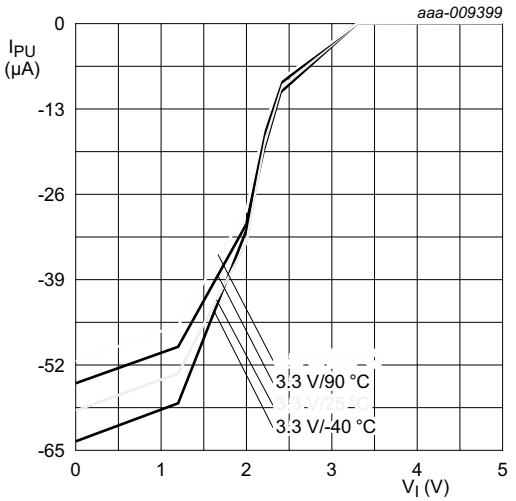
[14] Tri-state outputs go into tri-state mode in Deep power-down mode.

Table 9. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
WWDT	-	0.05	0.17	Main clock selected as clock source for the WDT.
I2C0	-	0.05	0.22	-
I2C1	-	0.05	0.18	-
SSP0	-	0.15	0.59	-
SSP1	-	0.15	0.58	-
USART0	-	0.31	1.19	-
USART1	-	0.12	0.50	-
USART2	-	0.13	0.49	-
USART3 + USART4	-	0.21	0.81	-
ADC0	-	2.15	2.68	Register interface disabled in SYSAHBCLKCTRL and analog block disabled in PDRUNCFG registers. Power consumption measured while the ADC is sampling a single channel with an ADC clock of 12 MHz or 48 MHz.
Temperature sensor	0.18	-	-	-
DMA	-	0.28	1.1	-
CRC	-	0.04	0.14	-

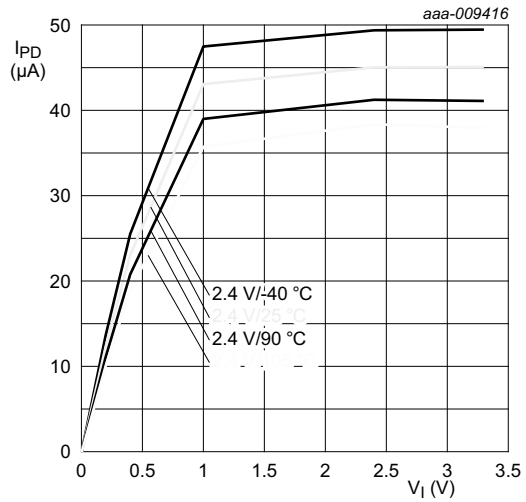


Conditions: V_{DD} = 2.4 V; standard port pins.

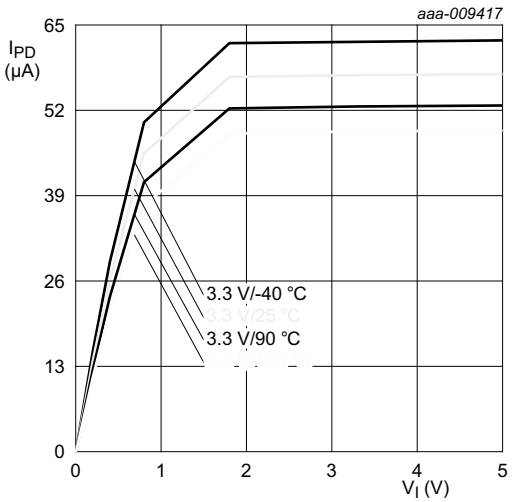


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 2.4 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

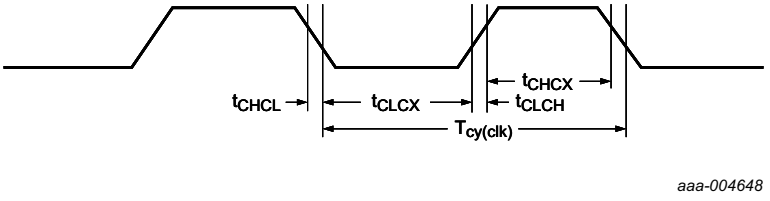


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

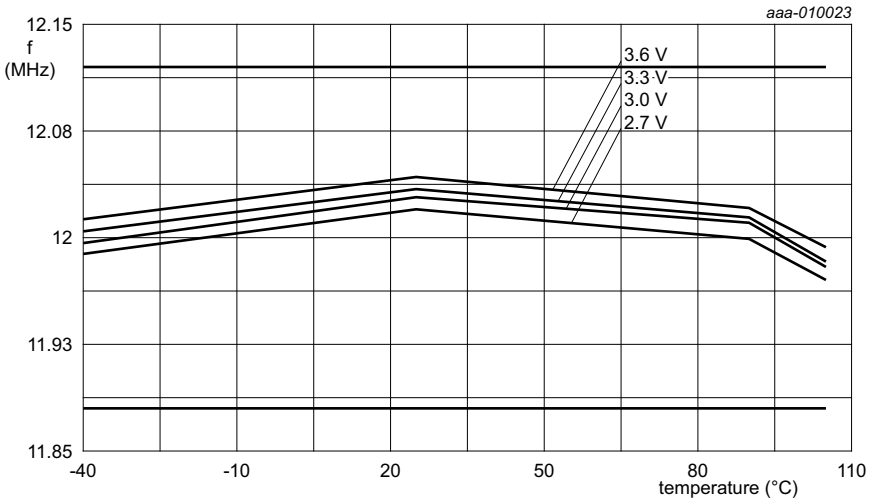
Table 13. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1 %	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2 %	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 30. Typical Internal RC oscillator frequency versus temperature

12.6 SSP interface

Table 17. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40$ °C to 105 °C; 2.4 V ≤ V_{DD} ≤ 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

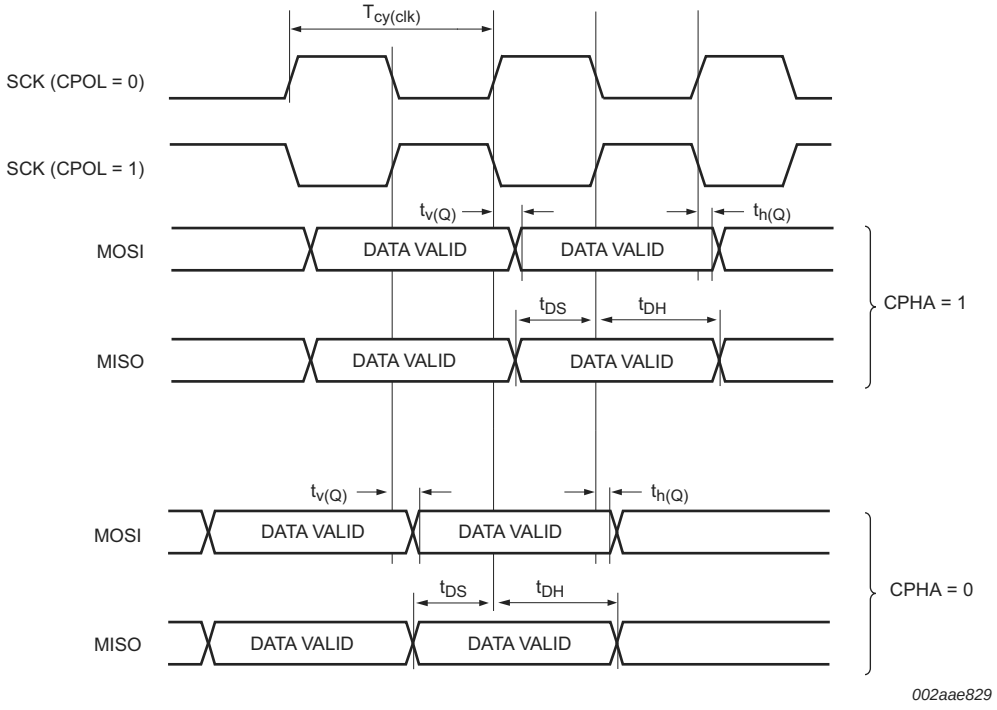


Fig 32. SSP master timing in SPI mode

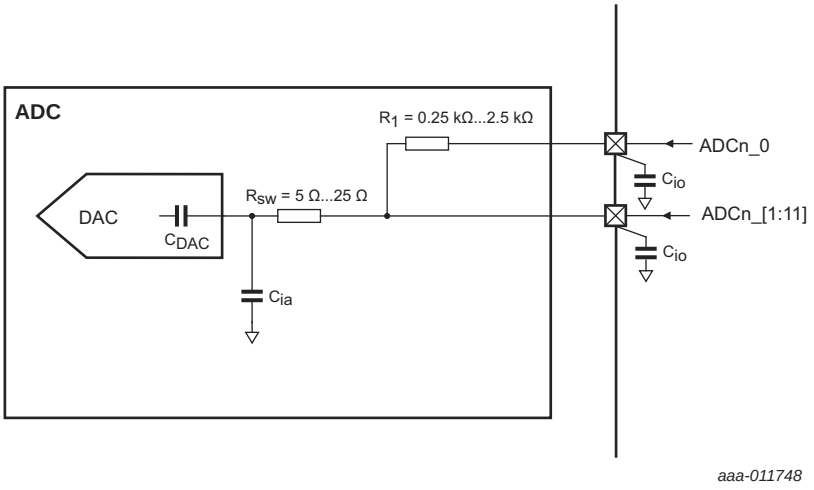


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C		-	−2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105 °C		-	606	-	mV

[3] WatchDog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake up the device from the low-power modes and when a GPIO output pin is set in the reset handler.

14.3 XTAL input and crystal oscillator component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

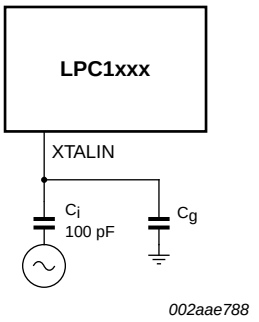
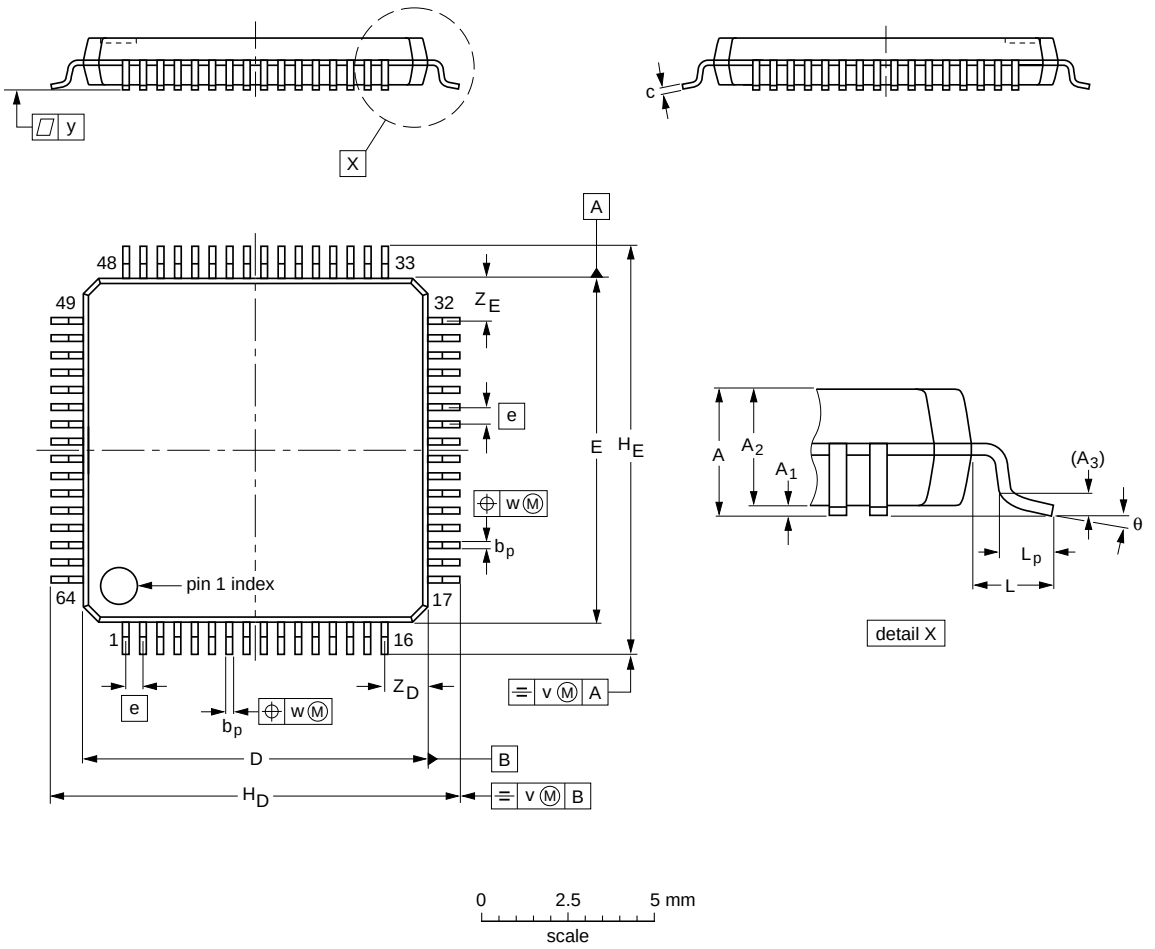


Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled through a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 39 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 39 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 43. Package outline LQFP64 (SOT314-2)

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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