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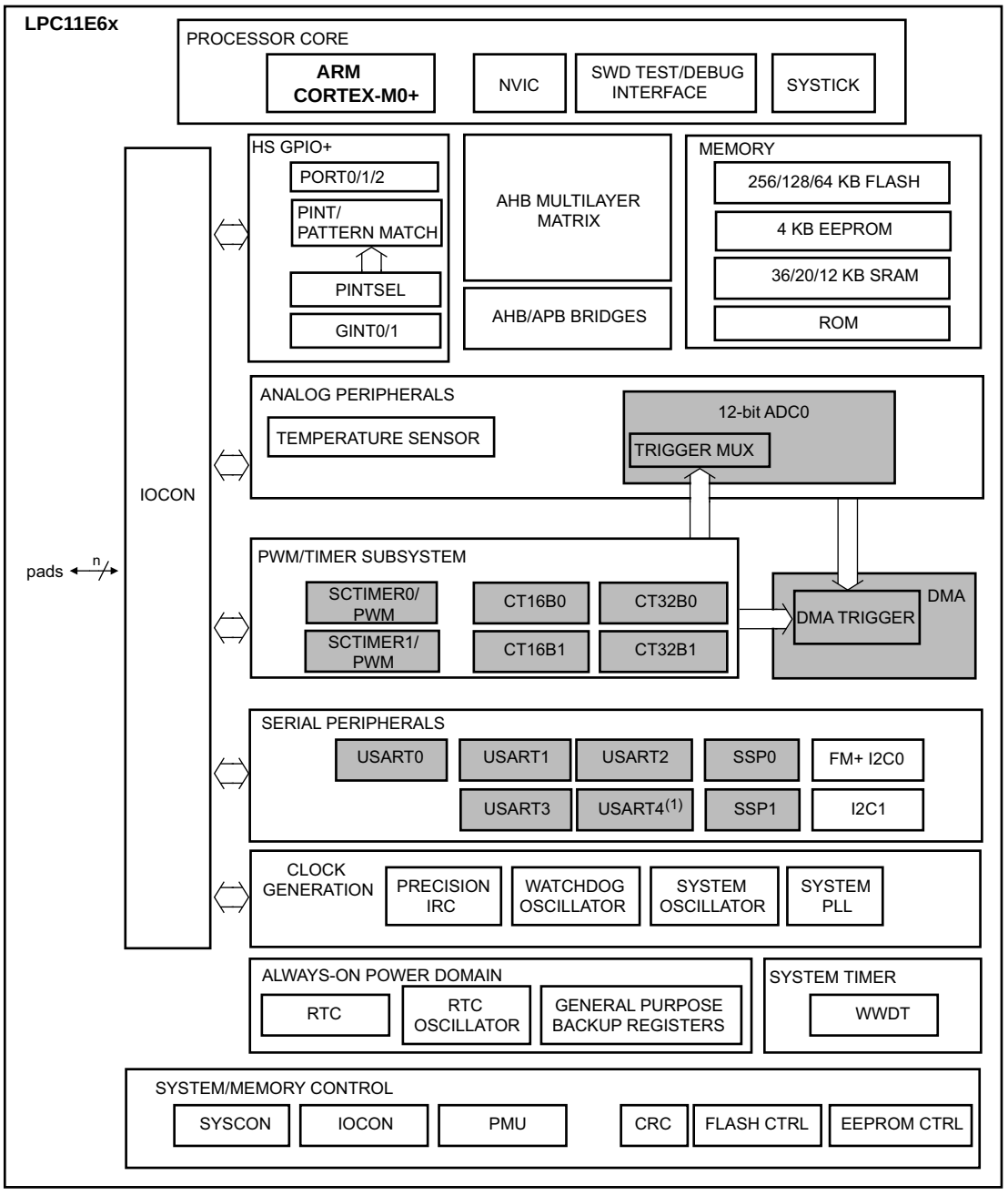
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11e67jbd100e

6. Block diagram



aaa-011045

Gray-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

(1) Available on LQFP100 packages only.

Fig 3. LPC11E6x block diagram

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
$\overline{\text{TRST}}$/PIO0_14	33	46	69	[3]	I; PU	IO	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. In boundary scan mode only.
						IO	**PIO0_14 —** General-purpose digital input/output pin.
						AI	**ADC_6 —** A/D converter, input channel 6.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						O	**U1_TXD —** Transmitter output for USART1.
SWDIO/PIO0_15	37	50	81	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						IO	**PIO0_15 —** General-purpose digital input/output pin.
						AI	**ADC_3 —** A/D converter, input channel 3.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/WAKEUP	38	51	82	[4]	I; PU	IO	**PIO0_16 —** General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
						I	**ADC_2 —** A/D converter, input channel 2.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_8 —** Reserved.
PIO0_17	42	56	90	[6]	I; PU	IO	**PIO0_17 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART0 in synchronous mode.
PIO0_18	45	60	94	[6]	I; PU	IO	**PIO0_18 —** General-purpose digital input/output pin.
						I	**U0_RXD —** Receiver input for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19	46	61	95	[6]	I; PU	IO	**PIO0_19 —** General-purpose digital input/output pin.
						O	**U0_TXD —** Transmitter output for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20	10	12	17	[6]	I; PU	IO	**PIO0_20 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
						I	**U2_RXD —** Receiver input for USART2.
PIO0_21	17	22	33	[6]	I; PU	IO	**PIO0_21 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO1_16	-	-	96 [6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
					IO	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R_25 —** Reserved.
PIO1_17	-	-	34 [6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
					I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
					I	**U0_RXD —** Receiver input for USART0.
					-	**R_26 —** Reserved.
PIO1_18	-	-	43 [6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
					I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					O	**U0_TXD —** Transmitter output for USART0.
					-	**R_27 —** Reserved.
PIO1_19	-	64	4 [6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
					O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
					-	**R_28 —** Reserved.
PIO1_20	13	18	29 [6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
					IO	**SSP1_SCK —** Serial clock for SSP1.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56 [6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
					IO	**SSP1_MISO —** Master In Slave Out for SSP1.
					I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80 [3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
					IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
					I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					AI	**ADC_4 —** A/D converter, input channel 4.
					-	**R_29 —** Reserved.
PIO1_23	18	23	35 [6]	I; PU	IO	**PIO1_23 —** General-purpose digital input/output pin.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					IO	**SSP1_SSEL —** Slave select for SSP1.
					O	**U2_TXD —** Transmitter output for USART2.
PIO1_24	22	28	42 [6]	I; PU	IO	**PIO1_24 —** General-purpose digital input/output pin.
					O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
					IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO2_15	-	32	49 [6]	I; PU	IO	**PIO2_15 —** General-purpose digital input/output pin.
					I	**SCT1_IN3 —** SCTimer1/PWM input 3.
PIO2_16	-	-	50 [6]	I; PU	IO	**PIO2_16 —** General-purpose digital input/output pin.
					O	**SCT1_OUT0 —** SCTimer1/PWM output 0.
PIO2_17	-	-	51 [6]	I; PU	IO	**PIO2_17 —** General-purpose digital input/output pin.
					O	**SCT1_OUT1 —** SCTimer1/PWM output 1.
PIO2_18	-	33	52 [6]	I; PU	IO	**PIO2_18 —** General-purpose port 2 input/output 18.
					O	**SCT1_OUT2 —** SCTimer1/PWM output 2.
PIO2_19	-	36	57 [6]	I; PU	IO	**PIO2_19 —** General-purpose port 2 input/output 19.
					O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO2_20	-	-	75 [6]	I; PU	IO	**PIO2_20 —** General-purpose port 2 input/output 20.
PIO2_21	-	-	76 [6]	I; PU	IO	**PIO2_21 —** General-purpose port 2 input/output 21.
PIO2_22	-	-	77 [6]	I; PU	IO	**PIO2_22 —** General-purpose port 2 input/output 22.
PIO2_23	-	-	1 [6]	I; PU	IO	**PIO2_23 —** General-purpose port 2 input/output 23.
$\overline{\text{RSTOUT}}$	-	-	88 [6]	IA	IO	Internal reset status output.
RTCXIN	48	1	5 [2]	-	-	RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	1	2	6 [2]	-	-	RTC oscillator output.
VREFP	34	47	73	-	-	ADC positive reference voltage. If the ADC is not used, tie VREFP to V_{DD}.
VREFN	35	48	74	-	-	ADC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.
V_{DDA}	40	53	84	-	-	Analog voltage supply. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	44, 8	58, 10, 34, 59	92, 14, 71, 54, 93	-	-	Supply voltage to the internal regulator and the external rail.
VBAT	47	63	99	-	-	Battery supply. Supplies power to the RTC. If no battery is used, tie VBAT to VDD.
V_{SSA}	41	54	85	-	-	Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	43, 2, 5	57, 3, 7	91, 7, 11, 53, 70	-	-	Ground.
n.c.	-	-	39			Not connected.
n.c.	-	-	38			Not connected.

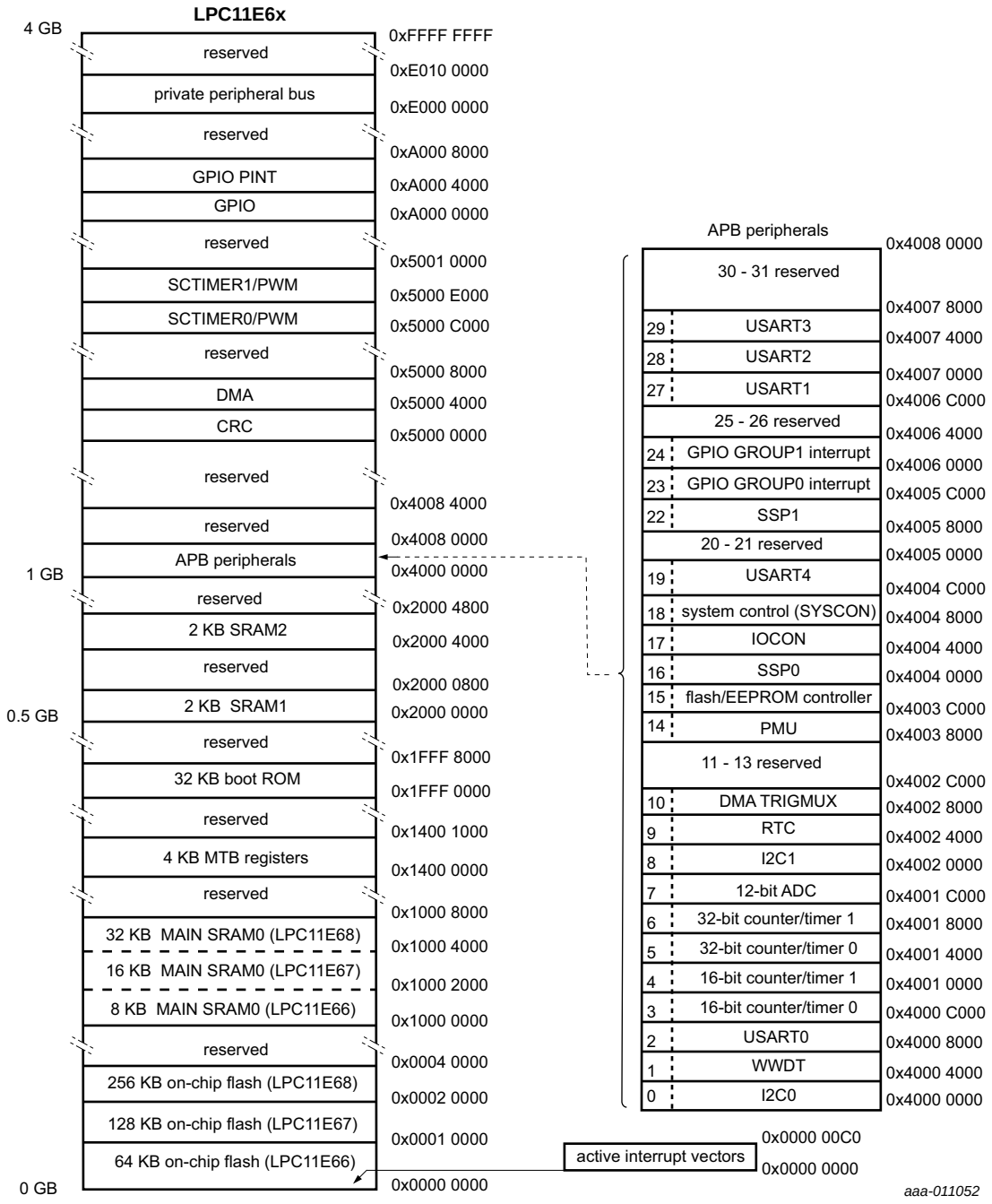


Fig 8. LPC11E6x Memory map

8.8 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.8.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11E6x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts. The following peripheral interrupts are ORed to contribute to one interrupt in the NVIC:
  - USART1, USART4
  - USART2, USART3
  - SCTimer0/PWM, SCTimer1/PWM
  - BOD, WWDT
  - ADC end-of-sequence A interrupt, threshold crossing interrupt
  - ADC end-of-sequence B interrupt, overrun interrupt
  - Flash, EEPROM
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

8.8.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.9 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt.

Enabling an analog function disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.9.1 Features

- Programmable pin function.
- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on pins PIO0_22, PIO0_23, PIO0_11 to PIO0_16, PIO1_3, PIO1_9, PIO1_22, and PIO1_29. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

LPC11E6x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 25 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin except pins PIO2_8 and PIO2_23 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to generate an RXEV notification to the ARM CPU as well.
  - The pattern match engine does not facilitate wake-up.

Table 4. PWM resources

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT16B0	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	4
2	2	2	CT16B1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	3
3	3	3	CT32B0	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	4
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.20.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDOsc). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

8.21 Real-Time Clock (RTC)

The RTC resides in a separate always-on voltage domain with battery back-up. The RTC uses an independent oscillator, also located in the always-on voltage domain.

8.21.1 Features

- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low-power modes, including Deep power-down.

8.22 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the counter/timer match outputs and capture inputs and the ARM TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

8.22.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 2 MSamples/s.
- Temperature sensor voltage output selectable as internal voltage source for channel 0.
- Two configurable conversion sequences with independent triggers.

consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.24.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11E6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

8.24.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

8.24.7.3 Deep-sleep mode

In Deep-sleep mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11E6x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Deep-sleep mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Deep-sleep mode saves power and allows for short wake-up times.

8.24.7.4 Power-down mode

In Power-down mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition, all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

Table 8. Static characteristics *…continued*

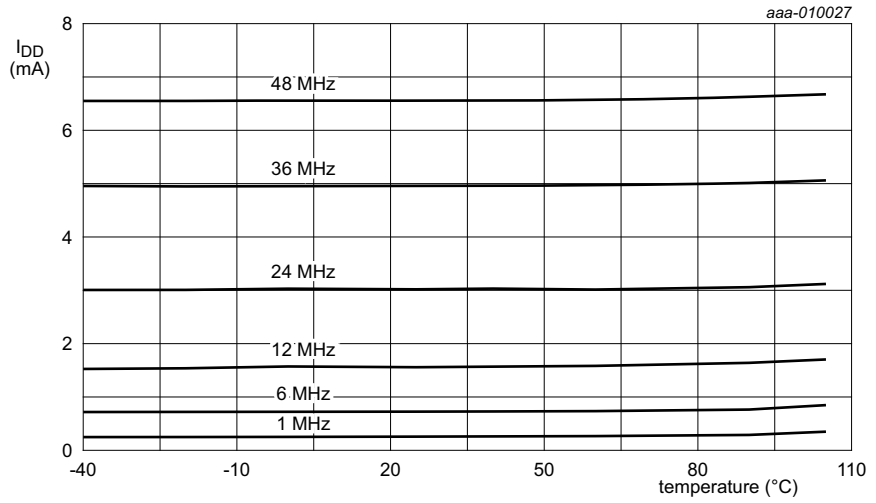
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	Sleep mode;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.2	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	0.8	-	mA
		system clock = 50 MHz; default mode; V_{DD} = 3.3 V	[2][3][9][6][7]	-	3.3	-	mA
		system clock = 50 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][9][6][7]	-	2.8	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][3][10]	-	275	350	μA
		T_{amb} = 105 °C		-	-	640	μA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[2][3][10]	-	5	22	μA
		T_{amb} = 105 °C		-	-	130	μA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; VBAT = 0 or VBAT = 3.0 V RTC oscillator running T_{amb} = 25 °C	[2][11]	-	1.2	5	μA
		T_{amb} = 105 °C		-	-	14	
		RTC oscillator input grounded	[2][11]	-	550	-	nA
I_{BAT}	battery supply current	Deep power-down mode; V_{DD} = V_{DDA} = 3.3 V; VBAT = 3.0 V; RTC oscillator running		-	0	-	-
		RTC off		-	0	-	-
I_{BAT}	battery supply current	V_{DD} = V_{DDA} = 0 V; VBAT = 3.0 V RTC oscillator running		-	1.2	-	μA
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq$ 2.4 V; 5 V tolerant pins	[13][14]	0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V;		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.4 V ≤ V_{DD} ≤ 3.6 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
High-drive output pins configured as digital pin (PIO0_7 and PIO1_31); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	V_{DD} ≥ 2.4 V	[13] [14]	0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 12 mA; 2.4 V ≤ V_{DD} < 2.5 V		V_{DD} − 0.4	-	-	V
		I_{OH} = 20 mA; 2.5 V ≤ V_{DD} < 3.6 V		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.4 V ≤ V_{DD} < 2.5 V		12	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} < 3.6 V		20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA



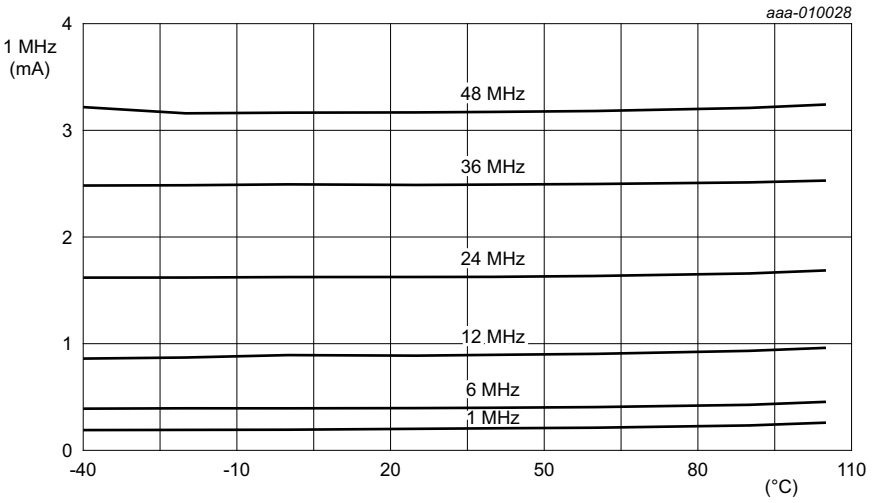
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F) all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 48 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 16. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.24	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
WatchDog oscillator at 600 kHz/2	0	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
System PLL	0.25	-	-	-
CLKOUT	-	0.25	0.89	System PLL is source of CLKOUT.
ROM	-	0.09	0.37	-
FLASHREG	-	0.17	0.66	-
FLASHARRAY	-	0.13	0.52	-
SRAM1	-	0.15	0.59	-
SRAM2	-	0.14	0.56	-
GPIO + pin interrupt/pattern match	-	0.18	0.69	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.08	0.30	-
SCTimer0/PWM + SCTimer1/PWM	-	0.29	1.1	-
CT16B0	-	0.05	0.17	-
CT16B1	-	0.04	0.16	-
CT32B0	-	0.04	0.13	-
CT32B1	-	0.03	0.13	-
RTC	-	0.02	0.10	-

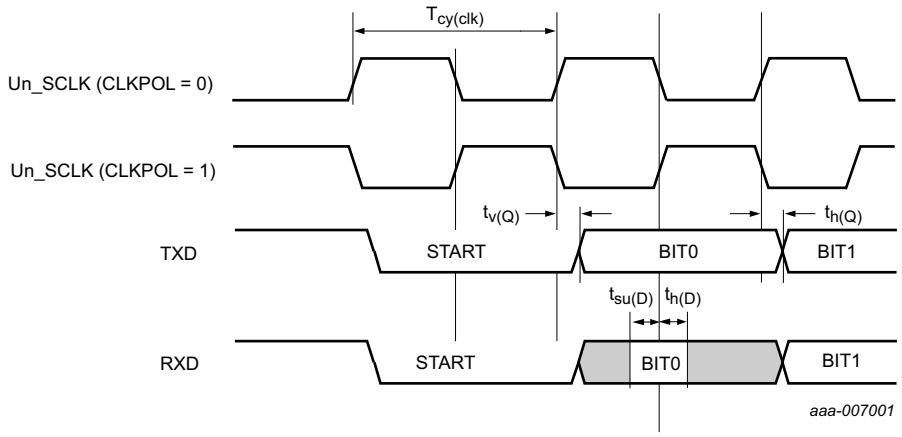


Fig 34. USART timing

12.8 SCTimer/PWM output timing

To estimate the skew between different outputs, compare the worst case to worst case (or best case to best case) values of individual pins.

Table 20. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V. Simulated skew (over process, voltage, and temperature) between any two SCT outputs; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
SCTimer0/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns
SCTimer1/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns

13. Characteristics of analog peripherals

Table 21. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.54	-	V
		de-assertion		-	2.68	-	V
		interrupt level 3					
		assertion		-	2.82	-	V
		de-assertion		-	2.93	-	V
		reset level 2					
		assertion		-	2.34	-	V
		de-assertion		-	2.49	-	V
		reset level 3					
		assertion		-	2.62	-	V
		de-assertion		-	2.77	-	V

[1] Interrupt and reset levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11E6x user manual*. Interrupt levels 0 and 1 are reserved.

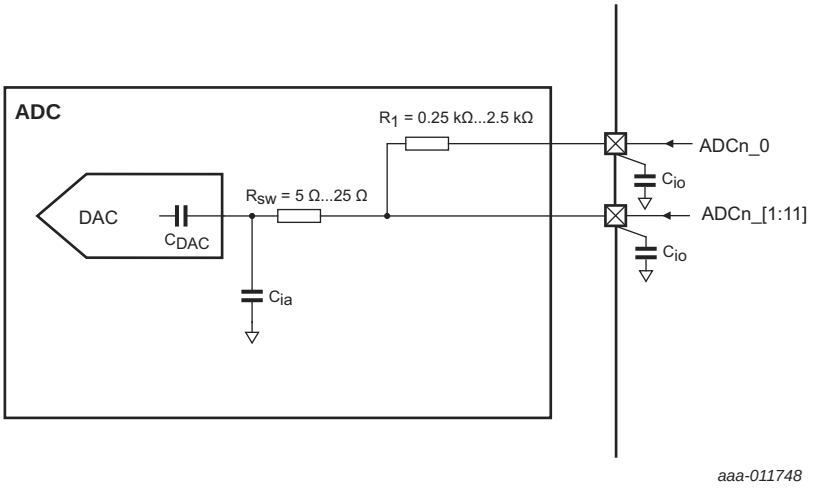


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

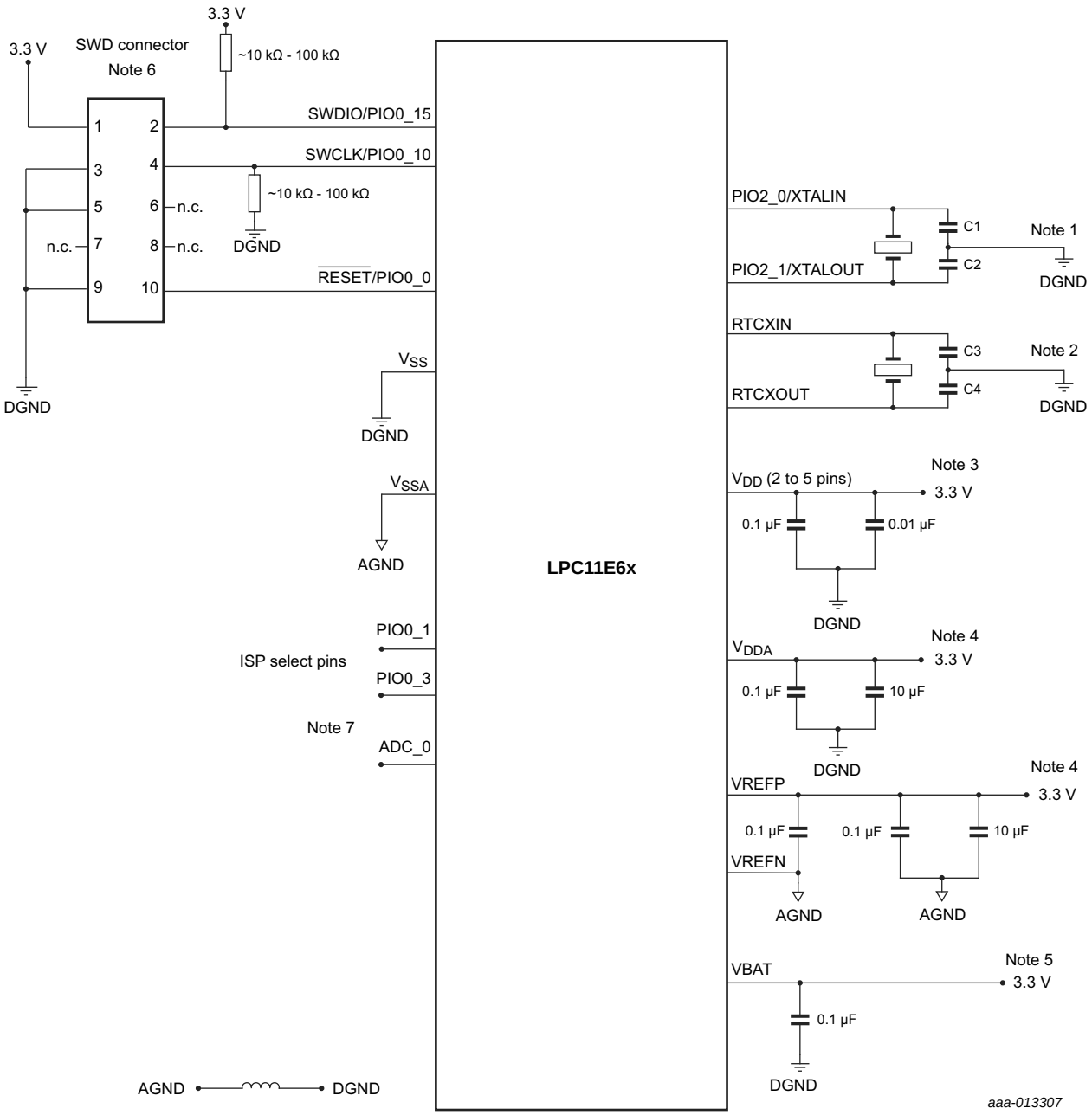
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C		-	−2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105 °C		-	606	-	mV



(1) See Section 14.3 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.5 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

Fig 41. Power, clock, and debug connections

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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