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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11e67jbd64e

5. Marking

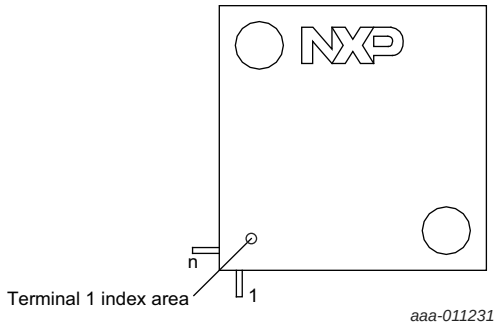


Fig 1. LQFP64/100 package marking

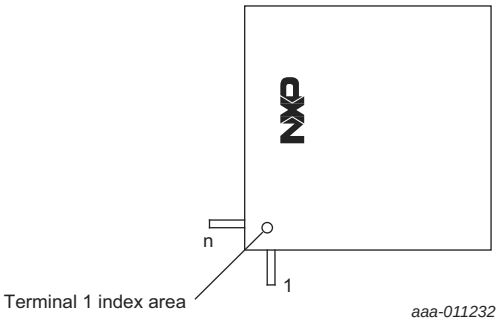


Fig 2. LQFP48 package marking

5.1 Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ

xx xx

xxxyy

wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

Field ‘R’ identifies the device revision.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO0_7	24	30	45 [5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
					I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART.
					-	**R_5 —** Reserved.
					IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58 [6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
					IO	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R_6 —** Reserved.
PIO0_9	27	38	59 [6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
					IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
					O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60 [6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					IO	**PIO0_10 —** General-purpose digital input/output pin.
					IO	**SSP0_SCK —** Serial clock for SSP0.
					O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64 [3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
					IO	**PIO0_11 —** General-purpose digital input/output pin.
					AI	**ADC_9 —** A/D converter, input channel 9.
					O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66 [3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
					IO	**PIO0_12 —** General-purpose digital input/output pin.
					AI	**ADC_8 —** A/D converter, input channel 8.
					I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
TDO/PIO0_13	32	45	68 [3]	I; PU	IO	**TDO —** Test Data Out for JTAG interface. In boundary scan mode only.
					IO	**PIO0_13 —** General-purpose digital input/output pin.
					AI	**ADC_7 —** A/D converter, input channel 7.
					O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I	**U1_RXD —** Receiver input for USART1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
$\overline{\text{TRST}}$/PIO0_14	33	46	69	[3]	I; PU	IO	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. In boundary scan mode only.
						IO	**PIO0_14 —** General-purpose digital input/output pin.
						AI	**ADC_6 —** A/D converter, input channel 6.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						O	**U1_TXD —** Transmitter output for USART1.
SWDIO/PIO0_15	37	50	81	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						IO	**PIO0_15 —** General-purpose digital input/output pin.
						AI	**ADC_3 —** A/D converter, input channel 3.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/WAKEUP	38	51	82	[4]	I; PU	IO	**PIO0_16 —** General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
						I	**ADC_2 —** A/D converter, input channel 2.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_8 —** Reserved.
PIO0_17	42	56	90	[6]	I; PU	IO	**PIO0_17 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART0 in synchronous mode.
PIO0_18	45	60	94	[6]	I; PU	IO	**PIO0_18 —** General-purpose digital input/output pin.
						I	**U0_RXD —** Receiver input for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19	46	61	95	[6]	I; PU	IO	**PIO0_19 —** General-purpose digital input/output pin.
						O	**U0_TXD —** Transmitter output for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20	10	12	17	[6]	I; PU	IO	**PIO0_20 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
						I	**U2_RXD —** Receiver input for USART2.
PIO0_21	17	22	33	[6]	I; PU	IO	**PIO0_21 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO1_7	-	6	10 [6]	I; PU	IO	**PIO1_7 —** General-purpose digital input/output pin.
					-	**R_17 —** Reserved.
					I	**U2_CTS —** Clear To Send input for USART2.
					I	**CT16B1_CAP0 —** Capture input 0 for 32-bit timer 1.
PIO1_8	-	-	61 [6]	I; PU	IO	**PIO1_8 —** General-purpose digital input/output pin.
					-	**R_18 —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_9	-	55	86 [3]	I; PU	IO	**PIO1_9 —** General-purpose digital input/output pin.
					I	**U0_CTS —** Clear To Send input for USART0.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					AI	**ADC_0 —** A/D converter, input channel 0.
PIO1_10	-	13	18 [6]	I; PU	IO	**PIO1_10 —** General-purpose digital input/output pin.
					O	**U2_RTS —** Request To Send output for USART2.
					IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
					O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_11	-	-	65 [6]	I; PU	IO	**PIO1_11 —** General-purpose digital input/output pin.
					IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
					O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I	**U0_RI —** Ring Indicator input for USART0.
PIO1_12	-	-	89 [6]	I; PU	IO	**PIO1_12 —** General-purpose digital input/output pin.
					IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
					O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	**R_21 —** Reserved.
PIO1_13	36	49	78 [6]	I; PU	IO	**PIO1_13 —** General-purpose digital input/output pin.
					I	**U1_CTS —** Clear To Send input for USART1.
					O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
					-	**R_22 —** Reserved.
PIO1_14	-	-	79 [6]	I; PU	IO	**PIO1_14 —** General-purpose digital input/output pin.
					IO	**I2C1_SDA —** I^2C1-bus data input/output (not open-drain).
					O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					-	**R_23 —** Reserved.
PIO1_15	-	-	87 [6]	I; PU	IO	**PIO1_15 —** General-purpose digital input/output pin.
					IO	**SSP0_SSEL —** Slave select for SSP0.
					O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	**R_24 —** Reserved.

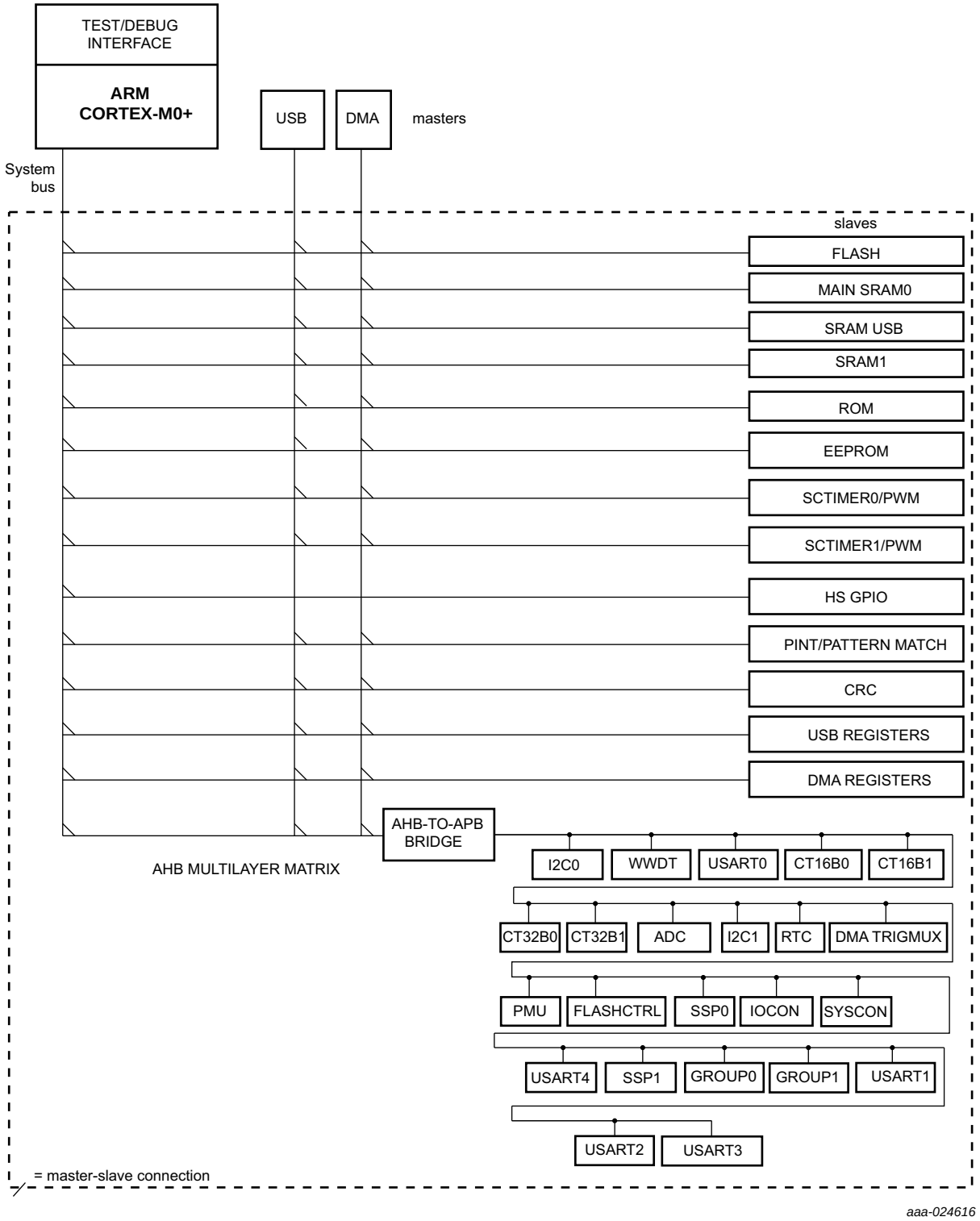


Fig 7. AHB multilayer matrix

Table 4. PWM resources

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT16B0	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	4
2	2	2	CT16B1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	3
3	3	3	CT32B0	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	4
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.18.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.18.1.1 Features

- Each SCTimer/PWM supports:
  - 5 match/capture registers.
  - 6 events.
  - 8 states.
  - 4 inputs and 4 outputs.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to four single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.

- Each event can be assigned to one or more states.
- State variable allows sequencing across multiple counter cycles.

- SCTimer match outputs (ORed with the general-purpose timer match outputs) serve as ADC hardware trigger inputs.

8.18.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1)

The LPC11E6x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.18.2.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM output function.
- Match outputs and capture inputs serve as hardware triggers for ADC conversions.

8.19 System tick timer (SysTick)

The ARM Cortex-M0+ includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.20 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

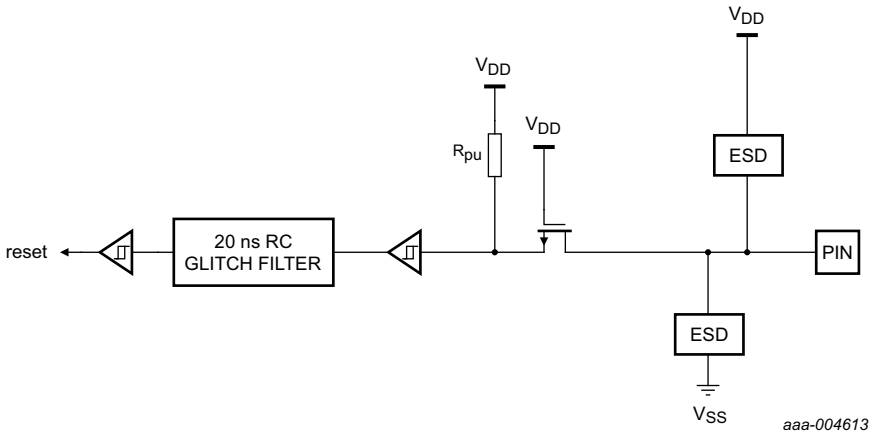


Fig 12. $\overline{\text{RESET}}$ pin configuration

8.25.2 Brownout detection

The LPC11E6x includes two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.25.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11U6x/E6x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[2]	–0.5	4.6	V
V_{DDA}	analog supply voltage			–0.5	4.6	V
V_{ref}	reference voltage	on pin VREFP		–0.5	4.6	V
V_{BAT}	battery supply voltage			–0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	–0.5	+5.5	V
		on open-drain I2C-bus pins PIO0_4 and PIO0_5	[5]	–0.5	+5.5	V
V_{IA}	analog input voltage		[6] [7]	–0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage	pins configured for XTALIN and XTALOUT	[2]	–0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage		[2]	–0.5	4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5\ V_{DD(IO)}) < V_I < (1.5\ V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[8]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[9]	-	3	kV

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_4 and PIO0_5.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[16]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[16]	−10	−50	−85	μA
		$V_{DD} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[17]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN	[19]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT	[19]	−0.5	-	3.6	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[20]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	[20]	-	-	2.5	pF
		pins with digital functions only	[20]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

[12] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[13] Including voltage on outputs in tri-state mode.

[14] Tri-state outputs go into tri-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 13.

[17] To V_{SS}.

[18] The parameter values specified are simulated and absolute values.

[19] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)} < \max(VBAT, V_{DD})$.

[20] Including bonding pad capacitance.

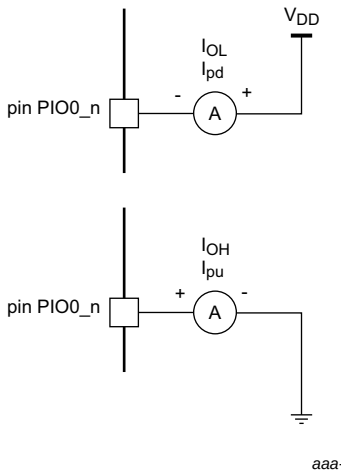
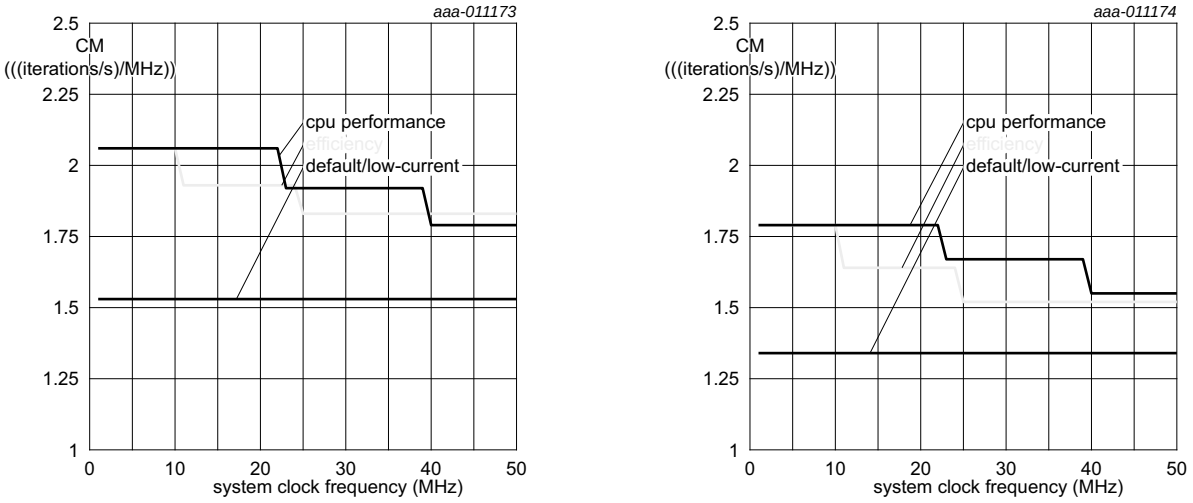


Fig 13. Pin input/output current measurement

11.2 CoreMark data

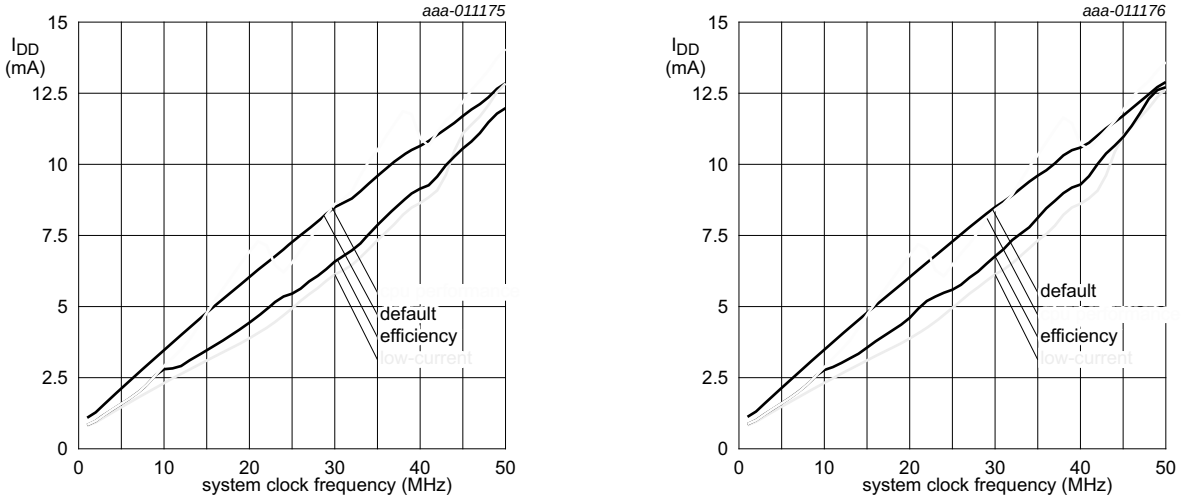


Measured with Keil uVision v.4.72.

Measured with Keil uVision v.4.60.

Conditions: Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCTimer disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled.

Fig 21. CoreMark score for different power mode settings of the power profiles



Measured with Keil uVision v.4.72.

Measured with Keil uVision v.4.60.

Conditions: Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCTimer disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled.

Fig 22. Active mode: CoreMark power consumption I_{DD} for different power mode settings of the power profiles

The CoreMark scores serve as a guideline to select the best power mode for a given application. To find the most suitable power mode, run the application in mode and compare power consumption and performance.

The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.24	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
WatchDog oscillator at 600 kHz/2	0	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
System PLL	0.25	-	-	-
CLKOUT	-	0.25	0.89	System PLL is source of CLKOUT.
ROM	-	0.09	0.37	-
FLASHREG	-	0.17	0.66	-
FLASHARRAY	-	0.13	0.52	-
SRAM1	-	0.15	0.59	-
SRAM2	-	0.14	0.56	-
GPIO + pin interrupt/pattern match	-	0.18	0.69	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.08	0.30	-
SCTimer0/PWM + SCTimer1/PWM	-	0.29	1.1	-
CT16B0	-	0.05	0.17	-
CT16B1	-	0.04	0.16	-
CT32B0	-	0.04	0.13	-
CT32B1	-	0.03	0.13	-
RTC	-	0.02	0.10	-

Table 14. Dynamic characteristics: WatchDog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the *LPC11E6x user manual.*

12.4 I/O pins

Table 15. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 16. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.26	-	µs

12.7 USART interface

The maximum USART bit rate for all USARTs is 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.

Table 18. USART dynamic characteristics USART0

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	[1]	100	-	ns
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time		44	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	10	ns
$t_{h(Q)}$	data output hold time		0	-	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		20	-	ns
$t_{v(Q)}$	data output valid time		-	40	ns
$t_{h(Q)}$	data output hold time		25	-	ns

[1] $T_{cy(clk)}$ = (main clock cycle time)/(UARTCLKDIV x 2 x (256 x DLM + DLL)). See the *LPC11E6x User manual UM10732*.

Table 19. USART dynamic characteristics USART1/2/3/4

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	[1]	100	-	ns
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time		44	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	10	ns
$t_{h(Q)}$	data output hold time		0	-	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	40	ns
$t_{h(Q)}$	data output hold time		20	-	ns

[1] $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the *LPC11E6x User manual UM10732*.

keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 40. If the RTC is not used, the RTCXIN pin can be grounded.

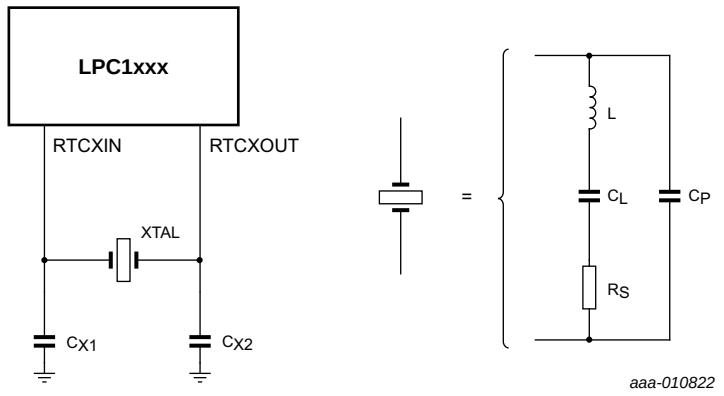


Fig 40. RTC oscillator components

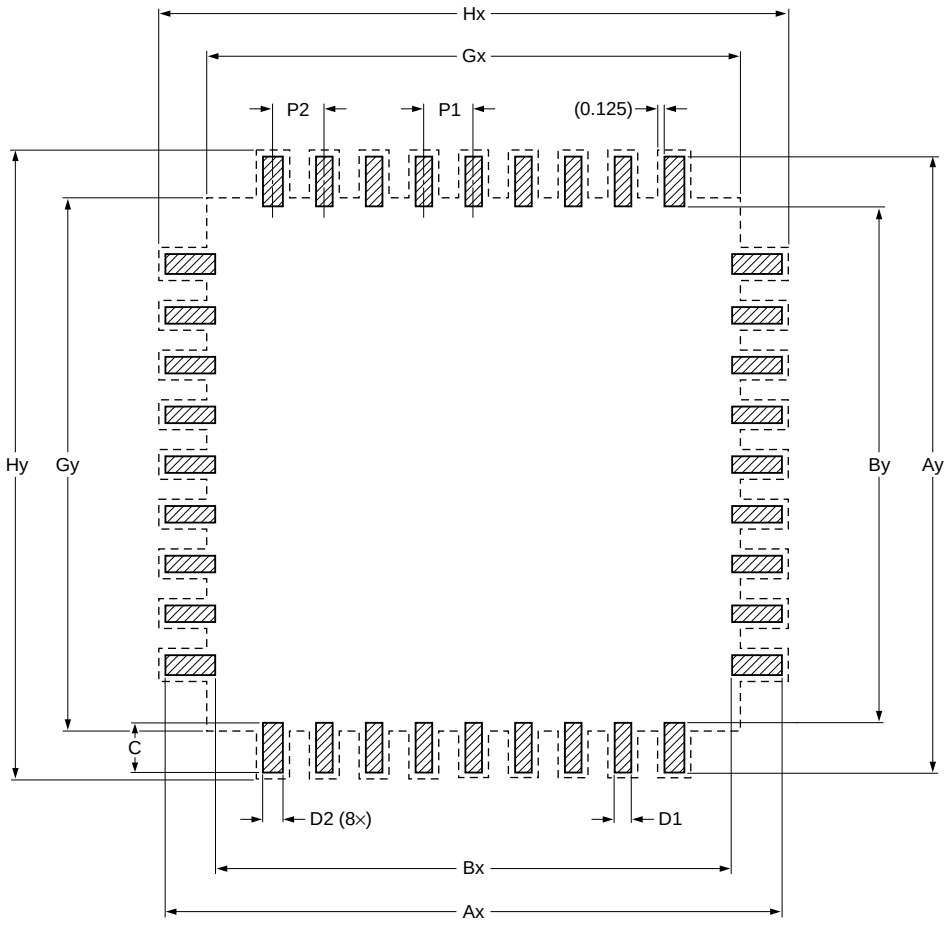
Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry. The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If load capacitance of the external crystal is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$$C_{x1} = C_{x2} = 2 \times C_L - C_P$$

14.6 Connecting power, clocks, and debug functions

Figure 41 shows the basic board connections to power the LPC11E6x, to connect an external crystal and the 32 kHz oscillator, and provide debug capabilities.

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 46. Reflow soldering for the LQFP64 package

17. Abbreviations

Table 31. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC11U6x/E6x User manual UM10732: http://www.nxp.com/documents/user_manual/UM10732.pdf

[2] LPC11E6x Errata sheet: http://www.nxp.com/documents/errata_sheet/ES_LPC11E6X.pdf

[3] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

22. Contents

continued >>