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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11e68jbd100e

- 32-bit integer division routines.

- Digital peripherals:
  - Simple DMA engine with 16 channels and programmable input triggers.
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 80 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and programmable glitch filter and digital filter.
  - Pin interrupt and pattern match engine using eight selectable GPIO pins.
  - Two GPIO group interrupt generators.
  - CRC engine.
- Configurable PWM/timer subsystem (two 16-bit and two 32-bit standard counter/timers, two State-Configurable Timers (SCTimer/PWM)) that provides:
  - Up to four 32-bit and two 16-bit counter/timers or two 32-bit and six 16-bit counter/timers.
  - Up to 21 match outputs and 16 capture inputs.
  - Up to 19 PWM outputs with 6 independent time bases.
- Windowed WatchDog timer (WWDT).
- Real-time Clock (RTC) in the always-on power domain with separate battery supply pin and 32 kHz oscillator.
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 2 Msamples/s. The ADC supports two independent conversion sequences.
  - Temperature sensor.
- Serial interfaces:
  - Up to five USART interfaces, all with DMA, synchronous mode, and RS-485 mode support. Four USARTs use a shared fractional baud generator.
  - Two SSP controllers with DMA support.
  - Two I^2C-bus interfaces. One I^2C-bus interface with specialized open-drain pins supports I2C Fast-mode Plus.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - On-chip 32 kHz oscillator for RTC.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz. Oscillator pins are shared with the GPIO pins.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on external pin inputs and USART activity.

5. Marking

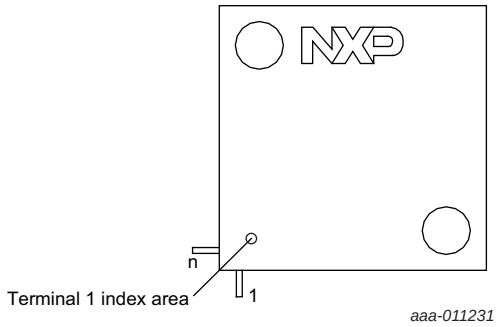


Fig 1. LQFP64/100 package marking

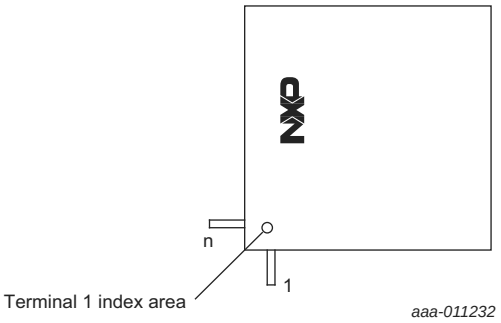


Fig 2. LQFP48 package marking

5.1 Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ

xx xx

xxxyy

wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

Field ‘R’ identifies the device revision.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO0_7	24	30	45 [5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
					I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART.
					-	**R_5 —** Reserved.
					IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58 [6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
					IO	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R_6 —** Reserved.
PIO0_9	27	38	59 [6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
					IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
					O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60 [6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					IO	**PIO0_10 —** General-purpose digital input/output pin.
					IO	**SSP0_SCK —** Serial clock for SSP0.
					O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64 [3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
					IO	**PIO0_11 —** General-purpose digital input/output pin.
					AI	**ADC_9 —** A/D converter, input channel 9.
					O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66 [3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
					IO	**PIO0_12 —** General-purpose digital input/output pin.
					AI	**ADC_8 —** A/D converter, input channel 8.
					I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
TDO/PIO0_13	32	45	68 [3]	I; PU	IO	**TDO —** Test Data Out for JTAG interface. In boundary scan mode only.
					IO	**PIO0_13 —** General-purpose digital input/output pin.
					AI	**ADC_7 —** A/D converter, input channel 7.
					O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					I	**U1_RXD —** Receiver input for USART1.

[1] Pin state at reset for default function: I = Input; O = Output; AI = Analog Input; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled;
F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] Special analog pad.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital input glitch filter. WAKEUP pin. The wake-up pin function can be disabled and the pin can be used for other purposes if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[9] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog crystal oscillator connections. When configured for the crystal oscillator input/output, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

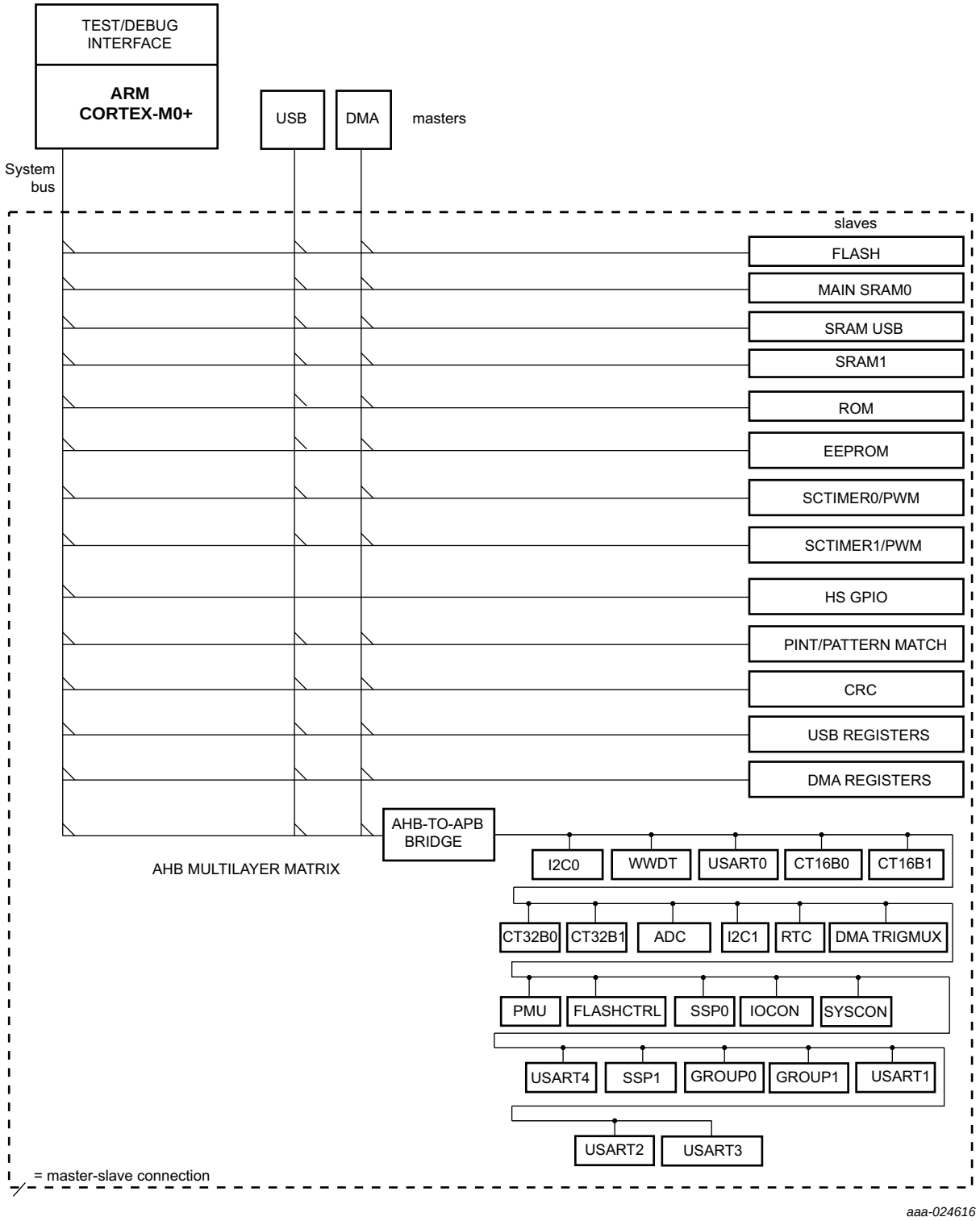


Fig 7. AHB multilayer matrix

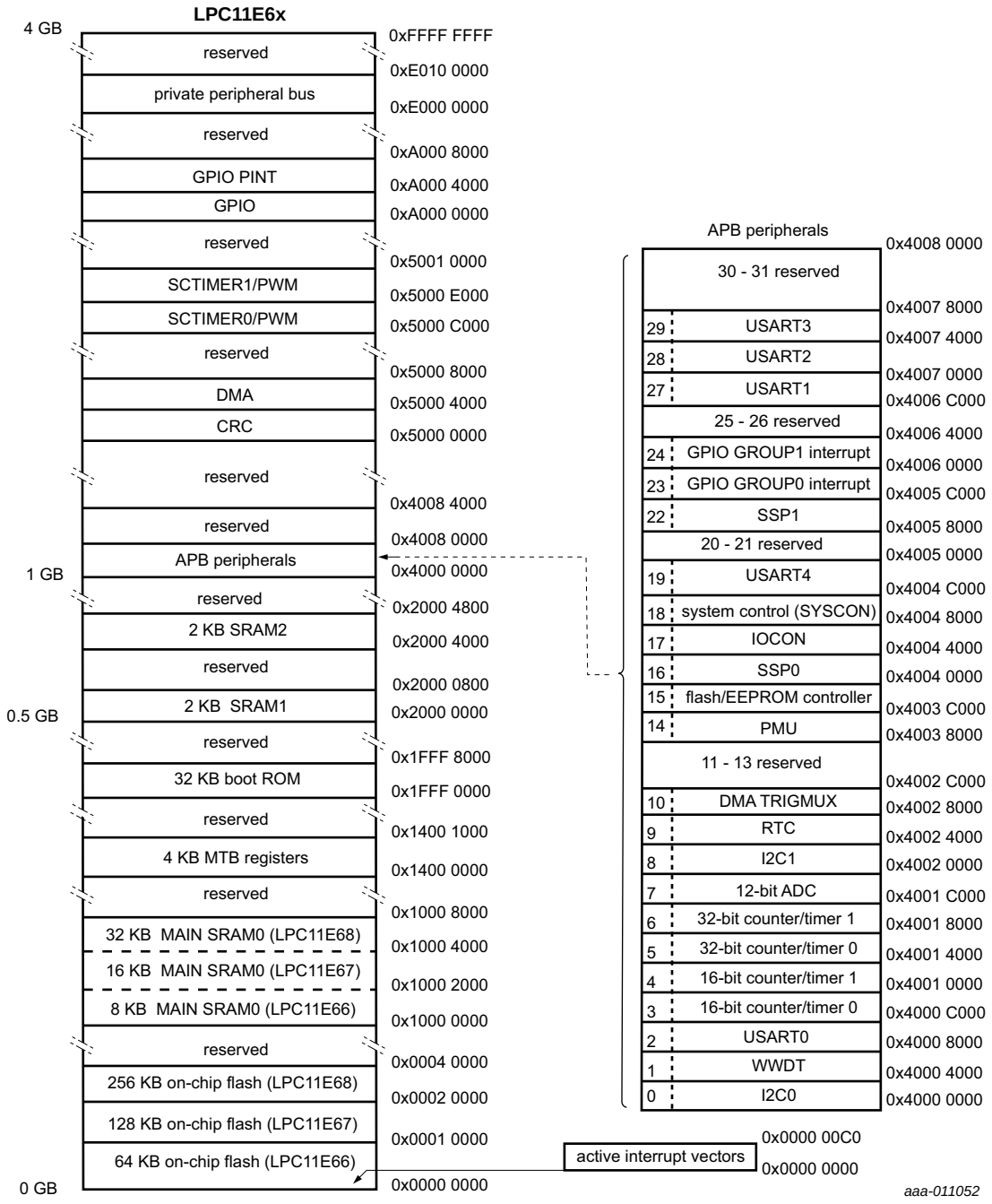


Fig 8. LPC11E6x Memory map

8.8 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.14 USART0

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/3x parts. USART1 to USART4 use a different register interface.

The USART0 includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART0 uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.14.1 Features

- Maximum USART0 data bit rate of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.
- DMA support.

8.15 USART1/2/3/4

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/LPC11E3x parts. USART1 to USART4 use a different register interface to achieve the same UART functionality except for modem and smart card control.

Remark: USART4 IS available only on part LPC11E68JBD100.

Interrupts generated by the USART1/2/3/4 peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled. This wake-up mechanism is not available with the USART0 peripheral.

8.15.1 Features

- Maximum bit rates of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits

- 4-bit to 16-bit frame
- DMA support

8.17 I²C-bus serial I/O controller

The LPC11E6x contain two I²C-bus controllers.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.17.1 Features

- One I²C-interface (I2C0) is an I²C-bus compliant interface with open-drain pins. The I²C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- One I²C-interface (I2C1) uses standard digital pins. The I²C-bus interface supports bit rates up to 400 kbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

8.18 Timer/PWM subsystem

Four standard timers and two state configurable timers can be combined to create multiple PWM outputs using the match outputs and the match registers for each timer. Each timer can create multiple PWM outputs with its own time base.

8.18.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.18.1.1 Features

- Each SCTimer/PWM supports:
  - 5 match/capture registers.
  - 6 events.
  - 8 states.
  - 4 inputs and 4 outputs.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to four single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.

consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.24.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11E6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

8.24.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

8.24.7.3 Deep-sleep mode

In Deep-sleep mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11E6x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Deep-sleep mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Deep-sleep mode saves power and allows for short wake-up times.

8.24.7.4 Power-down mode

In Power-down mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition, all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x/Ex user manual*.

8.26 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11E6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

[6] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] Dependent on package type.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP48				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	67	°C/W
		1 m/s	58	°C/W
		2.5 m/s	53	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	100	°C/W
		1 m/s	79	°C/W
		2.5 m/s	71	°C/W
θjc	thermal resistance junction-to-case		15	°C/W
θjb	thermal resistance junction-to-board		19	°C/W
LQFP64				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	58	°C/W
		1 m/s	51	°C/W
		2.5 m/s	47	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	81	°C/W
		1 m/s	66	°C/W
		2.5 m/s	60	°C/W

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[16]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[16]	−10	−50	−85	μA
		$V_{DD} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[17]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN	[19]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT	[19]	−0.5	-	3.6	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[20]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	[20]	-	-	2.5	pF
		pins with digital functions only	[20]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

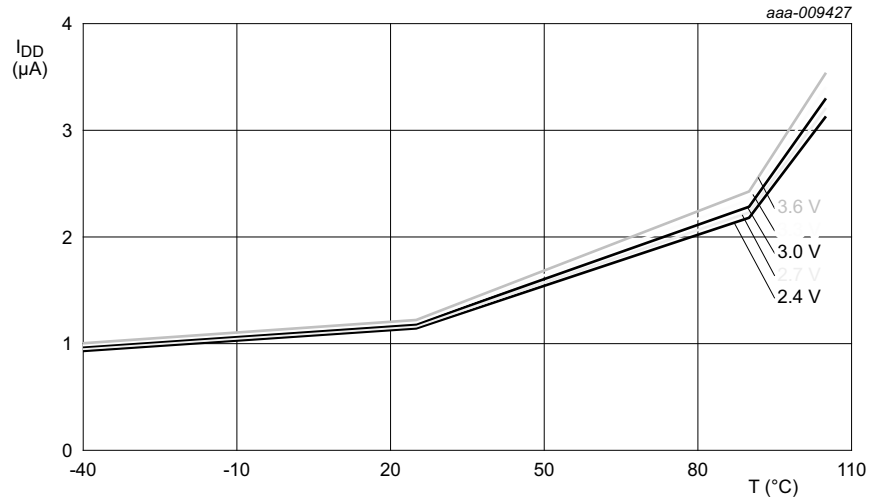
[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

[12] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

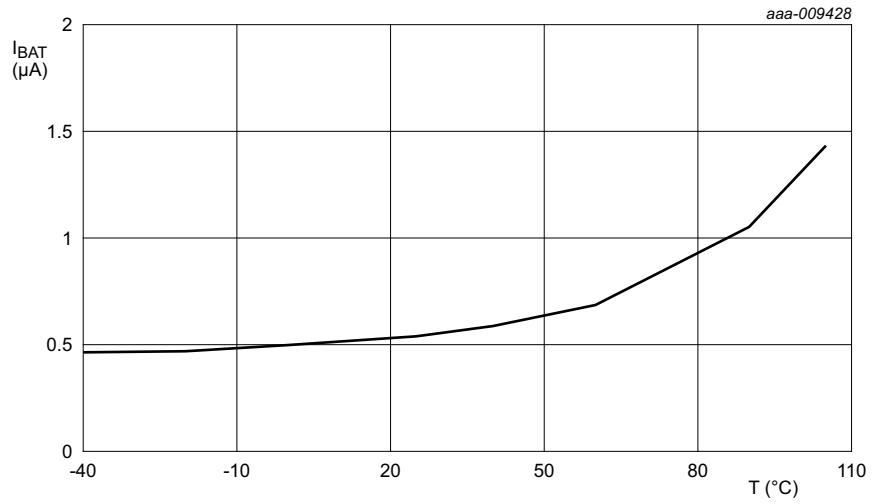
[13] Including voltage on outputs in tri-state mode.

[14] Tri-state outputs go into tri-state mode in Deep power-down mode.



Conditions: RTC running; VBAT = 0 V

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: RTC not running; V_{BAT} = 3.0 V; V_{DD} floating.

Fig 20. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

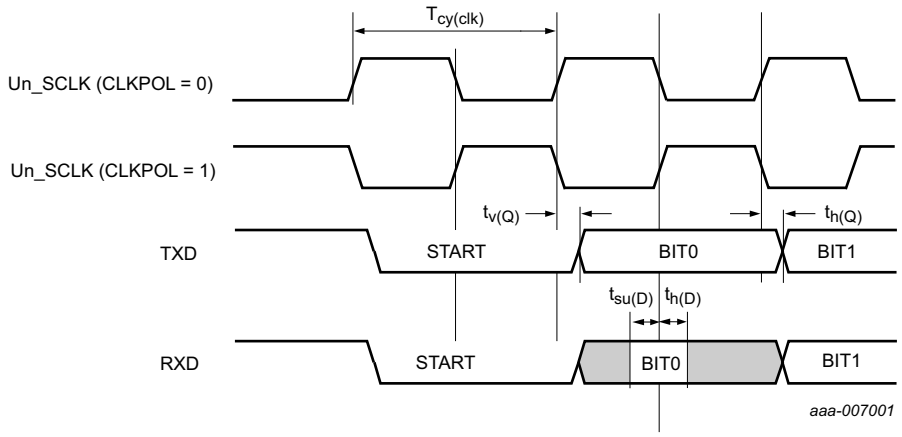


Fig 34. USART timing

12.8 SCTimer/PWM output timing

To estimate the skew between different outputs, compare the worst case to worst case (or best case to best case) values of individual pins.

Table 20. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V. Simulated skew (over process, voltage, and temperature) between any two SCT outputs; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
SCTimer0/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns
SCTimer1/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns

Table 22. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}. ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IA}	analog input voltage		[2]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[3]	-	-	0.1	pF
$f_{clk(ADC)}$	ADC clock frequency	$V_{DDA} \geq 2.7$ V				50	MHz
		$V_{DDA} \geq 2.4$ V				25	MHz
f_s	sampling frequency	$V_{DDA} \geq 2.7$ V			-	2	Msamples/s
		$V_{DDA} \geq 2.4$ V			-	1	Msamples/s
E_D	differential linearity error		[4]	-	-	±2.5	LSB
$E_{L(adj)}$	integral non-linearity		[5]	-	-	±2.5	LSB
E_O	offset error		[6]	-	-	±4.5	LSB
$V_{err(FS)}$	full-scale error voltage		[7]	-	-	±0.5	%
Z_i	input impedance	f_s = 2 Msamples/s	[8][9]	0.1	-	-	MΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The input resistance of ADC channel 0 is higher than for all other channels.

[3] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 2 Msamples/s.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 35.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 35.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 35.

[7] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 35.

[8] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.1 pF.

[9] Input resistance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia}: $Z_i \propto 1 / (f_s \times C_i)$. See Figure 36 “ADC input impedance”.

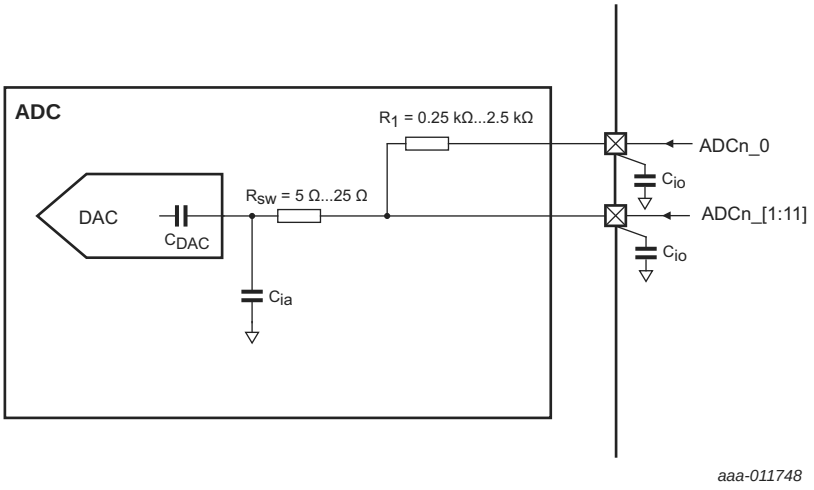


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

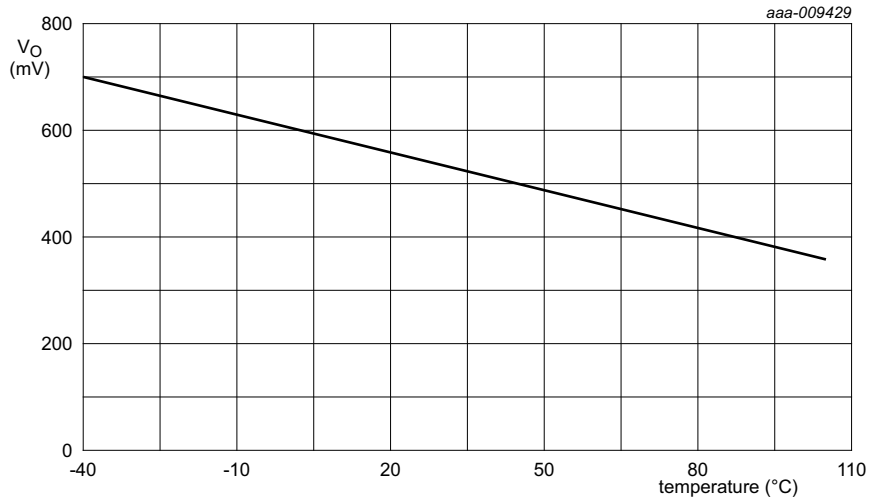
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C		-	−2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105 °C		-	606	-	mV



V_{DDA} = 3.3 V; measured on a typical silicon sample.

Fig 37. Typical LLS fit of the temperature sensor output voltage

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 22:

- The ADC input trace must be short and as close as possible to the LPC11E6x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Typical wake-up times

Table 25. Typical wake-up times
V_{DD} = 3.3 V; T_{amb} = 25 °C.

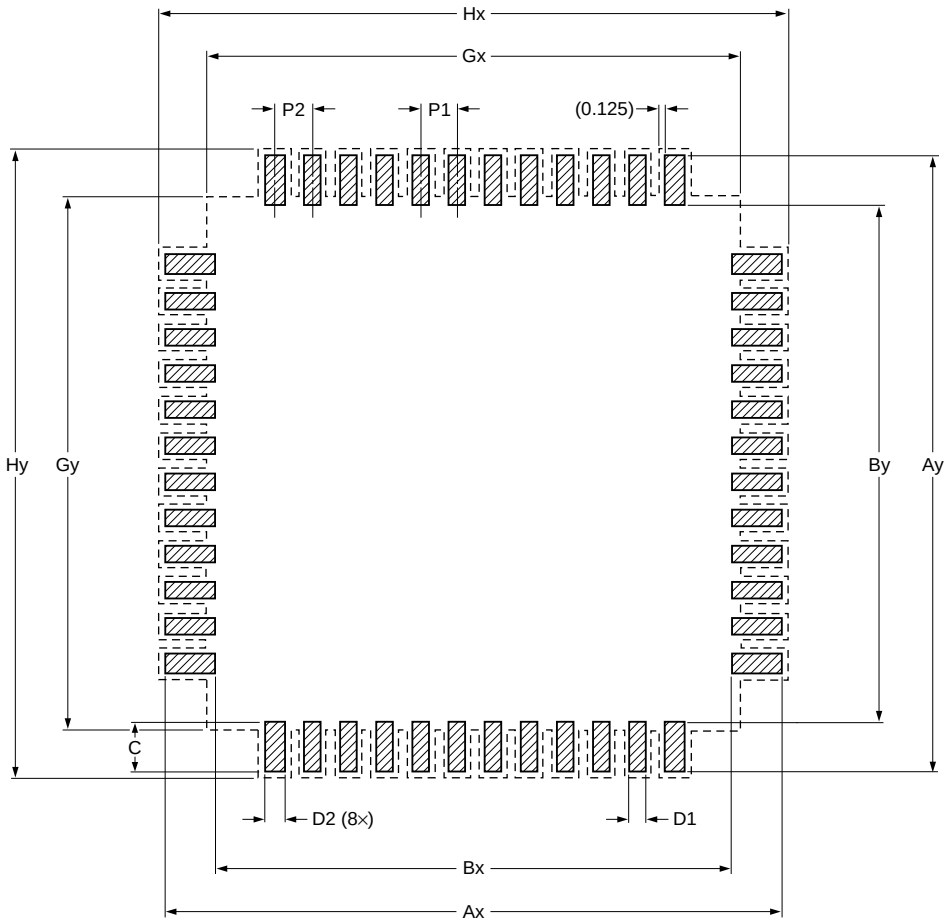
Power modes	Wake-up time
Sleep mode (12 MHz)[1][2]	2.6 μs
Deep-sleep mode[1][3]	4.4 μs
Power-down mode[1][3]	86.8 μs
Deep Power-down mode[4]	276 μs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake up the device from the low-power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

16. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

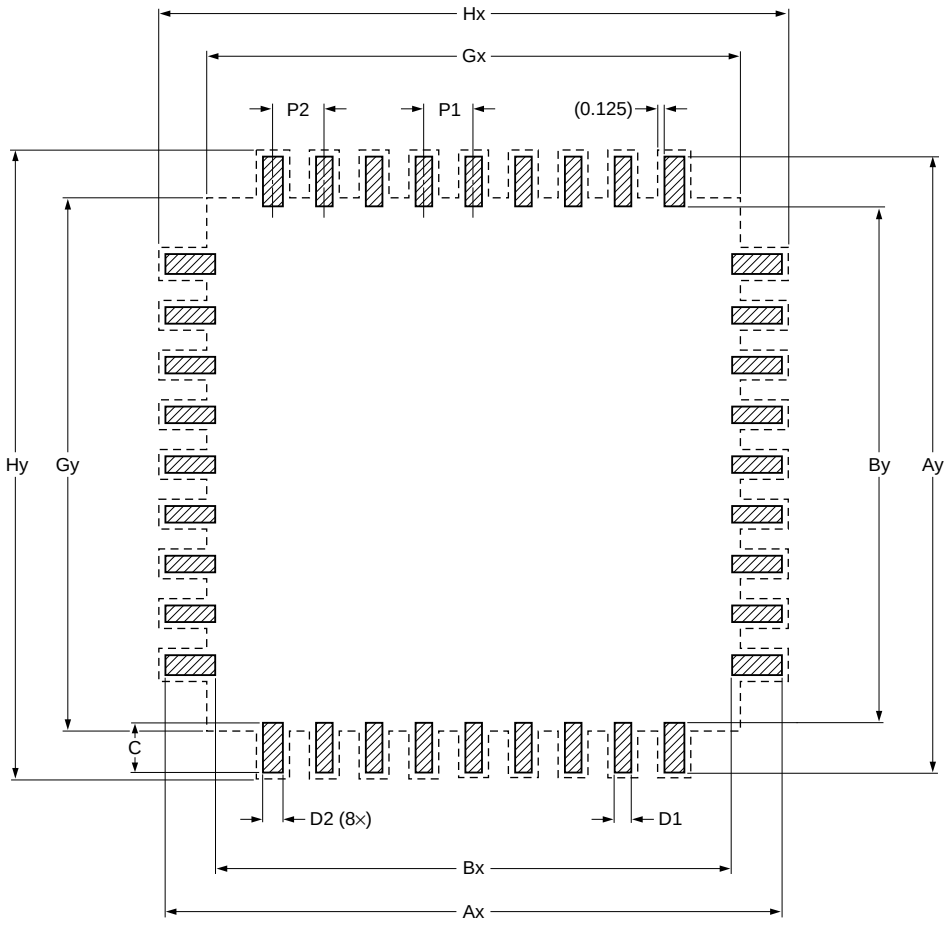
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 45. Reflow soldering for the LQFP48 package

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 46. Reflow soldering for the LQFP64 package