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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11e68jbd64e

5. Marking

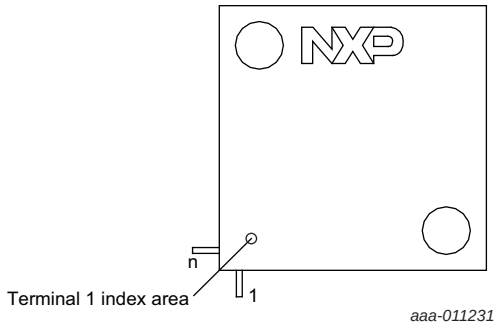


Fig 1. LQFP64/100 package marking

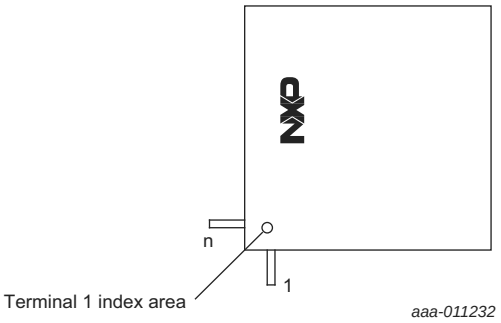


Fig 2. LQFP48 package marking

5.1 Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ

xx xx

xxxyy

wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

Field ‘R’ identifies the device revision.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO0_22	29	40	62 [3]	I; PU	IO	**PIO0_22 —** General-purpose digital input/output pin.
					AI	**ADC_11 —** A/D converter, input channel 11.
					I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					IO	**SSP1_MISO —** Master In Slave Out for SSP1.
PIO0_23	39	52	83 [3]	I; PU	IO	**PIO0_23 —** General-purpose digital input/output pin.
					AI	**ADC_1 —** A/D converter, input channel 1.
					-	**R_9 —** Reserved.
					I	**$\overline{\text{U0\_RI}}$ —** Ring Indicator input for USART0.
					IO	**SSP1_SSEL —** Slave select for SSP1.
PIO1_0	-	62	97 [6]	I; PU	IO	**PIO1_0 —** General-purpose digital input/output pin.
					O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					-	**R_10 —** Reserved.
					O	**U2_TXD —** Transmitter output for USART2.
PIO1_1	-	-	28 [6]	I; PU	IO	**PIO1_1 —** General-purpose digital input/output pin.
					O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					-	**R_11 —** Reserved.
					O	**$\overline{\text{U0\_DTR}}$ —** Data Terminal Ready output for USART0.
PIO1_2	-	-	55 [6]	I; PU	IO	**PIO1_2 —** General-purpose digital input/output pin.
					O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					-	**R_12 —** Reserved.
					I	**U1_RXD —** Receiver input for USART1.
PIO1_3	-	-	72 [3]	I; PU	IO	**PIO1_3 —** General-purpose digital input/output pin.
					O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	**R_13 —** Reserved.
					IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).
					AI	**ADC_5 —** A/D converter, input channel 5.
PIO1_4	-	-	23 [6]	I; PU	IO	**PIO1_4 —** General-purpose digital input/output pin.
					I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					-	**R_14 —** Reserved.
					I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
PIO1_5	-	-	47 [6]	I; PU	IO	**PIO1_5 —** General-purpose digital input/output pin.
					I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					-	**R_15 —** Reserved.
					I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
PIO1_6	-	-	98 [6]	I; PU	IO	**PIO1_6 —** General-purpose digital input/output pin.
					-	**R_16 —** Reserved.
					I	**U2_RXD —** Receiver input for USART2.
					I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.

8.3 On-chip flash programming memory

The LPC11E6x contain up to 256 KB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into 24 x 4 KB and 5 x 32 KB sectors. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.4 EEPROM

The LPC11E6x contain 4 KB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip bootloader software.

8.5 SRAM

The LPC11E6x contain a total of up to 36 KB on-chip static RAM memory. The main SRAM block contains either 8 KB, 16 KB. or 32 KB of main SRAM0. Two additional SRAM blocks of 2 KB (SRAM1 and SRAM2) are located in separate areas of the memory map. See Figure 8.

8.6 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - I2C
  - USART0 and USART1/2/3/4
  - DMA

8.7 Memory mapping

The LPC11E6x incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 KB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 KB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

8.14 USART0

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/3x parts. USART1 to USART4 use a different register interface.

The USART0 includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART0 uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.14.1 Features

- Maximum USART0 data bit rate of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.
- DMA support.

8.15 USART1/2/3/4

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/LPC11E3x parts. USART1 to USART4 use a different register interface to achieve the same UART functionality except for modem and smart card control.

Remark: USART4 IS available only on part LPC11E68JBD100.

Interrupts generated by the USART1/2/3/4 peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled. This wake-up mechanism is not available with the USART0 peripheral.

8.15.1 Features

- Maximum bit rates of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits

- 4-bit to 16-bit frame
- DMA support

8.17 I²C-bus serial I/O controller

The LPC11E6x contain two I²C-bus controllers.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.17.1 Features

- One I²C-interface (I2C0) is an I²C-bus compliant interface with open-drain pins. The I²C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- One I²C-interface (I2C1) uses standard digital pins. The I²C-bus interface supports bit rates up to 400 kbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

8.18 Timer/PWM subsystem

Four standard timers and two state configurable timers can be combined to create multiple PWM outputs using the match outputs and the match registers for each timer. Each timer can create multiple PWM outputs with its own time base.

8.18.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.18.1.1 Features

- Each SCTimer/PWM supports:
  - 5 match/capture registers.
  - 6 events.
  - 8 states.
  - 4 inputs and 4 outputs.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to four single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.

- Each event can be assigned to one or more states.
- State variable allows sequencing across multiple counter cycles.

- SCTimer match outputs (ORed with the general-purpose timer match outputs) serve as ADC hardware trigger inputs.

8.18.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1)

The LPC11E6x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.18.2.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM output function.
- Match outputs and capture inputs serve as hardware triggers for ADC conversions.

8.19 System tick timer (SysTick)

The ARM Cortex-M0+ includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.20 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

The LPC11E6x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Power-down mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.24.7.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the always-on RTC power domain. The LPC11E6x can wake up from Deep power-down mode via the WAKEUP pin or a wake-up signal generated by the RTC interrupt.

The LPC11E6x can be blocked from entering Deep power-down mode by setting a lock bit in the PMU block. Blocking the Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the WAKEUP pin is used in the application, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH while the part is in deep power-down mode. To wake up from deep power-down mode, pull the WAKEUP pin LOW. In addition, pull the RESET pin HIGH to prevent it from floating while in Deep power-down mode.

8.25 System control

8.25.1 Reset

Reset has four sources on the LPC11E6x: the RESET pin, the WatchDog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The RESET pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values. The internal reset status is reflected on the RSTOUT pin.

In Deep power-down mode, an external pull-up resistor is required on the RESET pin.

The RESET pin is operational in active, sleep, deep-sleep, and power-down modes if the RESET function is selected in the IOCON register for pin PIO0_0 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and also wakes up the part if in sleep, deep-sleep or power-down mode. The RESET pin is not functional in Deep power-down mode.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x/Ex user manual*.

8.26 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11E6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[16]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[16]	−10	−50	−85	μA
		$V_{DD} < V_I < 5$ V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[17]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN	[19]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT	[19]	−0.5	-	3.6	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[20]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	[20]	-	-	2.5	pF
		pins with digital functions only	[20]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

[12] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

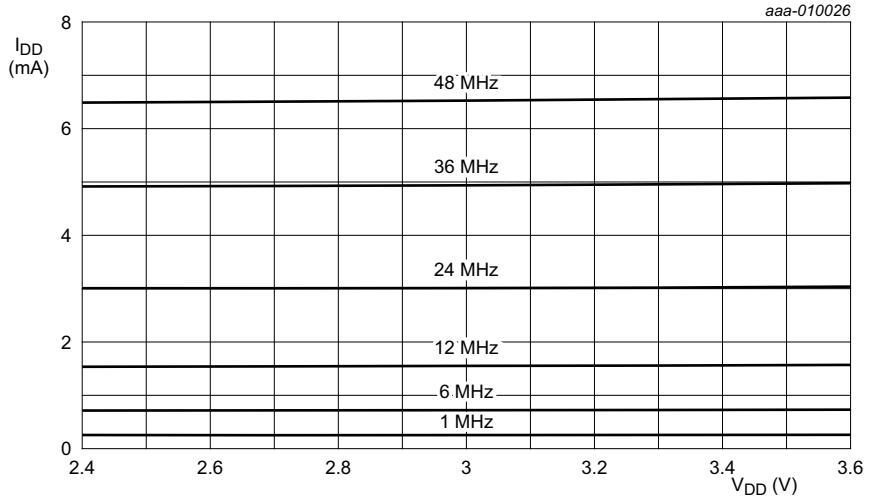
[13] Including voltage on outputs in tri-state mode.

[14] Tri-state outputs go into tri-state mode in Deep power-down mode.

11.1 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F), all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 14. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}

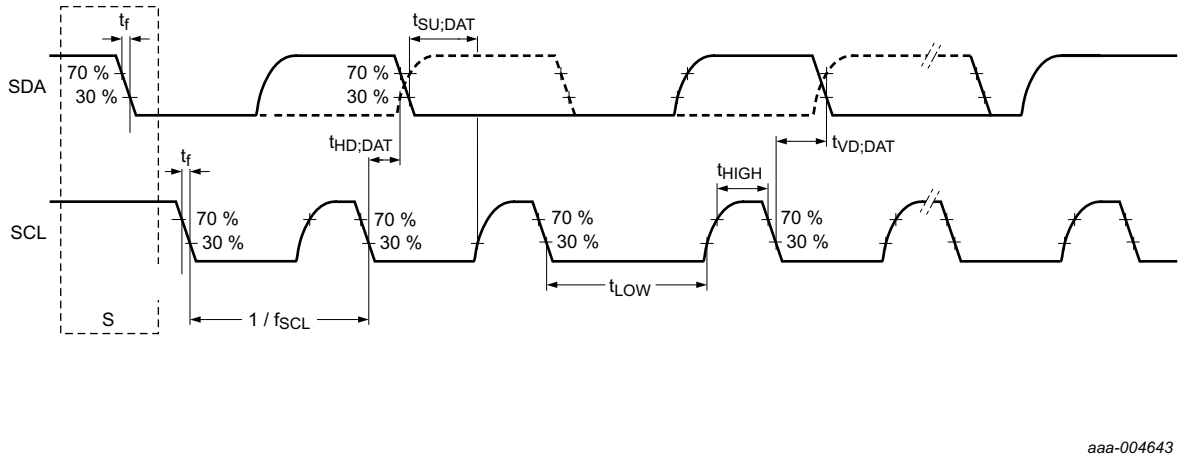


Fig 31. I²C-bus pins clock timing

12.6 SSP interface

Table 17. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40$ °C to 105 °C; 2.4 V ≤ V_{DD} ≤ 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

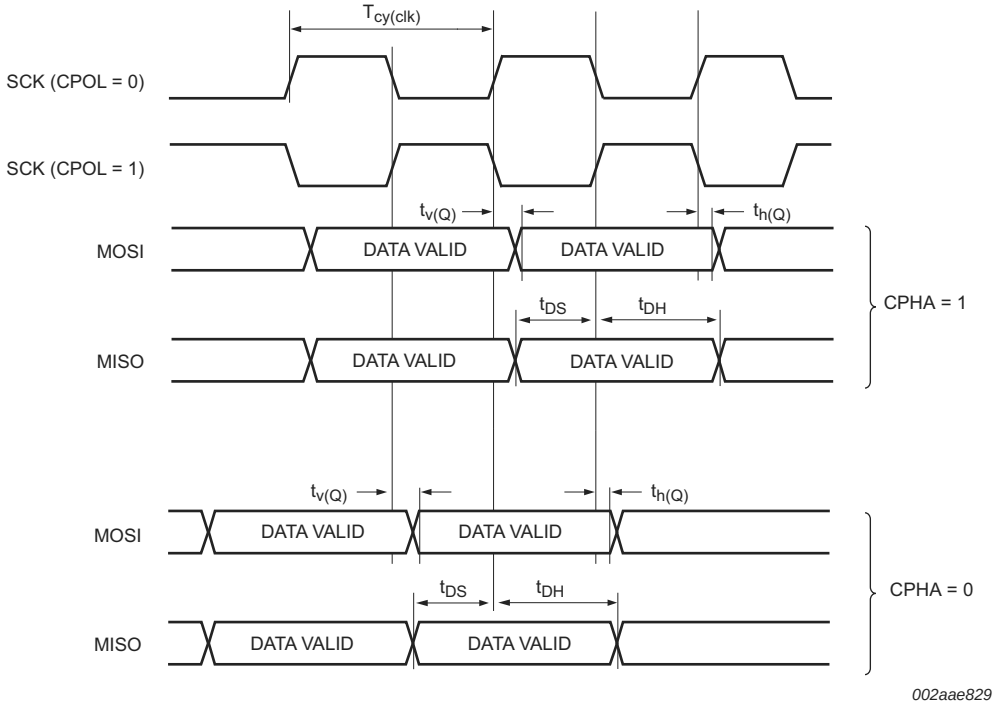


Fig 32. SSP master timing in SPI mode

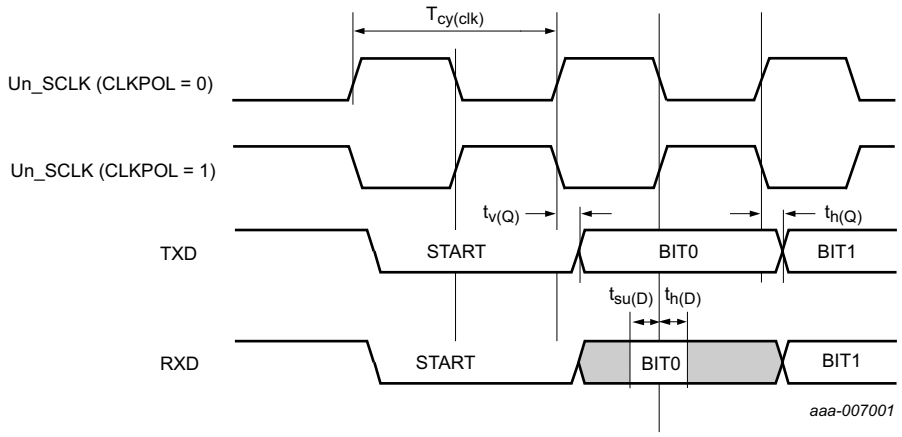


Fig 34. USART timing

12.8 SCTimer/PWM output timing

To estimate the skew between different outputs, compare the worst case to worst case (or best case to best case) values of individual pins.

Table 20. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V. Simulated skew (over process, voltage, and temperature) between any two SCT outputs; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
SCTimer0/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns
SCTimer1/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns

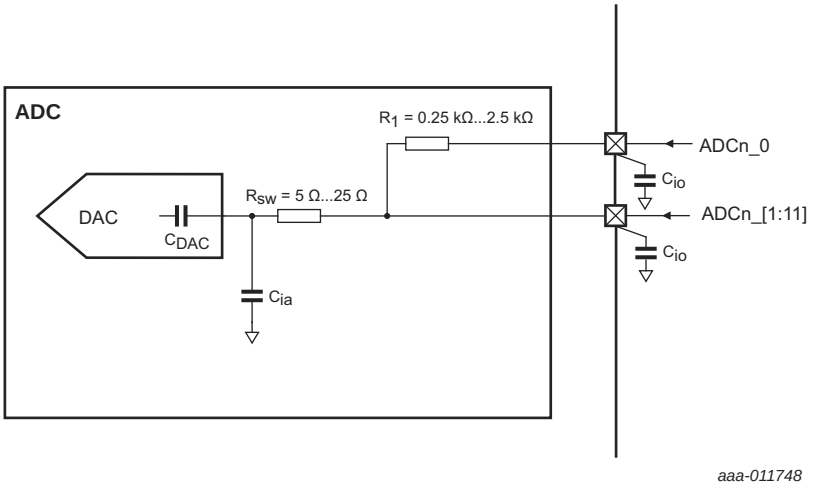


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

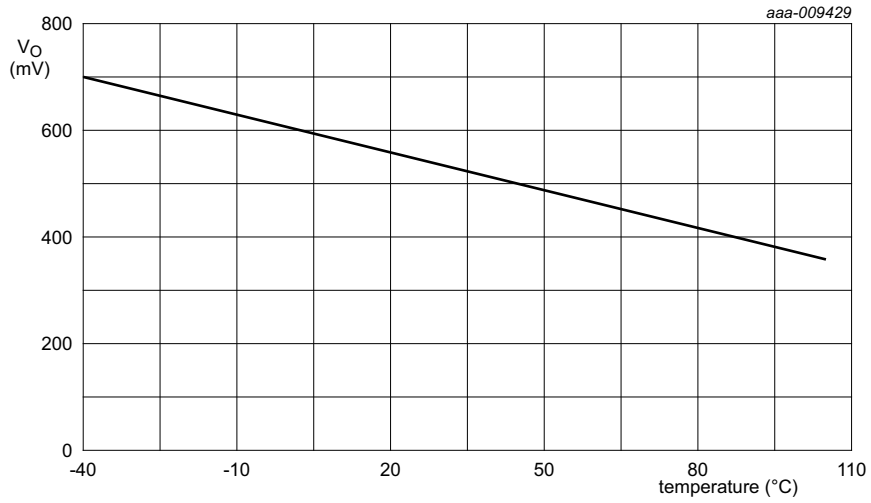
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C		-	−2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105 °C		-	606	-	mV



V_{DDA} = 3.3 V; measured on a typical silicon sample.

Fig 37. Typical LLS fit of the temperature sensor output voltage

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 22:

- The ADC input trace must be short and as close as possible to the LPC11E6x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Typical wake-up times

Table 25. Typical wake-up times
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Power modes	Wake-up time
Sleep mode (12 MHz)[1][2]	2.6 μs
Deep-sleep mode[1][3]	4.4 μs
Power-down mode[1][3]	86.8 μs
Deep Power-down mode[4]	276 μs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake up the device from the low-power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

[3] WatchDog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake up the device from the low-power modes and when a GPIO output pin is set in the reset handler.

14.3 XTAL input and crystal oscillator component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

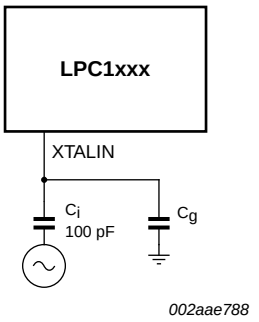


Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled through a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 39 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 39 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

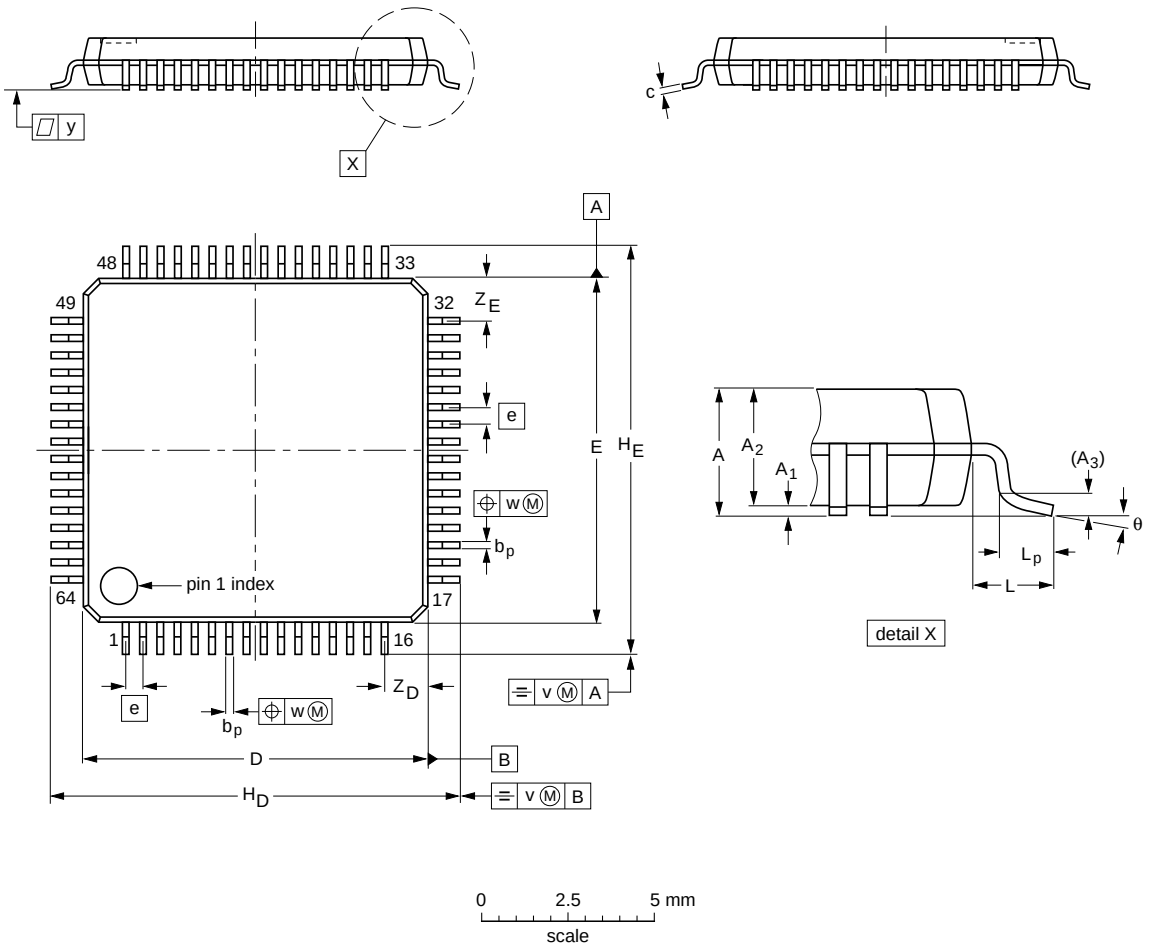
14.8 Pin states in different power modes

Table 29. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_4/PIO0_5 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
PIO0_16/ WAKEUP	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

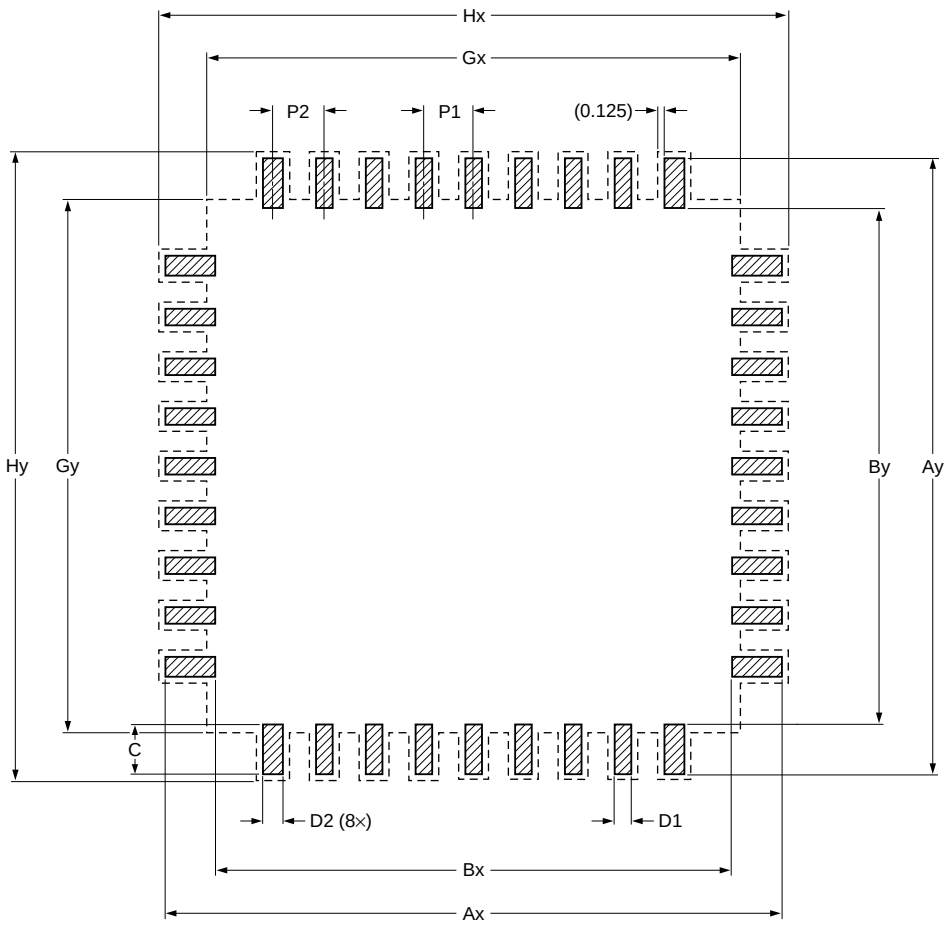
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 43. Package outline LQFP64 (SOT314-2)

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 47. Reflow soldering for the LQFP100 package