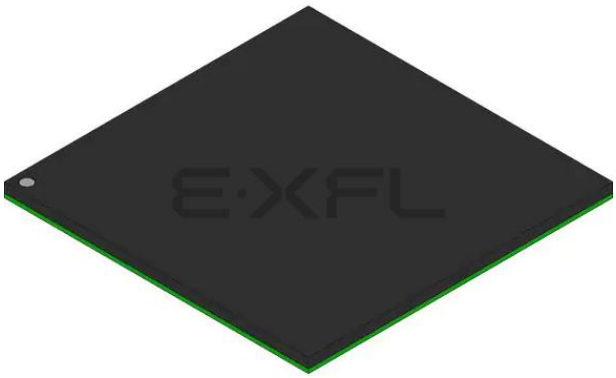

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc5200bv400

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	Vin = 0 or VDD_IO/VDD_IO_MEM$_{SDR}$ (depending on input type [1])	I_{IN}	—	±10	µA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.14
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor - memory I/O buffers	PULLUP_MEM VDD_IO_MEM$_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin[3]		I_{CS}	-1.0	1.0	mA	D3.23
Capacitance	Vin = 0V, f = 1 MHz	C_{in}	—	15	pF	D3.24

NOTES:
1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.
2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.
3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200 Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3V	8	8	mA	D3.26

3.2.4 G2_LE Core PLL Electrical Characteristics

The internal clocking of the G2_LE core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. G2_LE PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
G2_LE frequency	f_{core}	1	50	—	550	MHz	O4.1
G2_LE cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
G2_LE VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
G2_LE input clock frequency	f_{XLB_CLK}		25	—	367	MHz	O4.4
G2_LE input clock cycle time	t_{XLB_CLK}		2.73	—	50.0	ns	O4.5
G2_LE input clock jitter	t_{jitter}	2	—	—	150	ps	O4.6
G2_LE PLL relock time	t_{lock}	3	—	—	100	µs	O4.7

NOTES:
1 The XLB_CLK frequency and G2_LE PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and G2_LE PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = -40 to 85 °C
- Tj = -40 to 115 °C
- VDD_CORE = 1.42 to 1.58 V
  VDD_IO = 3.0 to 3.6 V
- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

3.3.1 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	G2_LE Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

3.3.2 Clock AC Specifications

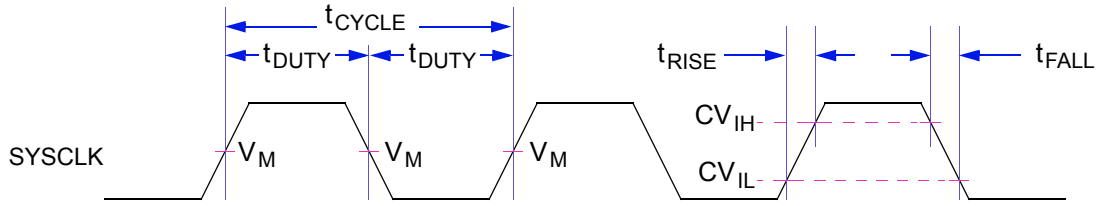
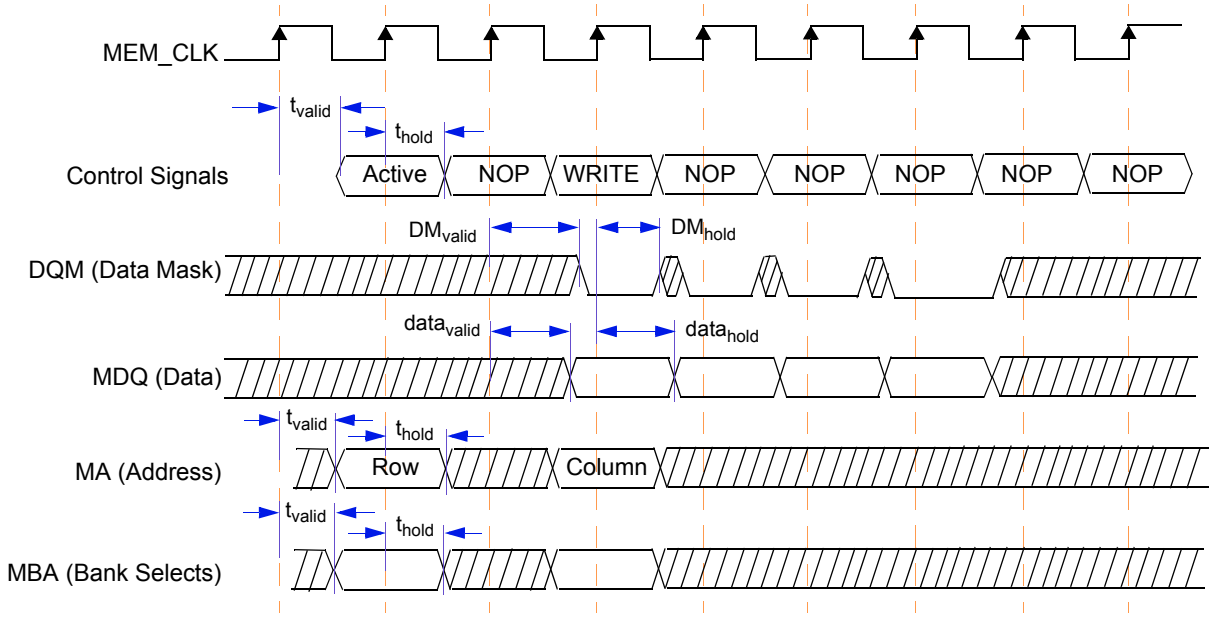


Figure 2. Timing Diagram—SYS_XTAL_IN

Table 19. Standard SDRAM Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.8
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.9
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.10
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.25+0.4	ns	A5.11
DM_{hold}	DQM hold after rising edge of Mem_clk	t_{mem_clk}*0.25-0.7	—	ns	A5.12
$data_{valid}$	MDQ valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.75+0.4	ns	A5.13
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	t_{mem_clk}*0.75-0.7	—	ns	A5.14



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 6. Timing Diagram—Standard SDRAM Memory Write Timing

3.3.5.3 Memory Interface Timing-DDR SDRAM Read Command

The SDRAM Memory Controller uses an internally skewed clock for reading DDR memory. The programmable bits in the Reset Configuration Register used to account for unknown board delays are in the CDM module. The internal read clock can be delayed up to 3 ns under worst operating conditions in 32 increments of 95 ps, (1.4 ns in 45 ps increments under best case operating conditions) by programming the CDM Reset Configuration Register tap delay bits. Note: These bits in the CDM Reset Configuration register are not ‘reset configured’ but have a hard coded reset value **and** are writable during operation.

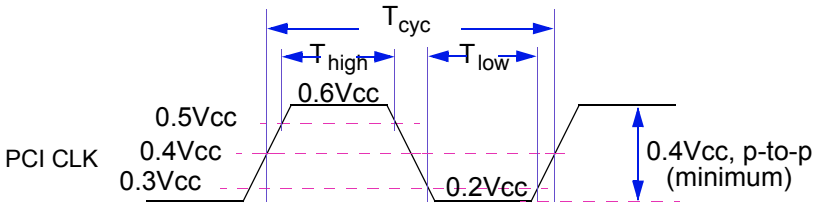


Figure 10. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
T_{cyc}	PCI CLK Cycle Time	15	30	30		ns	1,3	A6.1
T_{high}	PCI CLK High Time	6		11		ns		A6.2
t_{low}	PCI CLK Low Time	6						A6.3
-	PCI CLK Slew Rate	1.5	4	1	4	V/ns	2	A6.4

NOTES:
1. In general, all 66-MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 10.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
T_{val}	CLK to Signal Valid Delay - bused signals	2	6	2	11	ns	1,2,3	A6.5
T_{val}(ptp)	CLK to Signal Valid Delay - point to point	2	6	2	12	ns	1,2,3	A6.6
T_{on}	Float to Active Delay	2		2		ns	1	A6.7
T_{off}	Active to Float Delay		14		28	ns	1	A6.8
T_{su}	Input Setup Time to CLK - bused signals	3		7		ns	3,4	A6.9
T_{su}(ptp)	Input Setup Time to CLK - point to point	5		10,12		ns	3,4	A6.10
T_{h}	Input Hold Time from CLK	0		0		ns	4	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification [4]. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.
2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification [4].
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification [4].

For Measurement and Test Conditions, see the PCI Local Bus Specification [4].

3.3.7 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200. Maximum eight configurable Chip-selects are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:
WS = Wait State
DC = Dead Cycle
LB = Long Burst
DS = Data size in Byte
tPCIck = PCI clock period
tIPBIck = IPBI clock period

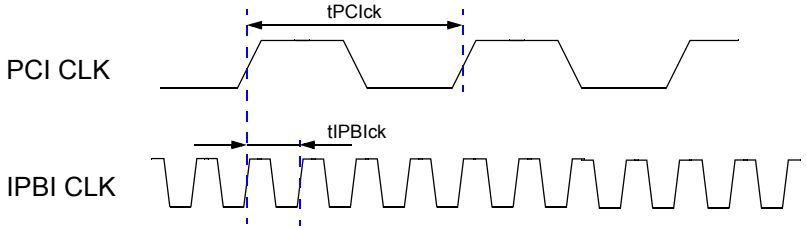


Figure 11. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

3.3.7.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.1
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.2
t_1	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns	1	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	-	ns	2	A7.5
t_4	OE assertion before CS assertion	-	0.4	ns		A7.6
t_5	OE negation before CS negation	-	0.4	ns		A7.7
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.8
t_7	RW hold after CS negation	t_{IPBIck}	-	ns		A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	-	ns		A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	-	ns		A7.11
t_{10}	DATA input setup before CS negation	2.8	-	ns		A7.12
t_{11}	DATA input hold after CS negation	0	(DC+1)*t_{PCIck}	ns		A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	-	ns	3	A7.14
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	3	A7.15

Table 24. Non-MUXed Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_{14}	TS assertion before CS assertion	-	0.8	ns	4	A7.16
t_{15}	TS pulse width	t_{PClck}	t_{PClck}	ns	4	A7.17
t_{16}	TSIZ valid before CS assertion	t_{IPBIck}	-	ns	5	A7.18
t_{17}	TSIZ hold after CS negation	t_{IPBIck}	-	ns	5	A7.19

NOTES:
1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0 - 65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause that the address is changing earlier as CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.

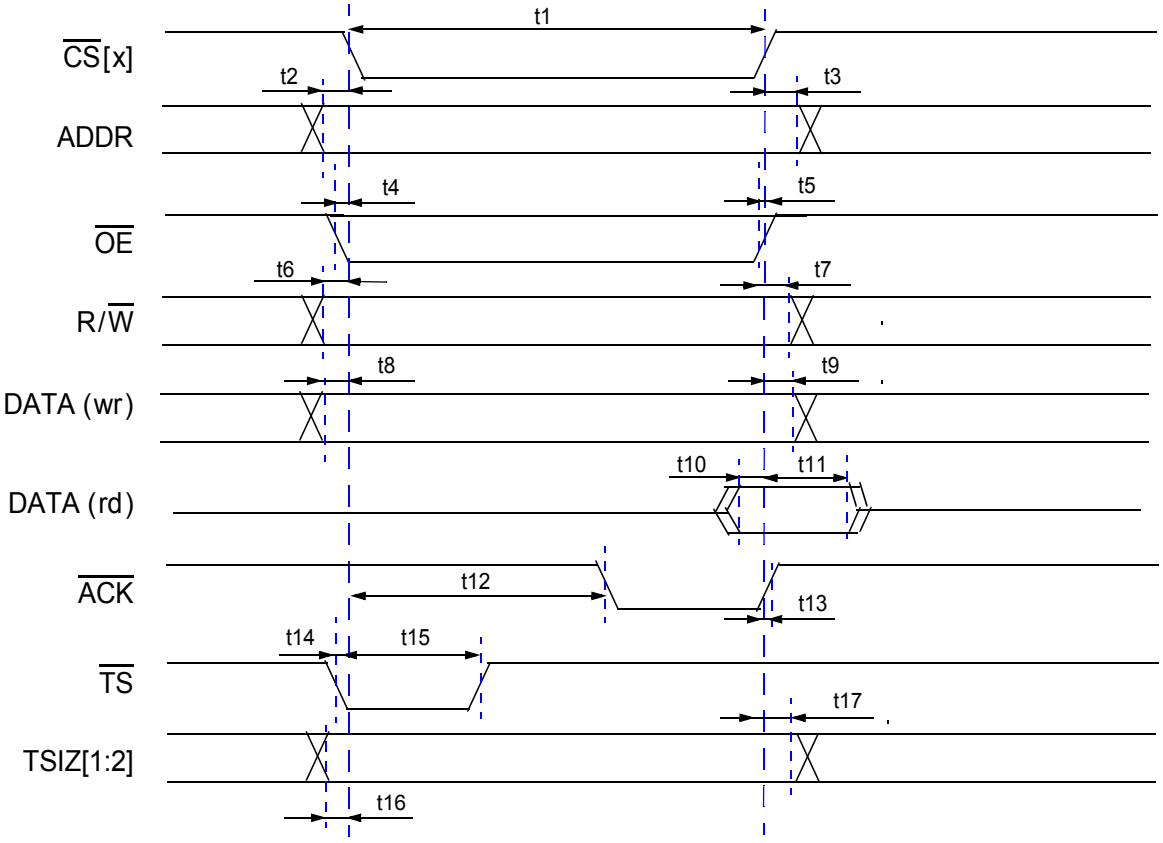


Figure 12. Timing Diagram—Non-MUXed Mode

3.3.7.3 MUXed Mode

Table 26. MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.15
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.16
t_{ALEA}	PCI CLK to ALE assertion	-	1	ns		A7.16
t_1	ALE assertion before Address, Bank, TSIZ assertion	-	0.8	ns		A7.17
t_2	CS assertion before Address, Bank, TSIZ negation	-	0.7	ns		A7.18
t_3	CS assertion before Data wr valid	-	0.7	ns		A7.19
t_4	Data wr hold after CS negation	t_{IPBIck}	-	ns		A7.20
t_5	Data rd setup before CS negation	2.8	-	ns		A7.21
t_6	Data rd hold after CS negation	0	(DC+1)*t_{PCIck}	ns	1	A7.22
t_7	ALE pulse width	-	t_{PCIck}	ns		A7.23
t_{TSA}	CS assertion after TS assertion	-	0.8	ns		A7.24
t_8	TS pulse width	-	t_{PCIck}	ns		A7.24
t_9	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns		A7.25
t_{OEA}	OE assertion before CS assertion	-	0.4	ns		A7.26
t_{OEN}	OE negation before CS negation	-	0.4	ns		A7.27
t_{10}	RW assertion before ALE assertion	t_{IPBIck}	-	ns		A7.26
t_{11}	RW negation after CS negation	-	t_{PCIck}	ns		A7.27
t_{12}	ACK assertion after CS assertion	t_{IPBIck}	-	ns	2	A7.28
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	2	A7.28

Note:
1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified 0 - 65535.
2. ACK is input and can be used to shorten the CS pulse width.

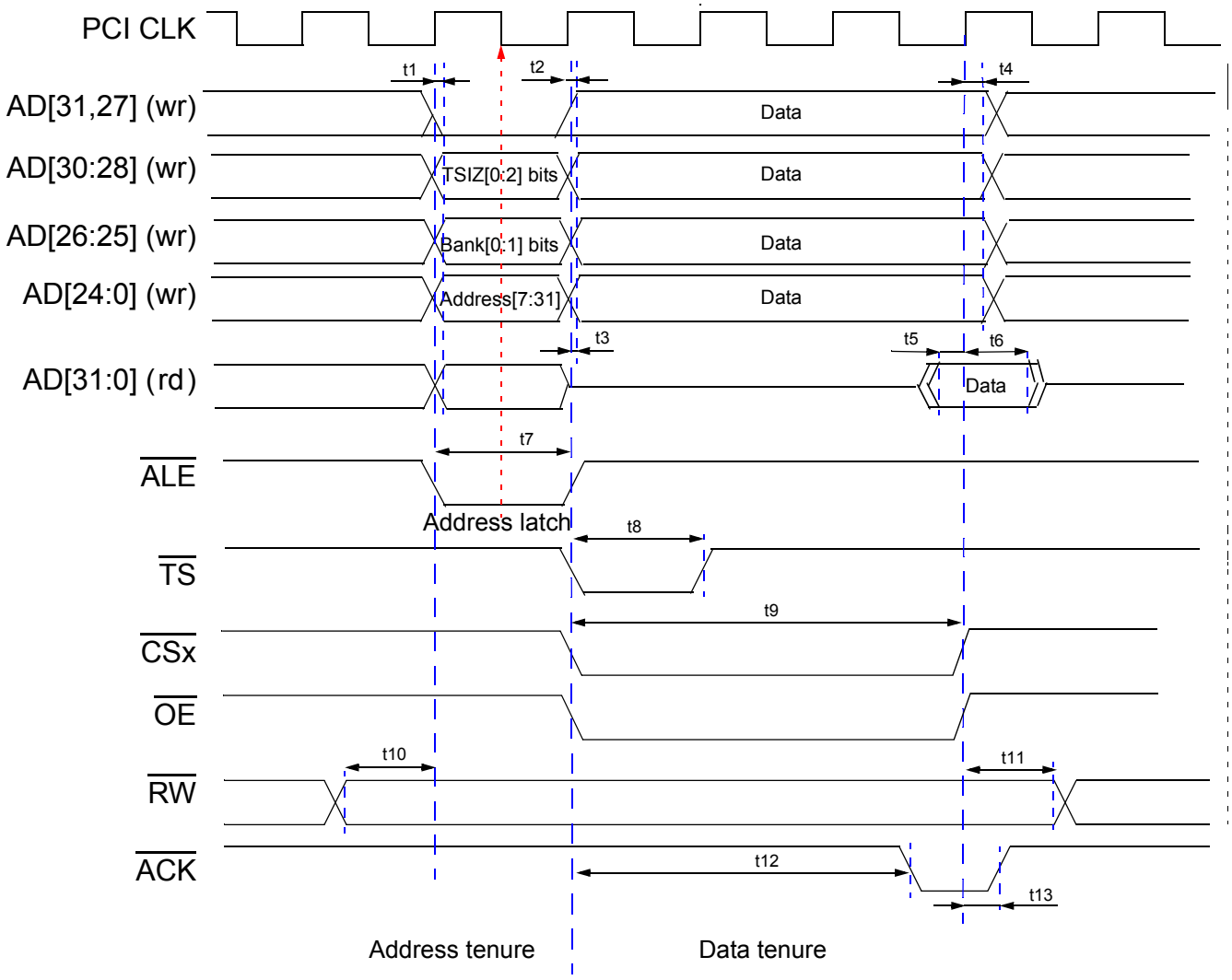


Figure 14. Timing Diagram—MUXed Mode

3.3.8 ATA

The MPC5200 ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nano seconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification [5] and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the MPC5200 User Manual [1].

The MPC5200 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5200 operating frequency (IP bus clock frequency)
- Internal MPC5200 bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5200. See the MPC5200 User Manual [1].

NOTE

All output timing numbers are specified for nominal 50 pF loads.

Table 27. PIO Mode Timing Specifications

	PIO Timing Parameter	Min/Max (ns)	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	SpecID
t0	Cycle Time	min	600	383	240	180	120	A8.1
t1	Address valid to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	70	50	30	30	25	A8.2
t2	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width 16-bit 8-bit	min min	165 290	125 290	100 290	80 80	70 70	A8.3
t2i	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ recovery time	min	—	—	—	70	25	A8.4
t3	$\overline{\text{DIOW}}$ data setup	min	60	45	30	30	20	A8.5
t4	$\overline{\text{DIOW}}$ data hold	min	30	20	15	10	10	A8.6
t5	$\overline{\text{DIOR}}$ data setup	min	50	35	20	20	20	A8.7
t6	$\overline{\text{DIOR}}$ data hold	min	5	5	5	5	5	A8.8
t9	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to address valid hold	min	20	15	10	10	10	A8.9
tA	IORDY setup	max	35	35	35	35	35	A8.10
tB	IORDY pulse width	max	1250	1250	1250	1250	1250	A8.11

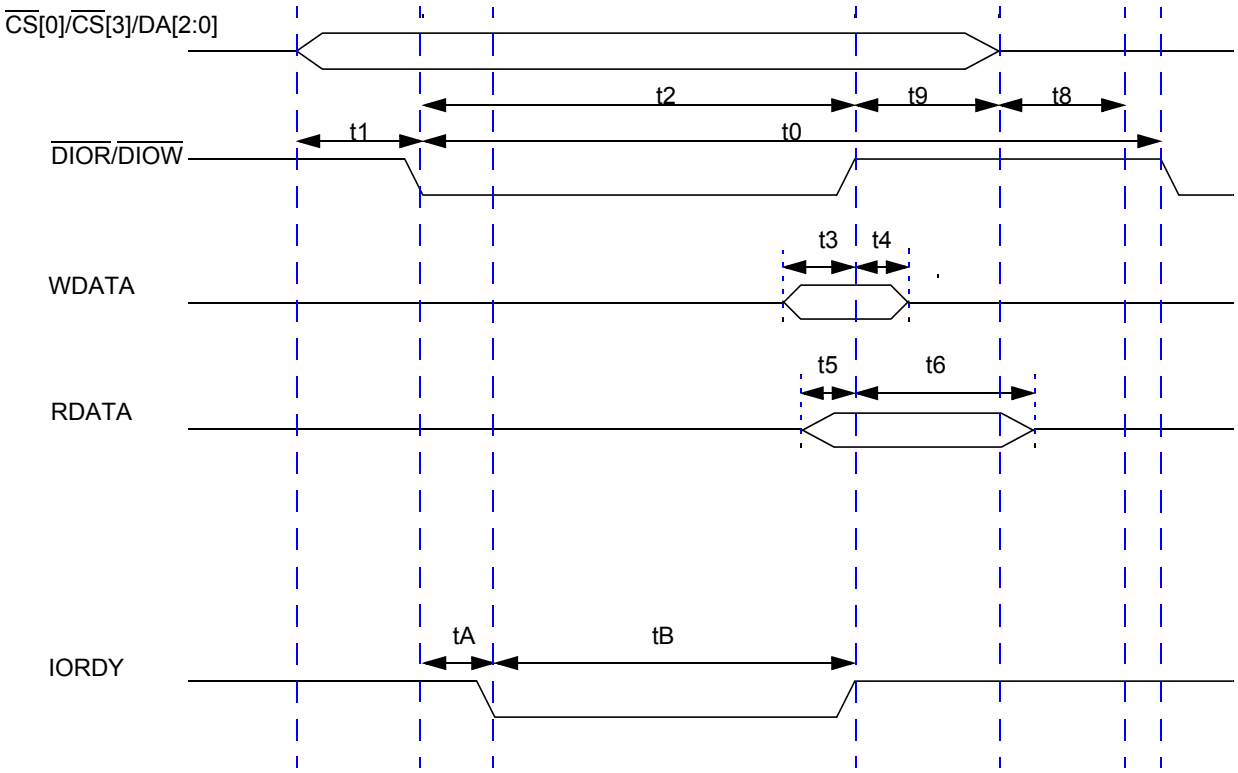


Figure 15. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

	Multiword DMA Timing Parameters	Min/Max	Mode 0(ns)	Mode 1(ns)	Mode 2(ns)	SpecID
t0	Cycle Time	min	480	150	120	A8.12
tC	$\overline{\text{DMACK}}$ to DMARQ delay	max	—	—	—	A8.13
tD	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width (16-bit)	min	215	80	70	A8.14
tE	$\overline{\text{DIOR}}$ data access	max	150	60	50	A8.15
tG	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ data setup	min	100	30	20	A8.16
tF	$\overline{\text{DIOR}}$ data hold	min	5	5	5	A8.17
tH	$\overline{\text{DIOW}}$ data hold	min	20	15	10	A8.18
tI	DMACK to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	0	0	0	A8.19
tJ	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to $\overline{\text{DMACK}}$ hold	min	20	5	5	A8.20
tKr	$\overline{\text{DIOR}}$ negated pulse width	min	50	50	25	A8.21
tKw	$\overline{\text{DIOW}}$ negated pulse width	min	215	50	25	A8.22
tLr	$\overline{\text{DIOR}}$ to DMARQ delay	max	120	40	35	A8.23
tLw	$\overline{\text{DIOW}}$ to DMARQ delay	max	40	40	35	A8.24

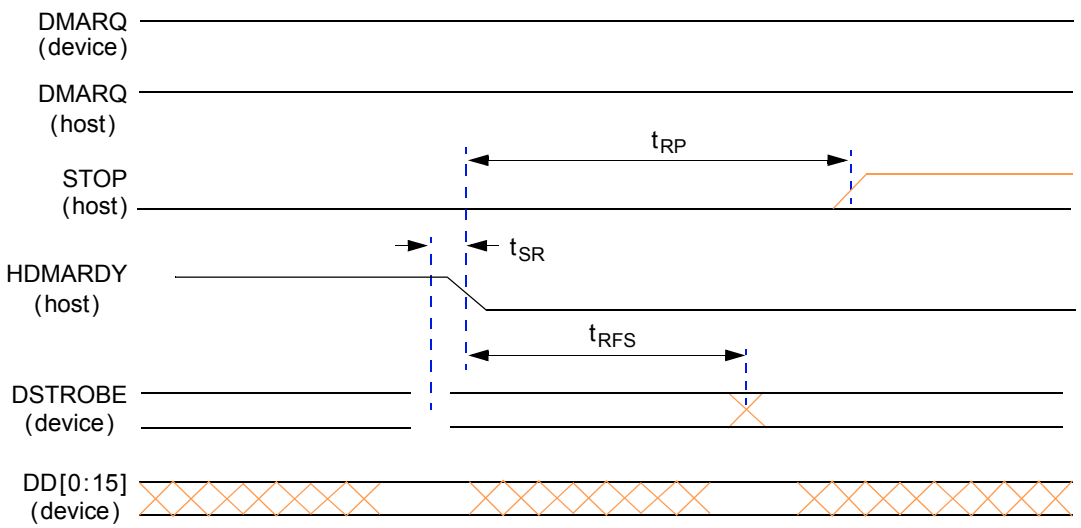


Figure 19. Timing Diagram—Host Pausing an Ultra DMA Data In Burst

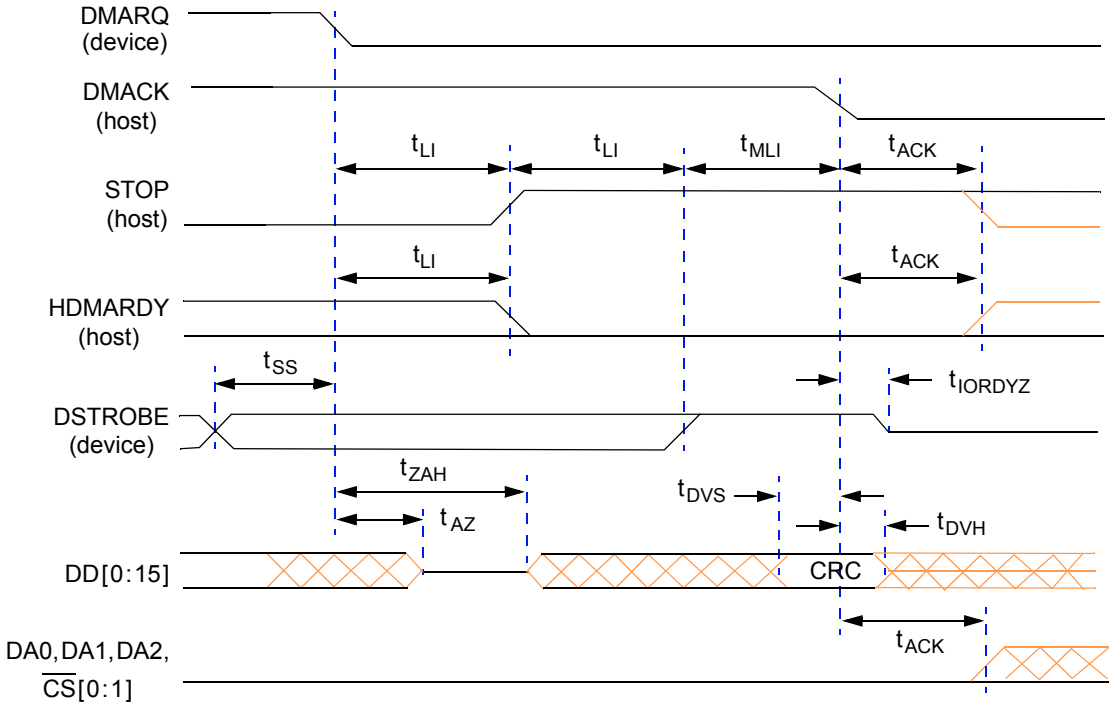


Figure 20. Timing Diagram—Drive Terminating Ultra DMA Data In Burst

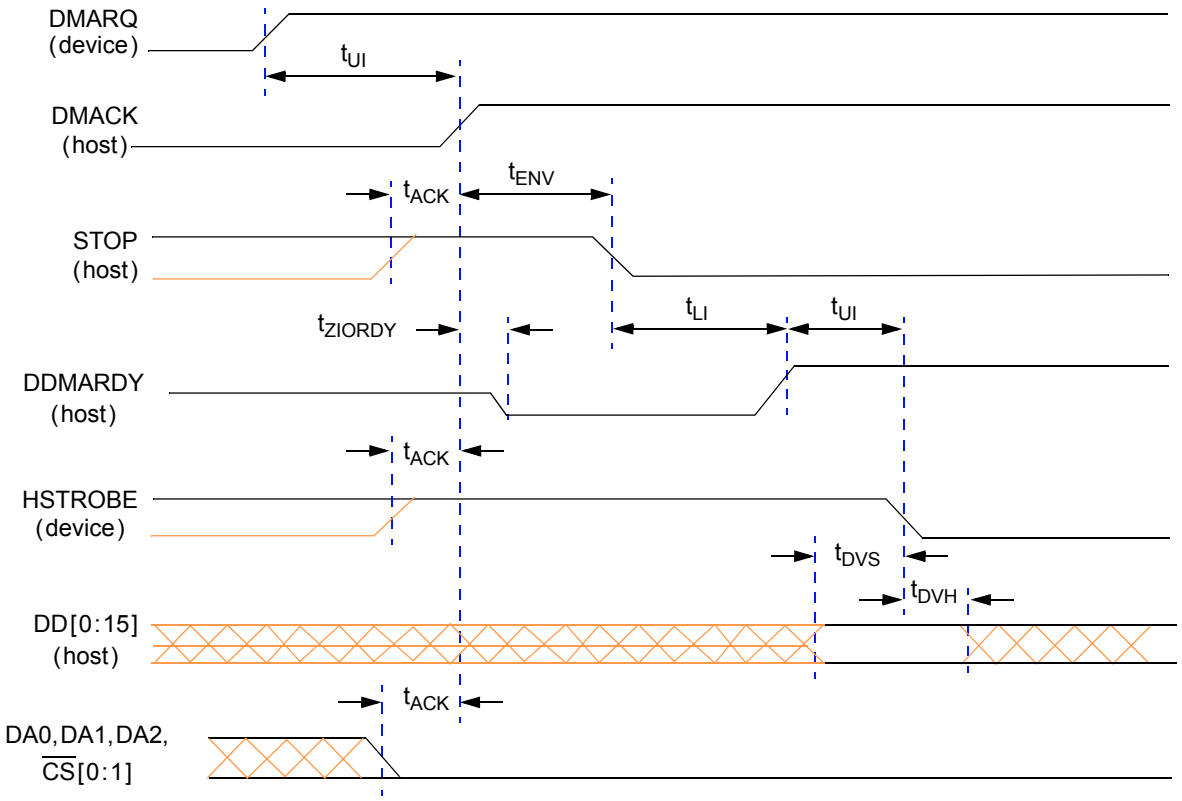


Figure 22. Timing Diagram—Initiating an Ultra DMA Data Out Burst

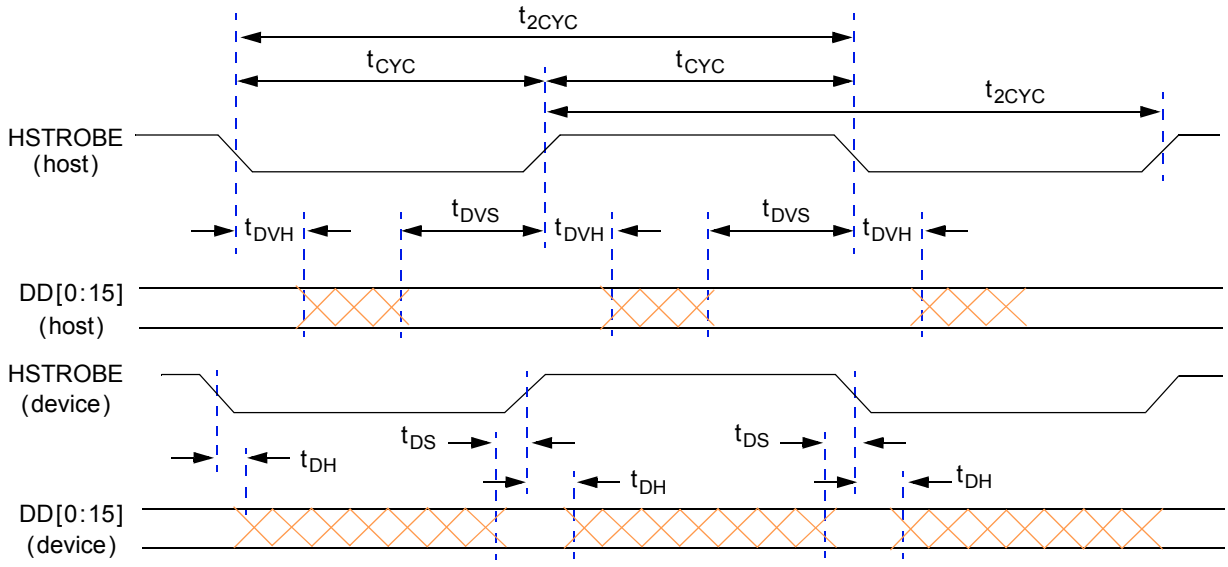


Figure 23. Timing Diagram—Sustained Ultra DMA Data Out Burst

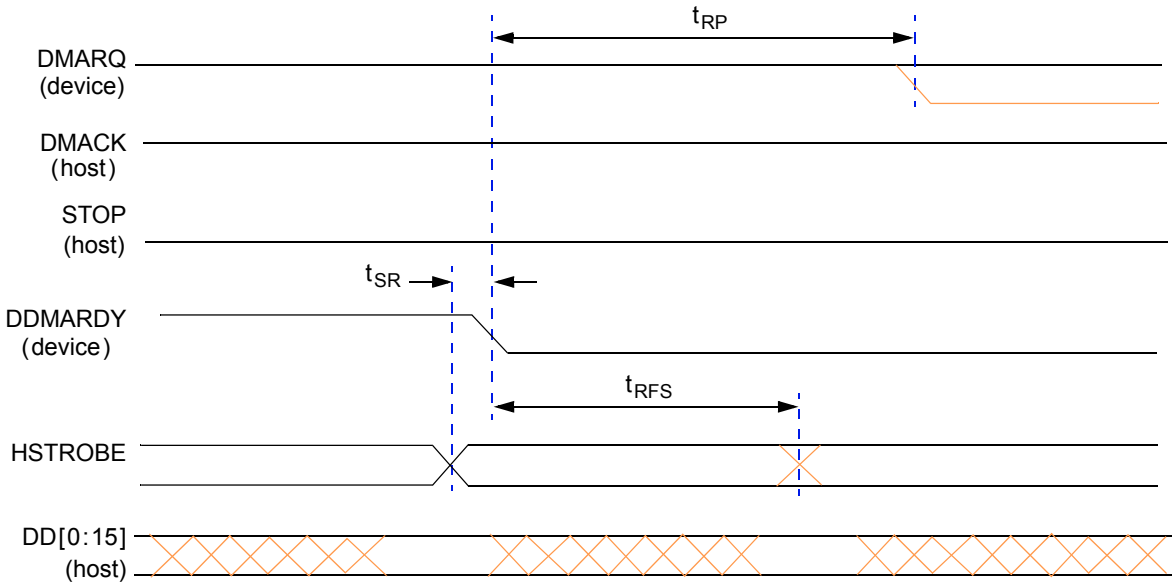


Figure 24. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

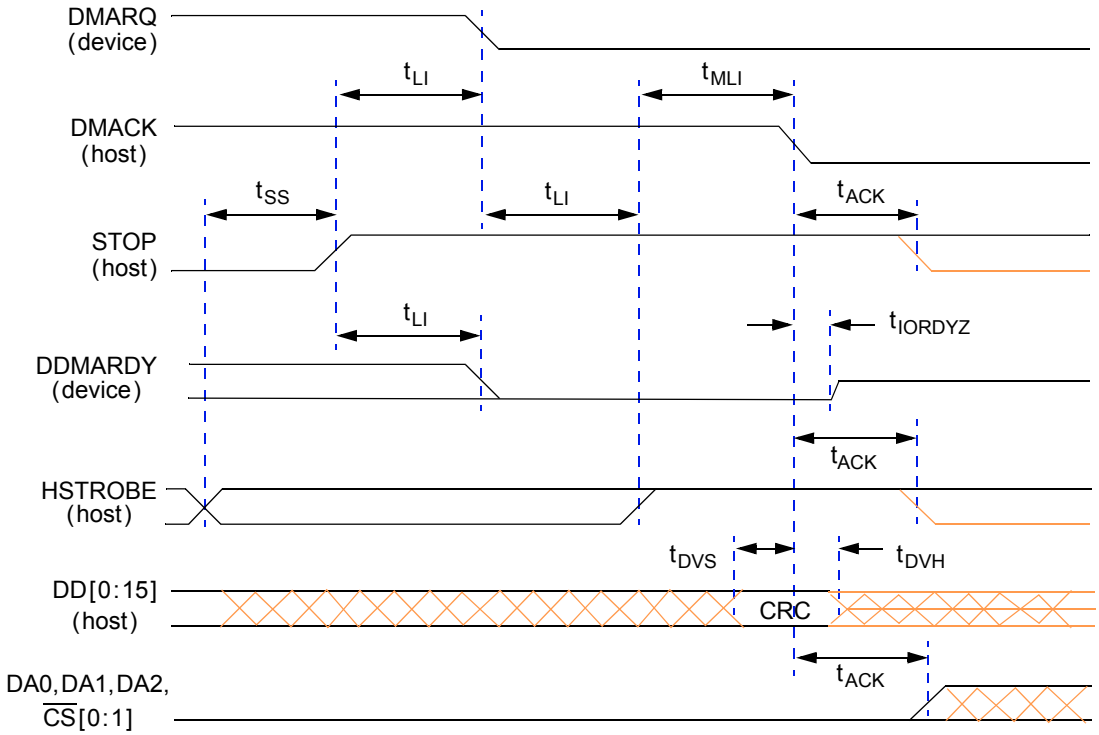


Figure 25. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

Table 32. MII Tx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
M5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER Delay	0	25	ns	A9.5
M6	TX_CLK pulse width high	35%	65%	TX_CLK Period[1]	A9.6
M7	TX_CLK pulse width low	35%	65%	TX_CLK Period(1)	A9.7

NOTES:
1 the TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification [6].

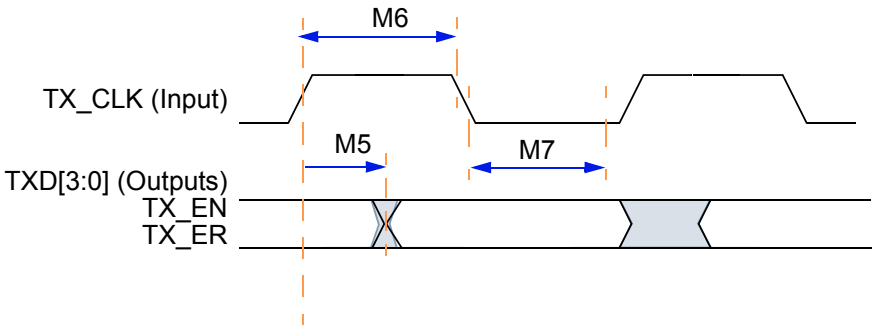


Figure 29. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

Sym	Description	Min	Max	Unit	SpecID
M8	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A9.8

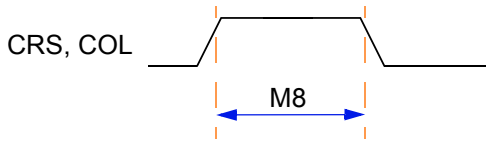


Figure 30. Ethernet Timing Diagram—MII Async

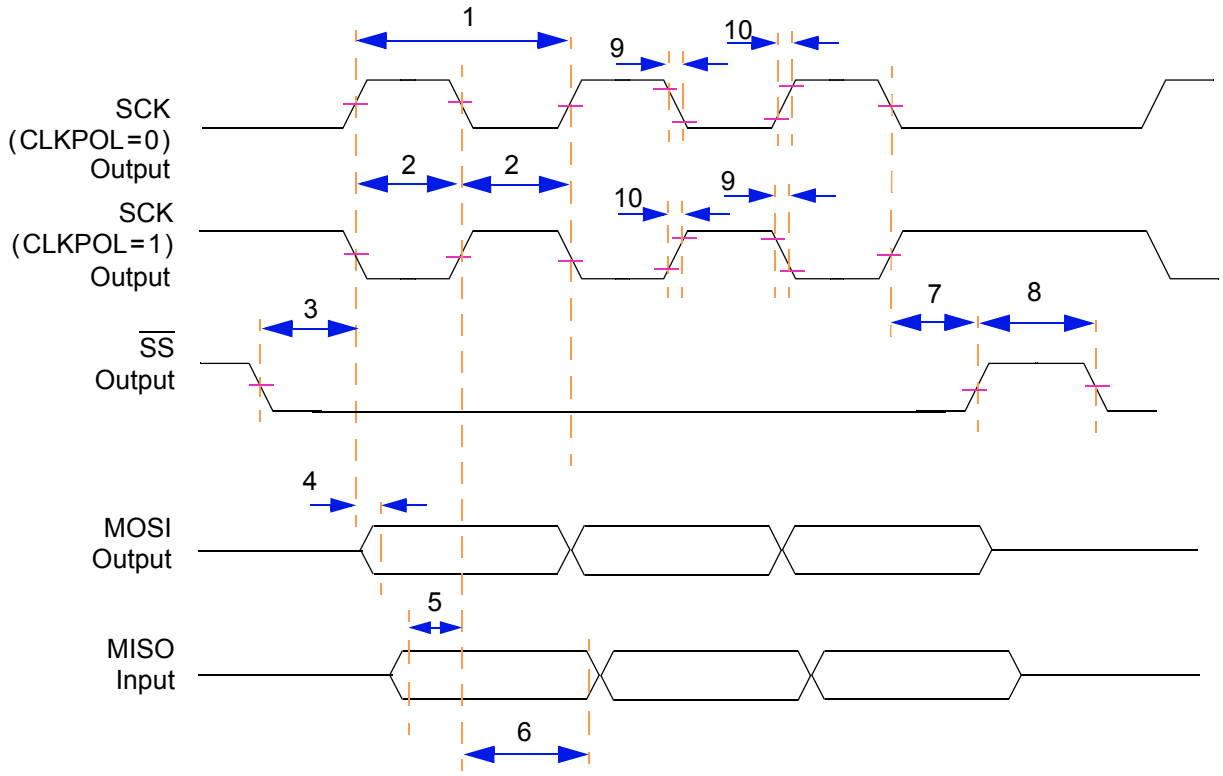


Figure 35. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 39. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.31
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.32
3	Slave select clock delay	15.0	—	ns	A11.33
4	Output data valid	—	50.0	ns	A11.34
5	Input Data setup time	50.0	—	ns	A11.35
6	Input Data hold time	0.0	—	ns	A11.36
7	Slave disable lag time	15.0	—	ns	A11.37
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.38

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

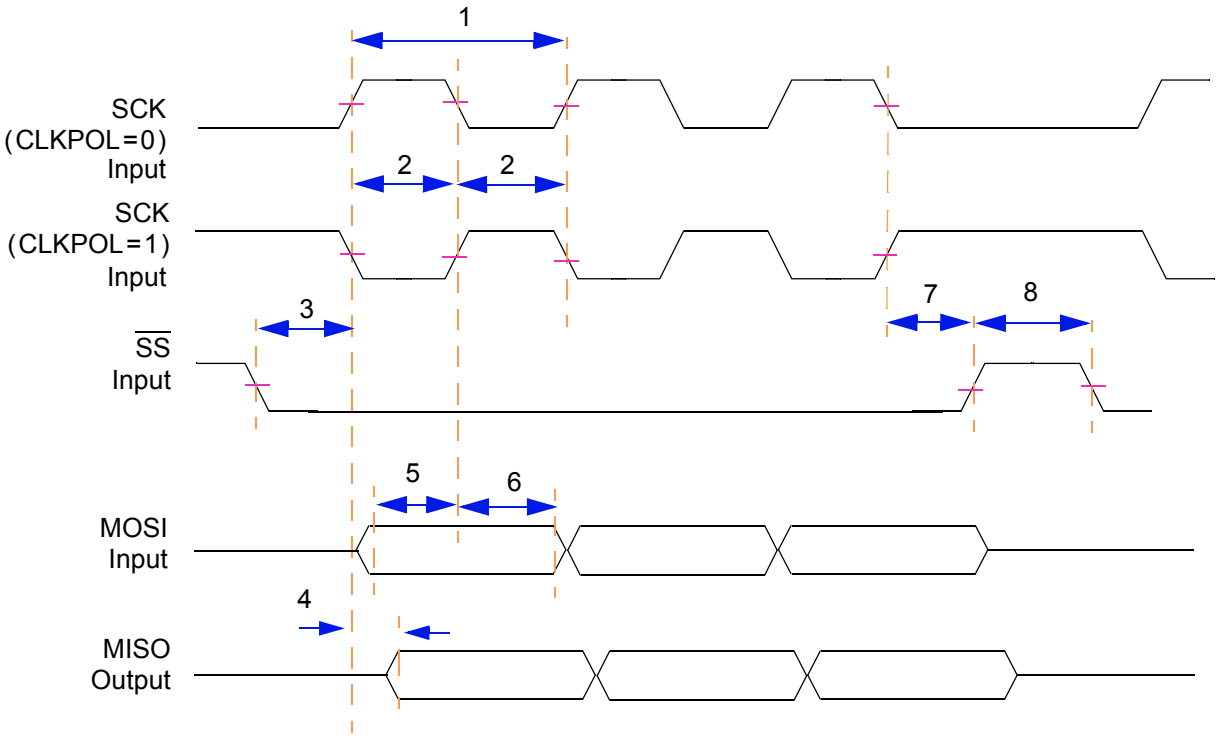


Figure 36. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

3.3.12 MSCAN

The CAN functions are available as RX and TX pins at normal IO pads (I^2C1+GPTimer or PSC2). There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.13 I^2C

Table 40. I^2C Input Timing Specifications—SCL and SDA

Sym	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A13.1
2	Clock low period	8	—	IP-Bus Cycle[1]	A13.2
4	Data hold time	0.0	—	ns	A13.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A13.4
7	Data setup time	0.0	—	ns	A13.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A13.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A13.7

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

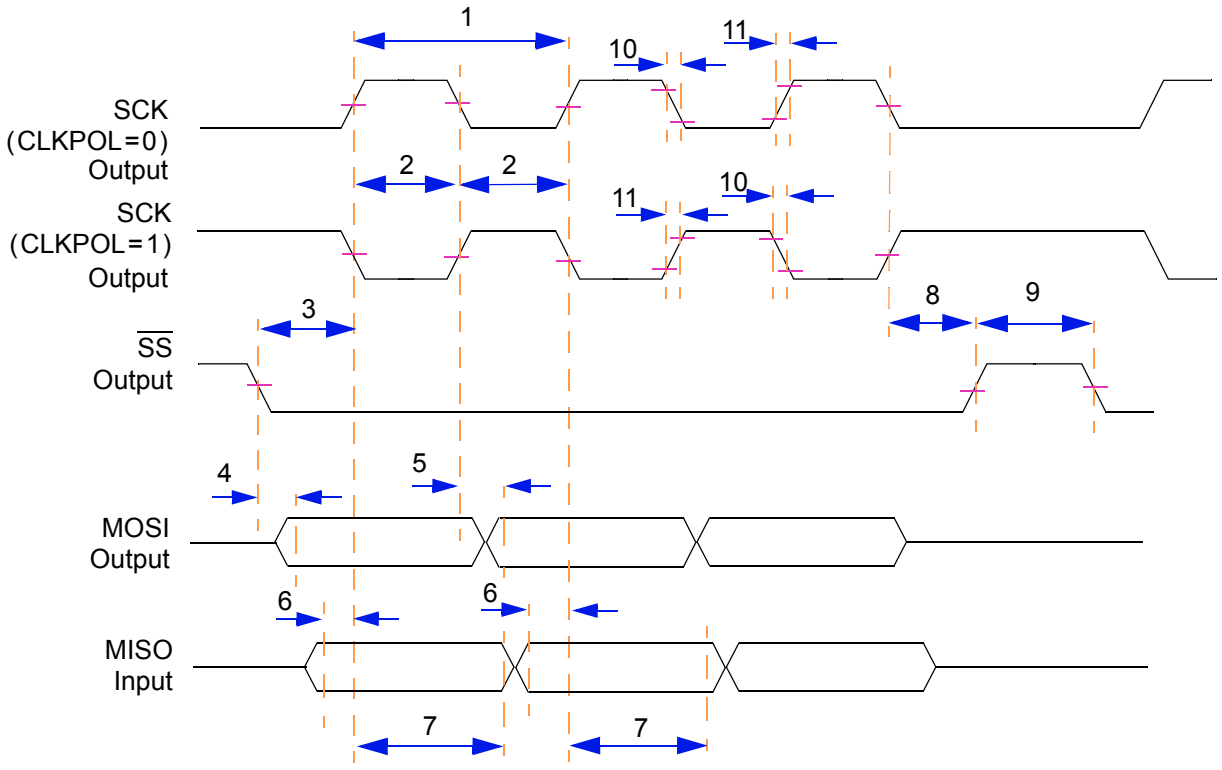


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

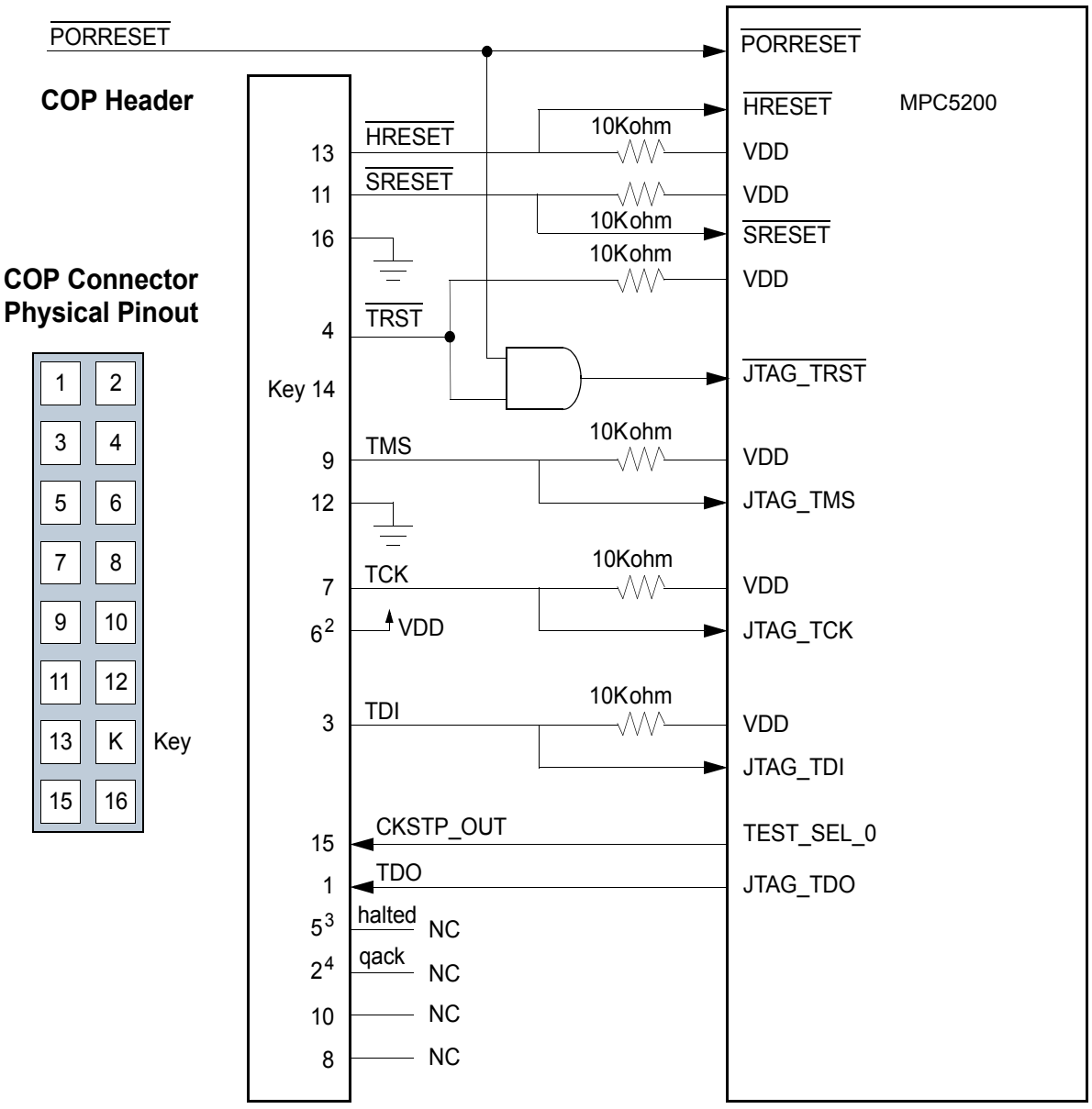


Figure 55. COP Connector Diagram