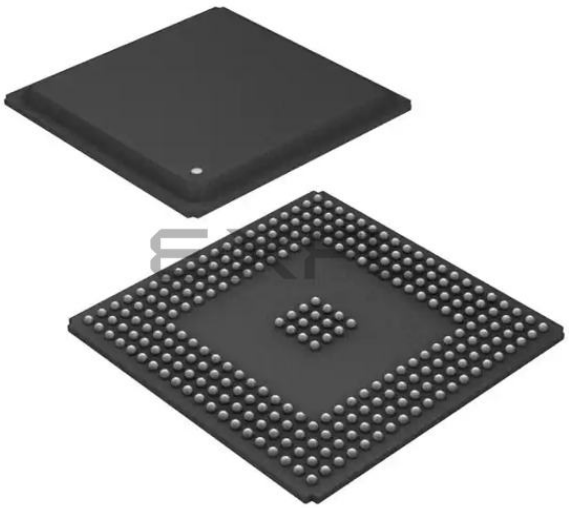

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5200cbv266

3 Electrical and Thermal Characteristics

3.1 DC Electrical Characteristics

3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200 DC Electrical characteristics. Table 1 gives the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Min	Max	Unit	SpecID
Supply voltage - G2_LE core and peripheral logic	VDD_CORE	–0.3	1.8	V	D1.1
Supply voltage - I/O buffers	VDD_IO, VDD_MEM_IO	–0.3	3.6	V	D1.2
Supply voltage - System APLL	SYS_PLL_AVDD	–0.3	2.1	V	D1.3
Supply voltage - G2_LE APLL	CORE_PLL_AVDD	–0.3	2.1	V	D1.4
Input voltage (VDD_IO)	Vin	–0.3	VDD_IO + 0.3	V	D1.5
Input voltage (VDD_MEM_IO)	Vin	–0.3	VDD_MEM_IO + 0.3	V	D1.6
Input voltage overshoot	Vinos	–	1.0	V	D1.7
Input voltage undershoot	Vinus	–	1.0	V	D1.8
Storage temperature range	Tstg	–55	150	°C	D1.9

NOTES:
1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

3.1.2 Recommended Operating Conditions

Table 2 gives the recommended operating conditions.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min[1]	Max[(1)]	Unit	SpecID
Supply voltage - G2_LE core and peripheral logic	VDD_CORE	1.42	1.58	V	D2.1
Supply voltage - standard I/O buffers	VDD_IO	3.0	3.6	V	D2.2
Supply voltage - memory I/O buffers (SDR)	$VDD\_MEM\_IO_{SDR}$	3.0	3.6	V	D2.3
Supply voltage - memory I/O buffers (DDR)	$VDD\_MEM\_IO_{DDR}$	2.42	2.63	V	D2.4
Supply voltage - System APLL	SYS_PLL_AVDD	1.42	1.58	V	D2.5
Supply voltage - G2_LE APLL	CORE_PLL_AVDD	1.42	1.58	V	D2.6
Input voltage - standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage - memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Min[1]	Max[(1)]	Unit	SpecID
Input voltage - memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	-40	+85	°C	D2.10
Extended ambient operating temperature range[3]	T_{Aext}	-40	+105	°C	D2.11
Die junction operating temperature range	Tj	-40	+115	°C	D2.12
Extended die junction operating temperature range	Tjext	-40	+125	°C	D2.13

NOTES:
1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.
2 Maximum G2_LE core operating frequency is 400 MHz
3 Maximum G2_LE core operating frequency is 264 MHz

3.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200 at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12

Table 4. Drive Capability of MPC5200 Output Pins (continued)

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV8_OD	VDD_IO = 3.3V	-	8	mA	D3.27
DRV16_MEM	VDD_IO_MEM = 3.3V	16	16	mA	D3.28
DRV16_MEM	VDD_IO_MEM = 2.5V	16	16	mA	D3.29
PCI	VDD_IO = 3.3V	16	16	mA	D3.30

3.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (i.e., either GND or V_{CC}). Table 7 gives package thermal characteristics for this device.

Table 5. ESD and Latch-Up Protection Characteristics

Sym	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM)—JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM)—JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM)—JEDEC JESD22-C101	500	—	V	D4.3
I_{LAT}	Latch-up Current at T_A=85°C positive negative	 +100 -100	—	mA	D4.4
I_{LAT}	Latch-up Current at T_A=27°C positive negative	 +200 -200	—	mA	D4.5

3.1.5 Power Dissipation

Power dissipation of the MPC5200 is caused by 3 different components: the dissipation of the internal or core digital logic (supplied by VDD_CORE), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD) and the dissipation of the IO logic (supplied by VDD_IO_MEM and VDD_IO). Table 6 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated by the user for each application case using the following formula

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200 processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{\text{analog}} + P_{IO}$$

Table 6. Power Dissipation

Core Power Supply (VDD_CORE)					
Mode	SYS_XTAL/XLB/PCI/IPG/CORE (MHz)		Unit	Notes	SpecID
	33/66/33/33/264	33/132/66/132/396			
	Typ	Typ			
Operational	727.5	1080	mW	[1],[2]	D5.1
Doze	—	600	mW	[1],[3]	D5.2
Nap	—	225	mW	[1],[4]	D5.3
Sleep	—	225	mW	[1],[5]	D5.4
Deep-Sleep	52.5	52.5	mW	[1],[6]	D5.5
PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)					
Mode	**Typ**		**Unit**	**Notes**	
Typical	2		mW	[7]	D5.6
Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8])					
Mode	**Typ**		**Unit**	**Notes**	
Typical	33		mW	[9]	D5.7

NOTES:
1. Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 C
2. Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.
3. Doze power is measured with the G2_LE core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive
4. Nap power is measured with the G2_LE core in Nap mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
5. Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
6. Deep-Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL, Core PLL and all other system modules are inactive
7. Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 C
8. IO power figures given in the table represent the worst case scenario. For the mem_io rail connected to 2.5V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3V.
9. Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD\_MEM\_IO_{SDR}$= 3.3 V, Tj = 25 C

3.2.4 G2_LE Core PLL Electrical Characteristics

The internal clocking of the G2_LE core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. G2_LE PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
G2_LE frequency	f_{core}	1	50	—	550	MHz	O4.1
G2_LE cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
G2_LE VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
G2_LE input clock frequency	f_{XLB_CLK}		25	—	367	MHz	O4.4
G2_LE input clock cycle time	t_{XLB_CLK}		2.73	—	50.0	ns	O4.5
G2_LE input clock jitter	t_{jitter}	2	—	—	150	ps	O4.6
G2_LE PLL relock time	t_{lock}	3	—	—	100	µs	O4.7

NOTES:
1 The XLB_CLK frequency and G2_LE PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and G2_LE PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

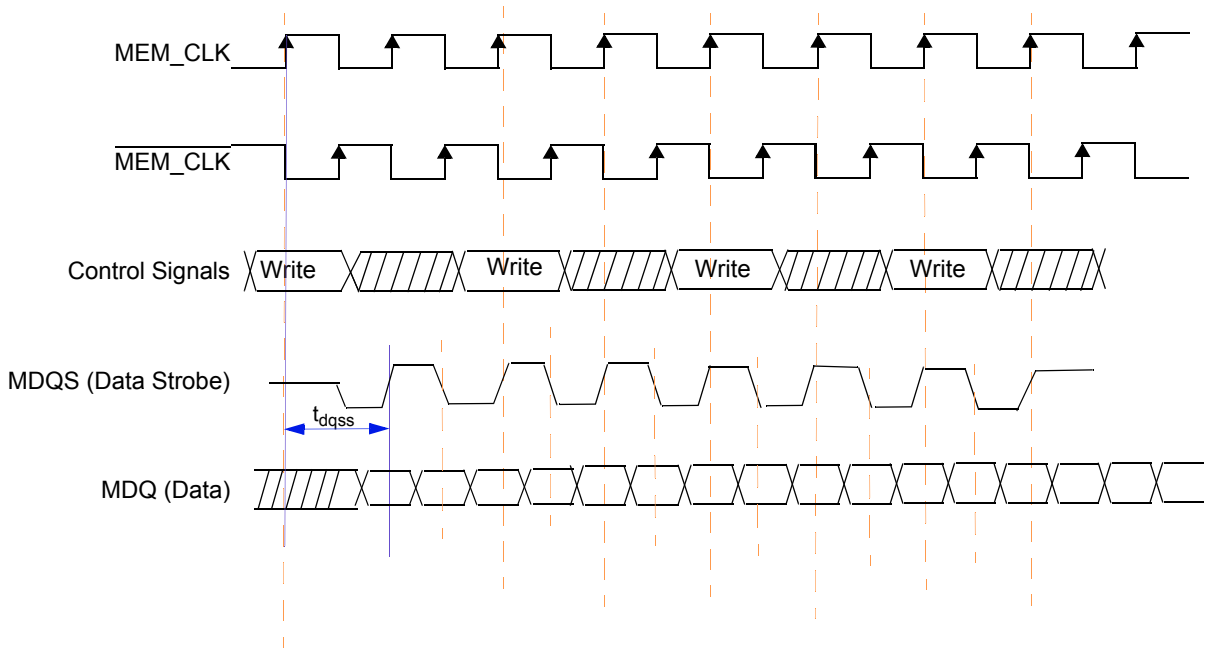
AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

3.3.5.4 Memory Interface Timing-DDR SDRAM Write Command

Table 21. DDR SDRAM Memory Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.20
t_{DQSS}	Delay from write command to first rising edge of MDQS	—	t_{mem_clk}+0.4	ns	A5.21



NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 9. DDR SDRAM Memory Write Timing

3.3.6 PCI

The PCI interface on the MPC5200 is designed to PCI Version 2.2 and supports 33-MHz and 66-MHz PCI operations. See the PCI Local Bus Specification [4]; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

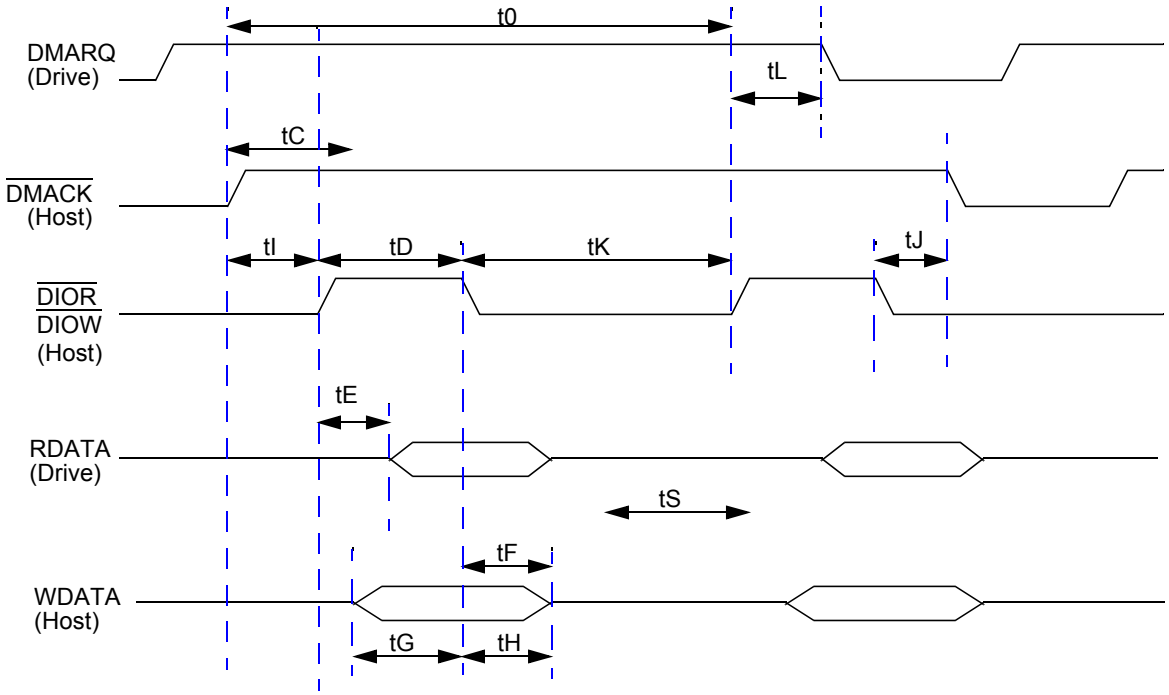
The MPC5200 is always the source of the PCI CLK. The clock waveform must be delivered to each 33-MHz or 66-MHz PCI component in the system. Figure 10 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.

3.3.7.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.20
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.21
t_1	CS pulse width	$(1+WS+4^{LB}*2*(32/DS))*t_{PCIck}$	$(1+WS+4^{LB}*2*(32/DS))*t_{PCIck}$	ns	1,2	A7.22
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.23
t_3	ADDR hold after CS negation	-	-0.7	ns		A7.24
t_4	OE assertion before CS assertion	-	0.4	ns		A7.25
t_5	OE negation before CS negation	-	0.4	ns		A7.26
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.27
t_7	RW hold after CS negation	t_{PCIck}	-	ns		A7.28
t_8	DATA setup before rising edge of PCI	1.8	-	ns		A7.29
t_9	DATA hold after rising edge of PCI	0	-	ns		A7.30
t_{10}	DATA hold after CS negation	0	$(DC+1)*t_{PCIck}$	ns		A7.31
t_{11}	ACK assertion after CS assertion	-	$(WS+1)*t_{PCIck}$	ns		A7.32
t_{12}	ACK negation before CS negation	-	0.6	ns	3	A7.33
t_{13}	ACK pulse width	$4^{LB}*2*(32/DS)*t_{PCIck}$	$4^{LB}*2*(32/DS)*t_{PCIck}$	ns	2,3	A7.34
t_{14}	CS assertion after TS assertion	-	0.8	ns		A7.35
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns		A7.36

NOTES:
1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified 0 - 65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => $4^1*2*(32/8) = 32$ => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1+10+32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.



NOTE: The direction of signal assertion is towards the top of the page, and the direction of negation is towards the bottom of the page, irrespective of the electrical properties of the signal.

Figure 16. Multiword DMA Timing

Table 29. Ultra DMA Timing Specification

Name	MODE 0 (ns)		MODE 1 (ns)		MODE 2 (ns)		Comment	SpecID
	Min	Max	Min	Max	Min	Max		
$(t)_{2CYC}$	240	—	160	—	120	—	Typical sustained average two cycle time. For information only, do not test.	A8.26
$(t)_{CYC}$	114	—	75	—	55	—	Cycle time allowing for asymmetry and clock variations from STROBE edge to STROBE edge	A8.27
$(t)_{2CYC}$	235	—	156	—	117	—	Two-cycle time allowing for clock variations, from rising edge to next rising edge or from falling edge to next falling edge of STROBE.	A8.28
$(t)_{DS}$	15	—	10	—	7	—	Data setup time at recipient.	A8.29
$(t)_{DH}$	5	—	5	—	5	—	Data hold time at recipient.	A8.30
$(t)_{DVS}$	70	—	48	—	34	—	Data valid setup time at sender, to STROBE edge.	A8.31
$(t)_{DVH}$	6	—	6	—	6	—	Data valid hold time at sender, from STROBE edge.	A8.32
$(t)_{FS}$	0	230	0	200	0	170	First STROBE time for drive to first negate DSTROBE from STOP during a data-in burst.	A8.33

Table 29. Ultra DMA Timing Specification (continued)

Name	MODE 0 (ns)		MODE 1 (ns)		MODE 2 (ns)		Comment	SpecID
	Min	Max	Min	Max	Min	Max		
$(t)_{LI}$	0	150	0	150	0	150	Limited Interlock time.[1,2]	A8.34
$(t)_{MLI}$	20	—	20	—	20	—	Interlock time with minimum.[1,2]	A8.35
$(t)_{UI}$	0	—	0	—	0	—	Unlimited interlock time. [1,2]	A8.36
$(t)_{AZ}$	—	10	—	10	—	10	Maximum time allowed for output drivers to release from being asserted or negated	A8.37
$(t)_{ZAH}$	20	—	20	—	20	—	Minimum delay time required for output drivers to assert or negate from released state	A8.38
$(t)_{ZAD}$	0	—	0	—	0	—		A8.39
$(t)_{ENV}$	20	70	20	70	20	70	Envelope time—from $\overline{\text{DMACK}}$ to STOP and $\overline{\text{HDMARDY}}$ during data out burst initiation.	A8.40
$(t)_{SR}$	—	50	—	30	—	20	STROBE to $\overline{\text{DMARDY}}$ time, if $\overline{\text{DMARDY}}$ is negated before this long after STROBE edge, the recipient receives no more than one additional data word.	A8.41
$(t)_{RFS}$	—	75	—	60	—	50	Ready-to-Final STROBE time—no STROBE edges are sent this long after negation of $\overline{\text{DMARDY}}$.	A8.42
$(t)_{RP}$	160	—	125	—	100	—	Ready-to-Pause time—the time recipient waits to initiate pause after negating $\overline{\text{DMARDY}}$.	A8.43
$(t)_{IORDYZ}$	—	20	—	20	—	20	Pull-up time before allowing IORDY to be released.	A8.44
$(t)_{ZIORDY}$	0	—	0	—	0	—	Minimum time drive waits before driving IORDY	A8.45
$(t)_{ACK}$	20	—	20	—	20	—	Setup and hold times for $\overline{\text{DMACK}}$, before assertion or negation.	A8.46
$(t)_{SS}$	50	—	50	—	50	—	Time from STROBE edge to negation of DMARQ or assertion of STOP, when sender terminates a burst.	A8.47

NOTES:

1 t_{UI}, t_{MLI}, t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks. That is, one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.
- t_{UI} is an unlimited interlock that has no maximum time value.
- t_{MLI} is a limited time-out that has a defined minimum.
- t_{LI} is a limited time-out that has a defined maximum.

2 All timing parameters are measured at the connector of the drive to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after negation of DMARDY. Both STROBE and DMARDY timing measurements are taken at the connector of the sender. Even though the sender stops generating STROBE edges, the receiver may receive additional STROBE edges due to propagation delays. All timing measurement switching points (low to high and high to low) are taken at 1.5 V.

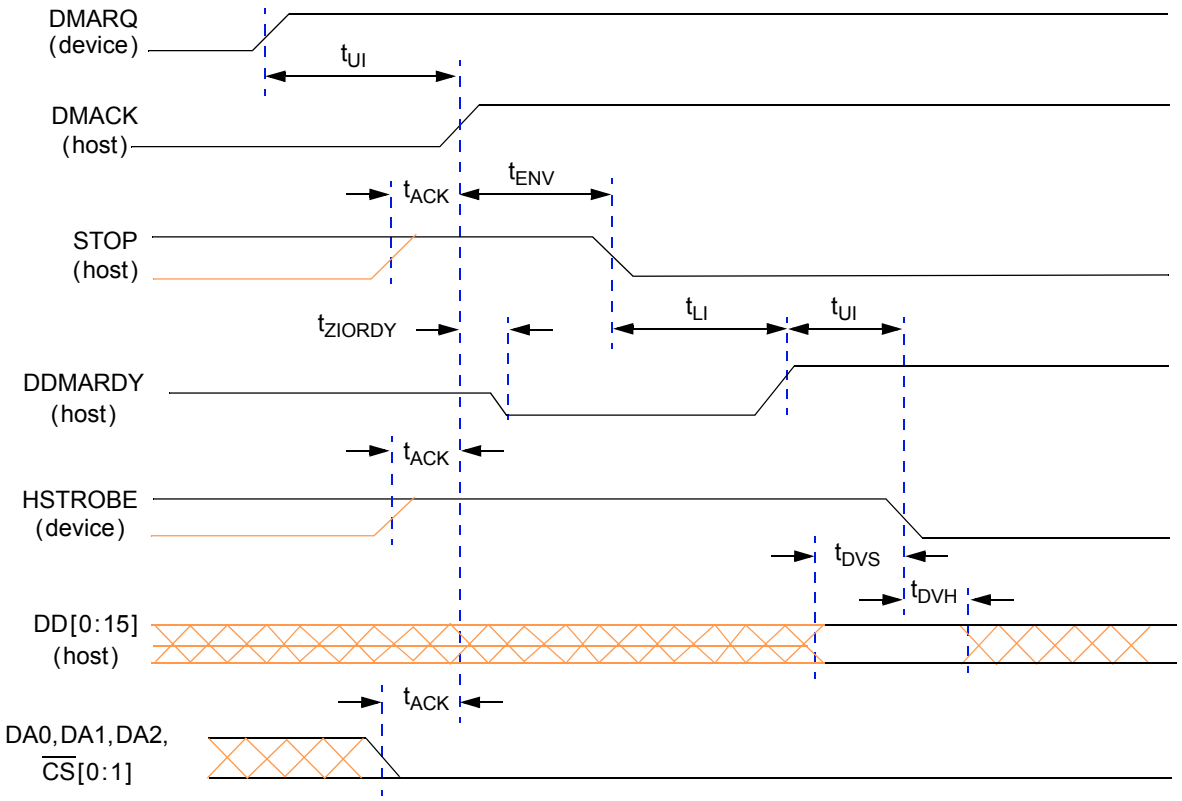


Figure 22. Timing Diagram—Initiating an Ultra DMA Data Out Burst

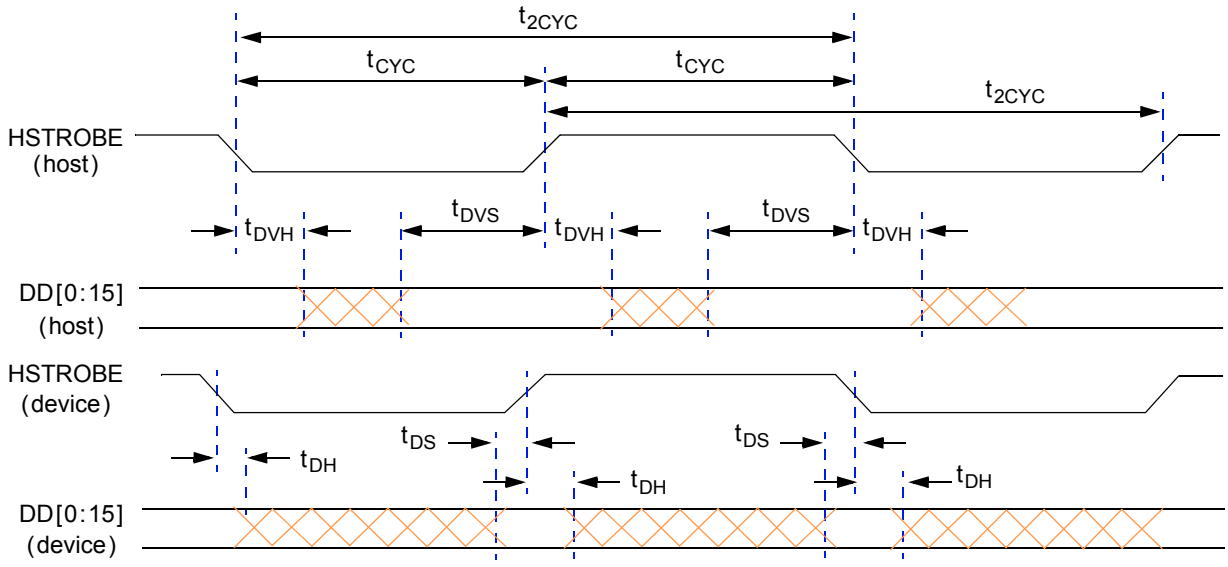


Figure 23. Timing Diagram—Sustained Ultra DMA Data Out Burst

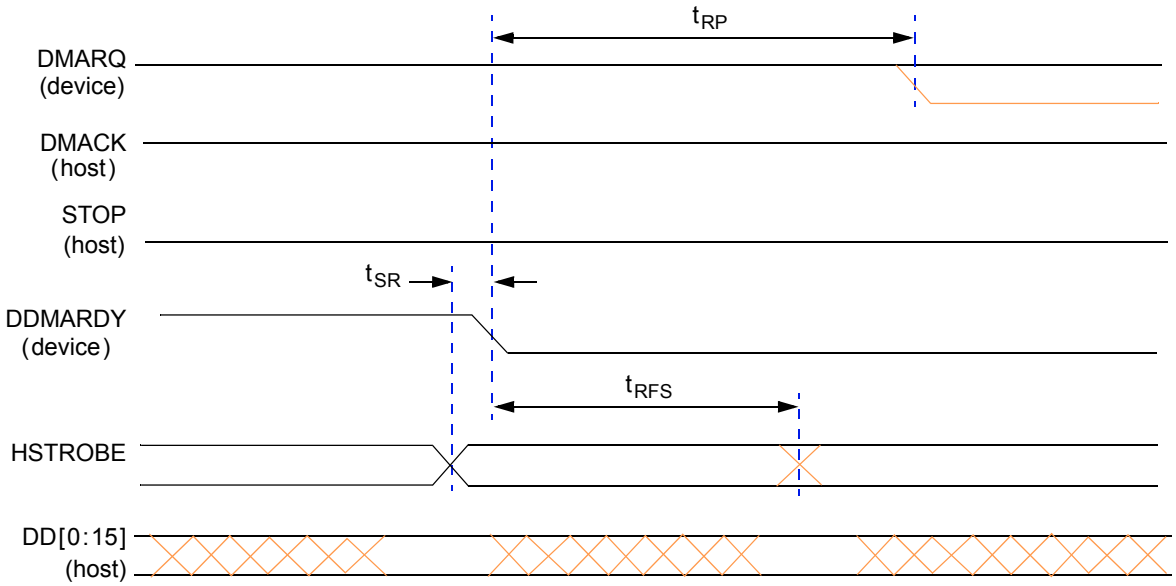


Figure 24. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

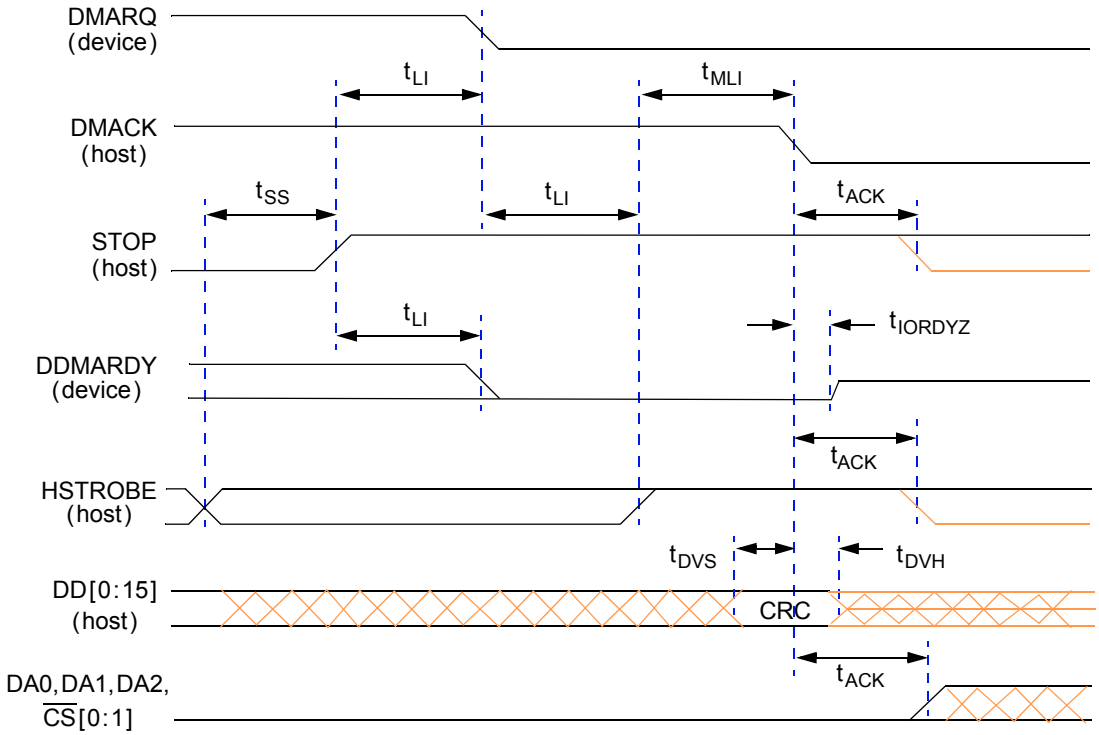


Figure 25. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

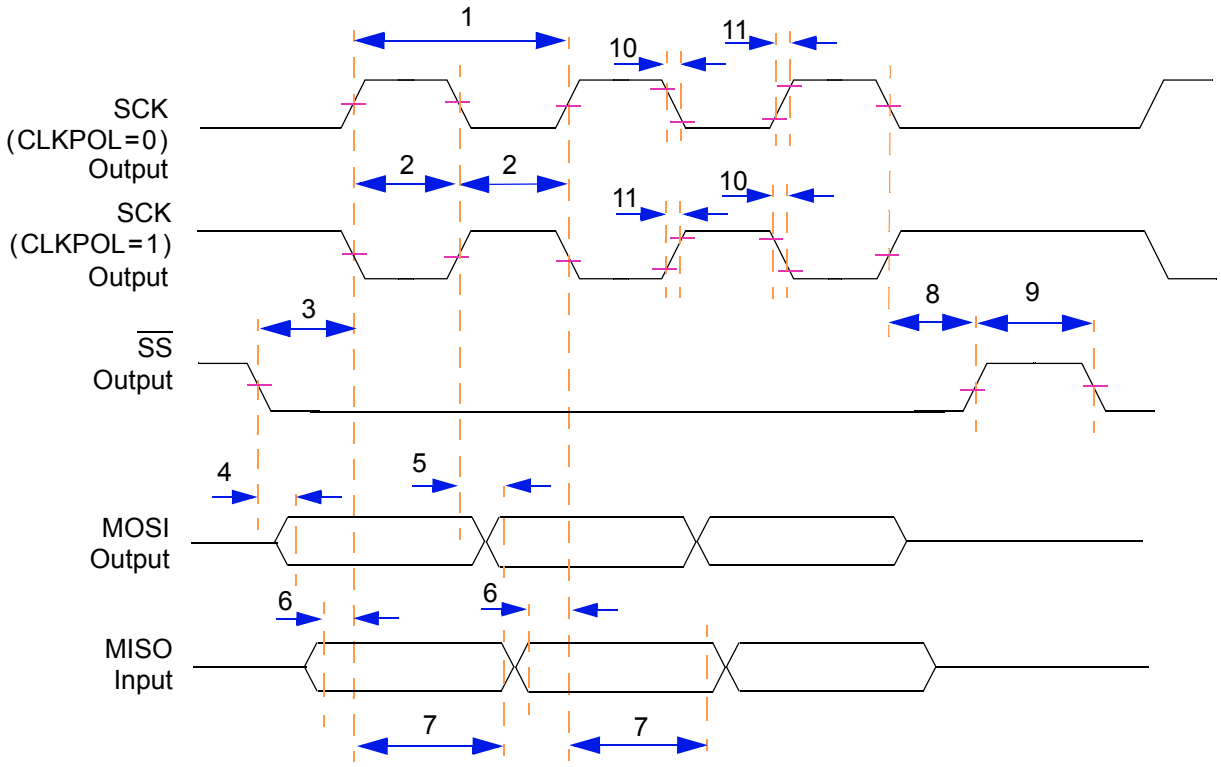


Figure 33. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 37. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.12
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.13
3	Slave select clock delay	15.0	—	ns	A11.14
4	Output Data valid after Slave Select ($\overline{SS}$)	—	50.0	ns	A11.15
5	Output Data valid after SCK	—	50.0	ns	A11.16
6	Input Data setup time	50.0	—	ns	A11.17
7	Input Data hold time	0.0	—	ns	A11.18
8	Slave disable lag time	15.0	—	ns	A11.19
9	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.20

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

Table 41. I²C Output Timing Specifications—SCL and SDA

Sym	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[3]	A13.8
2[1]	Clock low period	10	—	IP-Bus Cycle[3]	A13.9
3[2]	SCL/SDA rise time	—	7.9	ns	A13.10
4[1]	Data hold time	7	—	IP-Bus Cycle[3]	A13.11
5[1]	SCL/SDA fall time	—	7.9	ns	A13.12
6[1]	Clock high time	10	—	IP-Bus Cycle[3]	A13.13
7[1]	Data setup time	2	—	IP-Bus Cycle[3]	A13.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[3]	A13.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[3]	A13.16

NOTES:
1. Programming IFDR with the maximum frequency (IFDR=0x20) results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.
2. Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values
3. Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

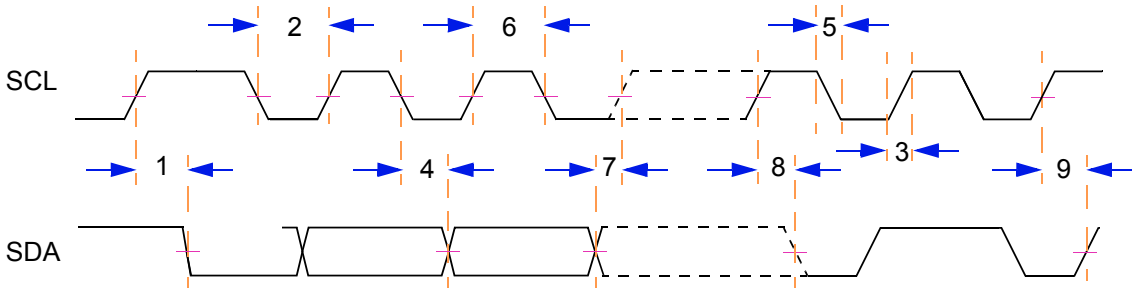


Figure 37. Timing Diagram—I²C Input/Output

3.3.14 J1850

See the MPC5200 User Manual [1].

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

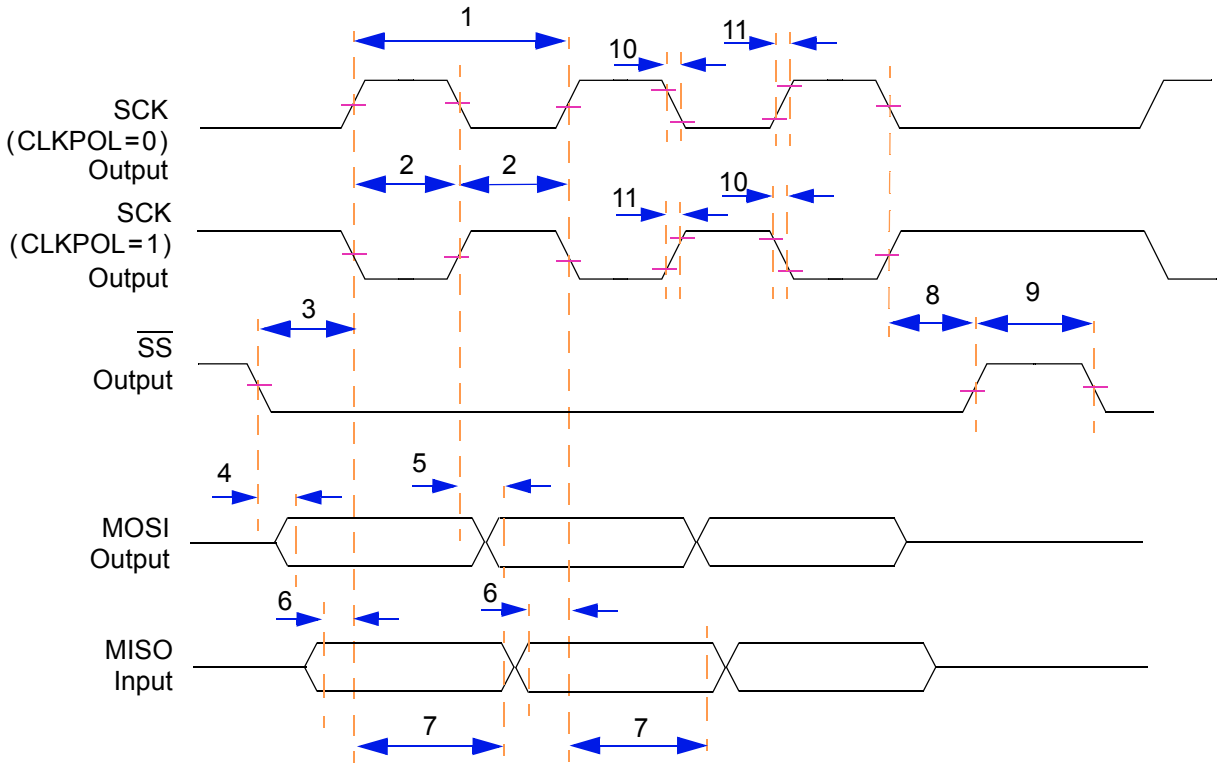


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

4 Package Description

4.1 Package Parameters

The MPC5200 uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline 27 mm x 27 mm
- Interconnects 272
- Pitch 1.27 mm

4.2 Mechanical Dimensions

Figure 51 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC5200, 272 TE-PBGA package.

4.3 Pinout Listings

See details in the MPC5200 User Manual [1].

Table 52. MPC5200 Pinout Listing

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
SDRAM						
MEM_CAS	CAS	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_CLK_EN	CLK_EN	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_CS		I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_DQM[3:0]	DQM	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_MA[12:0]	MA	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_MBA[1:0]	MBA	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_MDQS[3:0]	MDQS	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_MDQ[31:0]	MDQ	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_CLK		I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_CLK		I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_RAS	RAS	I/O	VDD_MEM_IO	DRV16_MEM	TTL	
MEM_WE		I/O	VDD_MEM_IO	DRV16_MEM	TTL	
PCI						
EXT_AD[31:0]		I/O	VDD_IO	PCI	PCI	
PCI_CBE_0		I/O	VDD_IO	PCI	PCI	
PCI_CBE_1		I/O	VDD_IO	PCI	PCI	
PCI_CBE_2		I/O	VDD_IO	PCI	PCI	
PCI_CBE_3		I/O	VDD_IO	PCI	PCI	
PCI_CLOCK		I/O	VDD_IO	PCI	PCI	
PCI_DEVSEL		I/O	VDD_IO	PCI	PCI	
PCI_FRAME		I/O	VDD_IO	PCI	PCI	
PCI_GNT		I/O	VDD_IO	DRV8	TTL	
PCI_IDSEL		I/O	VDD_IO	DRV8	TTL	
PCI_IRDY		I/O	VDD_IO	PCI	PCI	
PCI_PAR		I/O	VDD_IO	PCI	PCI	
PCI_PERR		I/O	VDD_IO	PCI	PCI	
PCI_REQ		I/O	VDD_IO	DRV8	TTL	
PCI_RESET		I/O	VDD_IO	PCI	PCI	
PCI_SERR		I/O	VDD_IO	PCI	PCI	
PCI_STOP		I/O	VDD_IO	PCI	PCI	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
I2C_3	SDA	I/O	VDD_IO	DRV4	Schmitt	
PSC						
PSC1_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC1_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	TTL	
PSC1_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC2_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC2_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	TTL	
PSC2_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_0	USB_OE, TxDS, TX	I/O	VDD_IO	DRV4	TTL	
PSC3_1	USB_TXN, RxD, RX	I/O	VDD_IO	DRV4	TTL	
PSC3_2	USB_TXP, BitClk, RTS	I/O	VDD_IO	DRV4	TTL	
PSC3_3	USB_RXD, Frame, $\overline{SS}$, CTS	I/O	VDD_IO	DRV4	TTL	
PSC3_4	USB_RXP, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
PSC3_6	USB_PRTPWR, Mclk, MOSI	I/O	VDD_IO	DRV4	TTL	
PSC3_7	USB_SPEED. MISO	I/O	VDD_IO	DRV4	TTL	
PSC3_8	USB_SUPEND, $\overline{SS}$	I/O	VDD_IO	DRV4	TTL	
PSC3_9	USB_OVRCNT, SCK	I/O	VDD_IO	DRV4	TTL	
GPIO/TIMER						
GPIO_WKUP_6	$\overline{MEM\_CS1}$	I/O	VDD_MEM_IO	DRV16_MEM	TTL	PULLUP_MEM
GPIO_WKUP_7		I/O	VDD_IO	DRV8	TTL	
TIMER_0		I/O	VDD_IO	DRV4	TTL	

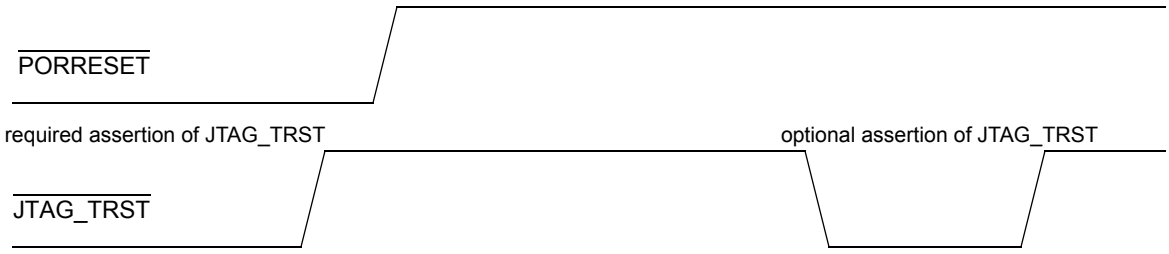


Figure 54. PORRESET vs. JTAG_TRST

5.4.1.2 Connecting JTAG_TRST

The wiring of the JTAG_TRST depends on the existence of a board-related debug interface (see Table 53 below).

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200.

5.4.2 G2_LE COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.4.2.1 Boards interfacing the JTAG port via a COP connector

The MPC5200 functional pin interface and internal logic provides access to the embedded G2_LE processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset		10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset		10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O

6 Ordering Information

Table 54. Ordering Information

Part Number	Speed	Ambient Temp	Qualification
MPC5200BV400	400	0C to 70C	Commercial
MPC5200CBV266	266	-40C to 85C	Industrial
MPC5200CBV400	400	-40C to 85C	Industrial
SPC5200CBV400	400	-40C to 85C	Automotive - AEC

7 Document Revision History

Table 55 provides a revision history for this hardware specification.

Table 55. Document Revision History

Rev. No.	Substantive Change(s)
0.1	First Preliminary release with some TBD's in spec tables (6/2003)
0.2	Added AC specs for missing modules, power-on sequence, misc other updates (7/2003)
0.2.1	Corrected maximum core operating frequency (7/2003)
0.3	Added Memory Interface Timing values, misc other updates (8/2003)
1.0	Added Information about JTAG_TRST (11/2003)
2.0	Added Power Numbers (Section 3.1.5), updated Oscillator and PLL Characteristics (Section 3.2), updated SDRAM AC Characteristics (Section 3.3.5)
3.0	Change to Freescale brand and format (8/2004)
4.0	Updates to LPC timing, DDR SDRAM timing, JTAG section, replaced TBD's (1/2005)
	Rev 4 has been regenerated with the new Freescale appearance guidelines, the title was changed and the reference to www.mobilegt.com in the first paragraph (Note) was changed to www. freescale.com (3/2006).

For more detailed information, refer to the following documentation:

[1] MPC5200 User Manual MPC5200UM

[2] PowerPC Microprocessor Family: The Programming Environments for 32-bit Microprocessors, Rev. 2: MPCFPE32B/AD

[3] G2 Core Reference Manual, Rev. 0: G2CORERM/D

[4] PCI Local Bus Specification, Revision 2.2, December 18, 1998

[5] ANSI ATA-4 Specification

[6] IEEE 802.3 Specification (ETHERNET)

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