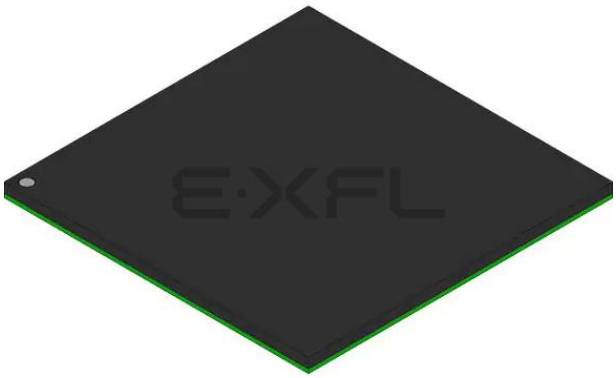

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc5200cbv400

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200 processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{\text{analog}} + P_{IO}$$

Table 6. Power Dissipation

Core Power Supply (VDD_CORE)					
Mode	SYS_XTAL/XLB/PCI/IPG/CORE (MHz)		Unit	Notes	SpecID
	33/66/33/33/264	33/132/66/132/396			
	Typ	Typ			
Operational	727.5	1080	mW	[1],[2]	D5.1
Doze	—	600	mW	[1],[3]	D5.2
Nap	—	225	mW	[1],[4]	D5.3
Sleep	—	225	mW	[1],[5]	D5.4
Deep-Sleep	52.5	52.5	mW	[1],[6]	D5.5
PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)					
Mode	**Typ**		**Unit**	**Notes**	
Typical	2		mW	[7]	D5.6
Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8])					
Mode	**Typ**		**Unit**	**Notes**	
Typical	33		mW	[9]	D5.7

NOTES:
1. Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 C
2. Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.
3. Doze power is measured with the G2_LE core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive
4. Nap power is measured with the G2_LE core in Nap mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
5. Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
6. Deep-Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL, Core PLL and all other system modules are inactive
7. Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 C
8. IO power figures given in the table represent the worst case scenario. For the mem_io rail connected to 2.5V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3V.
9. Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD\_MEM\_IO_{SDR}$= 3.3 V, Tj = 25 C

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance[1-3]. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.2 Oscillator and PLL Electrical Characteristics

The MPC5200 System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The G2_LE core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The G2_LE core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

3.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	100	µs	O1.2

3.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	1	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	T_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	2	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	3	—	—	100	µs	O3.5

NOTES:
1. The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2. This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3. Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 G2_LE Core PLL Electrical Characteristics

The internal clocking of the G2_LE core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. G2_LE PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
G2_LE frequency	f_{core}	1	50	—	550	MHz	O4.1
G2_LE cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
G2_LE VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
G2_LE input clock frequency	f_{XLB_CLK}		25	—	367	MHz	O4.4
G2_LE input clock cycle time	t_{XLB_CLK}		2.73	—	50.0	ns	O4.5
G2_LE input clock jitter	t_{jitter}	2	—	—	150	ps	O4.6
G2_LE PLL relock time	t_{lock}	3	—	—	100	µs	O4.7

NOTES:
1 The XLB_CLK frequency and G2_LE PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and G2_LE PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = -40 to 85 °C
- Tj = -40 to 115 °C
- VDD_CORE = 1.42 to 1.58 V
  VDD_IO = 3.0 to 3.6 V
- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

3.3.1 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	G2_LE Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

3.3.2 Clock AC Specifications

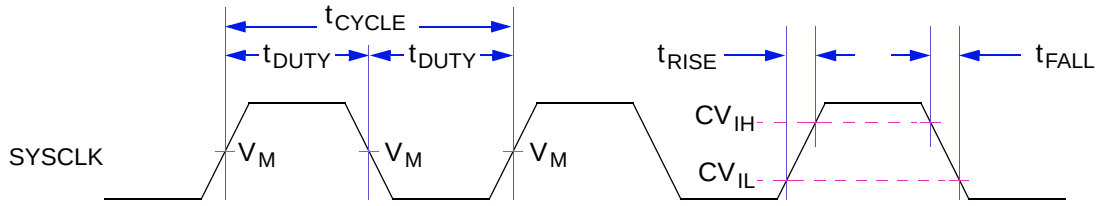


Figure 2. Timing Diagram—SYS_XTAL_IN

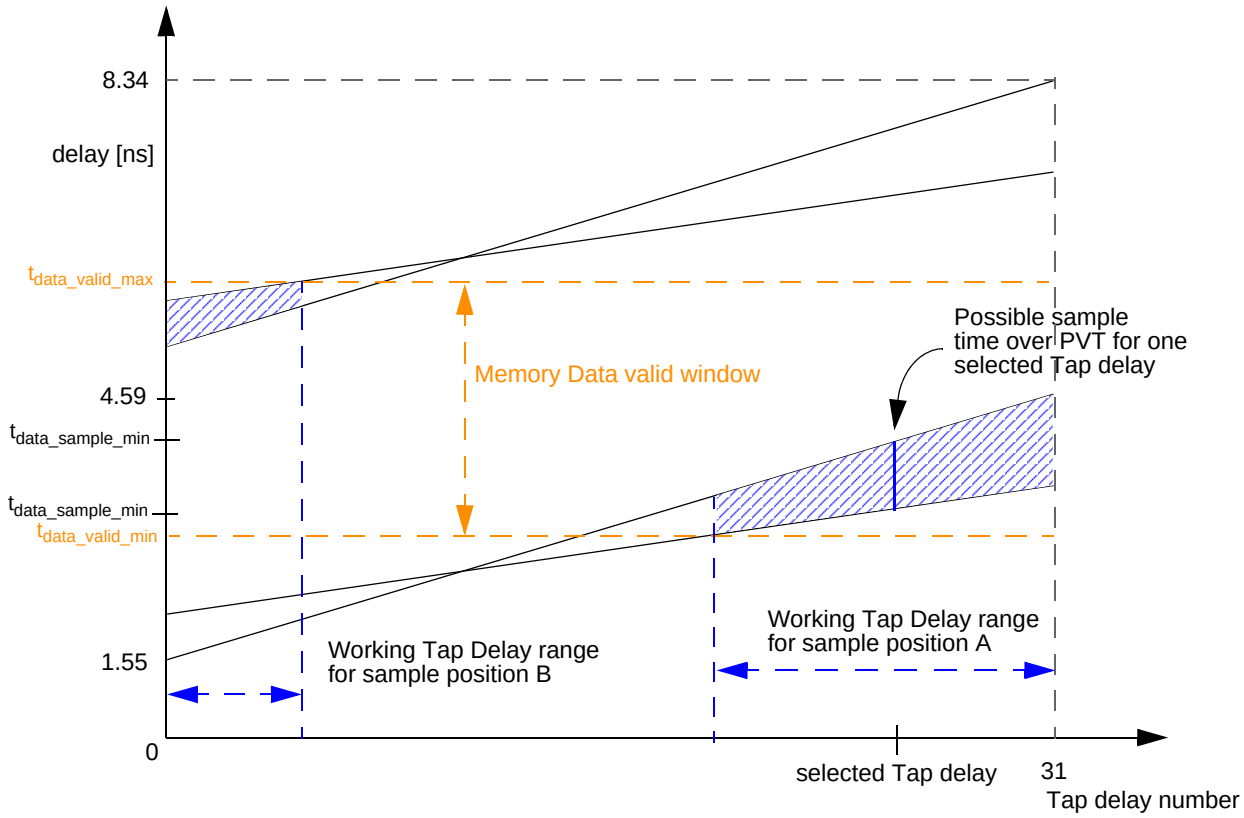


Figure 8. Read Data sample window depend on the number of Tap delay

The position of the t_{data_valid} window is depend on the clock / data flight time on the board. The MDQS signal indicate if the read data are valid. If the controller is not able to detect a valid MDQS signal on the sample time (sample position A) then the controller will look for valid MDQS / data on the next edge of the MEM_CLK signal (sample position B). Depend on the board travel time, different working tap delay configurations are possible. For a fast connection the data will be sampled with the next edge of MEM_CLK, this shows Figure 8, sample position A. With a longer connection maybe two sample positions are possible. Figure 8 shows a example with two working sample position (A and B). With a bigger board delay only sample position B will be possible.

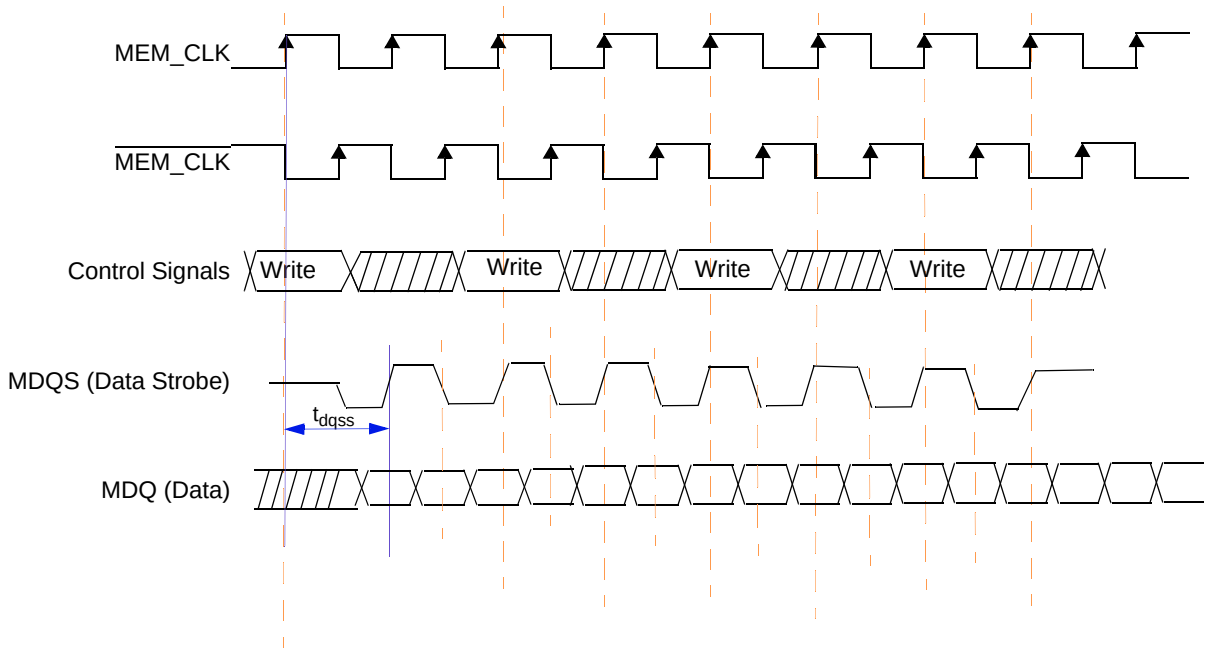
The equation below shows how to calculate the upper and lower limit. The right Tap delay number is selected, when the possible max and min sample timing is within the memory data valid window.

- $t_{data\_sample\_max}$ = max((1.55 + TapNum * 0.095), (1.74 + TapNum * 0.045))
- $t_{data\_sample\_min}$ = min((1.55 + TapNum * 0.095), (1.74 + TapNum * 0.045))

3.3.5.4 Memory Interface Timing-DDR SDRAM Write Command

Table 21. DDR SDRAM Memory Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.20
t_{DQSS}	Delay from write command to first rising edge of MDQS	—	t_{mem_clk}+0.4	ns	A5.21



NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 9. DDR SDRAM Memory Write Timing

3.3.6 PCI

The PCI interface on the MPC5200 is designed to PCI Version 2.2 and supports 33-MHz and 66-MHz PCI operations. See the PCI Local Bus Specification [4]; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

The MPC5200 is always the source of the PCI CLK. The clock waveform must be delivered to each 33-MHz or 66-MHz PCI component in the system. Figure 10 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
T_{val}	CLK to Signal Valid Delay - bused signals	2	6	2	11	ns	1,2,3	A6.5
T_{val}(ptp)	CLK to Signal Valid Delay - point to point	2	6	2	12	ns	1,2,3	A6.6
T_{on}	Float to Active Delay	2		2		ns	1	A6.7
T_{off}	Active to Float Delay		14		28	ns	1	A6.8
T_{su}	Input Setup Time to CLK - bused signals	3		7		ns	3,4	A6.9
T_{su}(ptp)	Input Setup Time to CLK - point to point	5		10,12		ns	3,4	A6.10
T_{h}	Input Hold Time from CLK	0		0		ns	4	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification [4]. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.
2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification [4].
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification [4].

For Measurement and Test Conditions, see the PCI Local Bus Specification [4].

3.3.7 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200. Maximum eight configurable Chip-selects are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:
WS = Wait State
DC = Dead Cycle
LB = Long Burst
DS = Data size in Byte
tPCIck = PCI clock period
tIPBIck = IPBI clock period

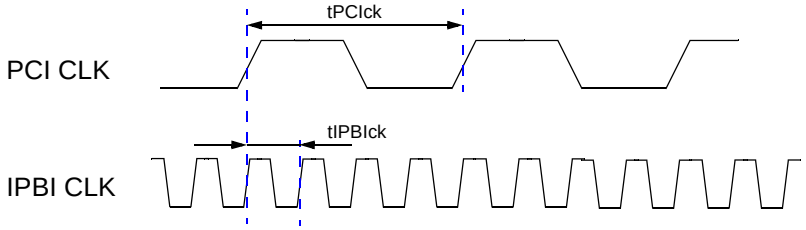


Figure 11. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

3.3.7.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.1
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.2
t_1	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns	1	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	-	ns	2	A7.5
t_4	OE assertion before CS assertion	-	0.4	ns		A7.6
t_5	OE negation before CS negation	-	0.4	ns		A7.7
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.8
t_7	RW hold after CS negation	t_{IPBIck}	-	ns		A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	-	ns		A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	-	ns		A7.11
t_{10}	DATA input setup before CS negation	2.8	-	ns		A7.12
t_{11}	DATA input hold after CS negation	0	(DC+1)*t_{PCIck}	ns		A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	-	ns	3	A7.14
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	3	A7.15

3.3.7.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.20
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.21
t_1	CS pulse width	$(1+WS+4^{LB}*2*(32/DS))*t_{PCIck}$	$(1+WS+4^{LB}*2*(32/DS))*t_{PCIck}$	ns	1,2	A7.22
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.23
t_3	ADDR hold after CS negation	-	-0.7	ns		A7.24
t_4	OE assertion before CS assertion	-	0.4	ns		A7.25
t_5	OE negation before CS negation	-	0.4	ns		A7.26
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.27
t_7	RW hold after CS negation	t_{PCIck}	-	ns		A7.28
t_8	DATA setup before rising edge of PCI	1.8	-	ns		A7.29
t_9	DATA hold after rising edge of PCI	0	-	ns		A7.30
t_{10}	DATA hold after CS negation	0	$(DC+1)*t_{PCIck}$	ns		A7.31
t_{11}	ACK assertion after CS assertion	-	$(WS+1)*t_{PCIck}$	ns		A7.32
t_{12}	ACK negation before CS negation	-	0.6	ns	3	A7.33
t_{13}	ACK pulse width	$4^{LB}*2*(32/DS)*t_{PCIck}$	$4^{LB}*2*(32/DS)*t_{PCIck}$	ns	2,3	A7.34
t_{14}	CS assertion after TS assertion	-	0.8	ns		A7.35
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns		A7.36

NOTES:
1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified 0 - 65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => $4^1*2*(32/8) = 32$ => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1+10+32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.

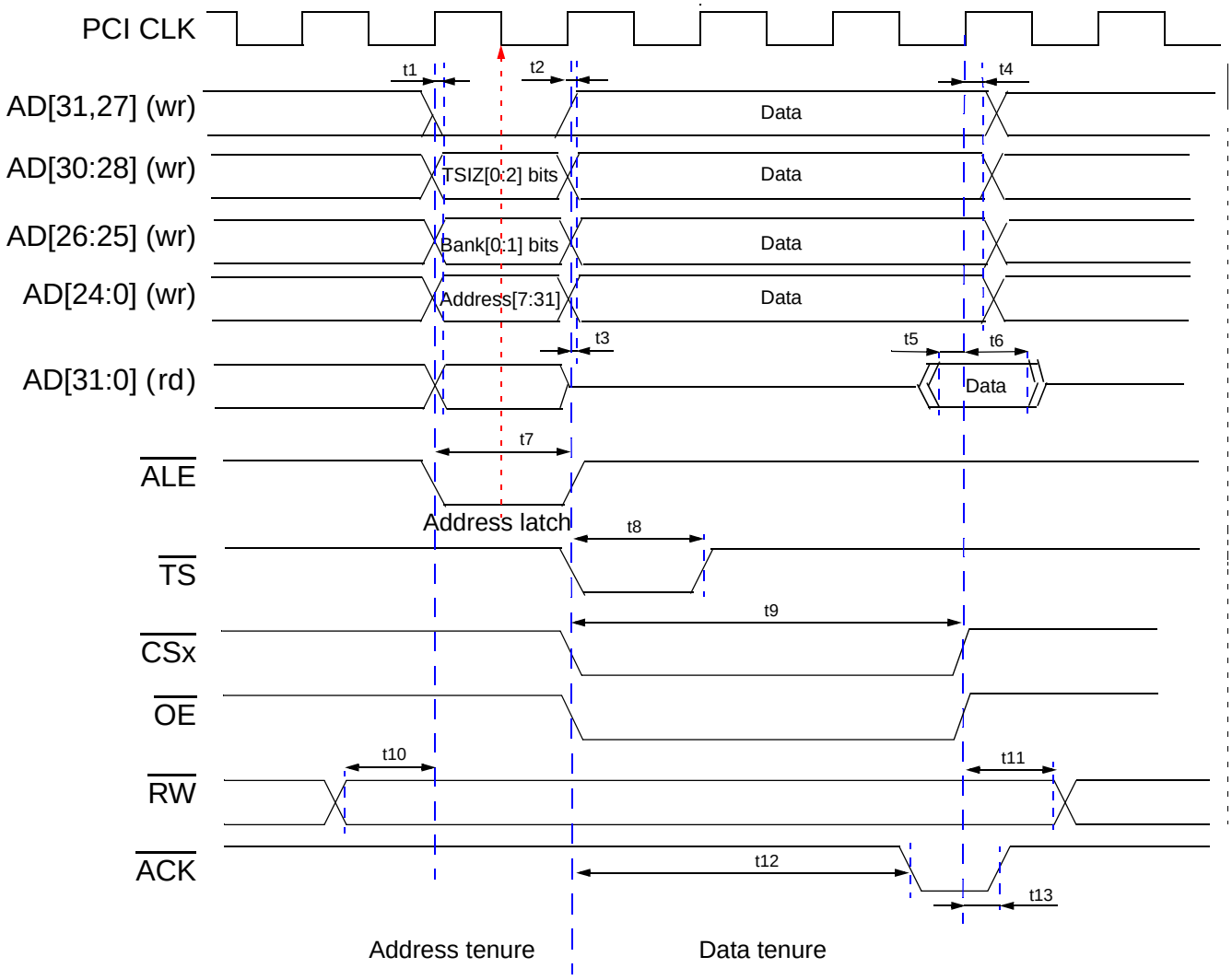


Figure 14. Timing Diagram—MUXed Mode

3.3.8 ATA

The MPC5200 ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nano seconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification [5] and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the MPC5200 User Manual [1].

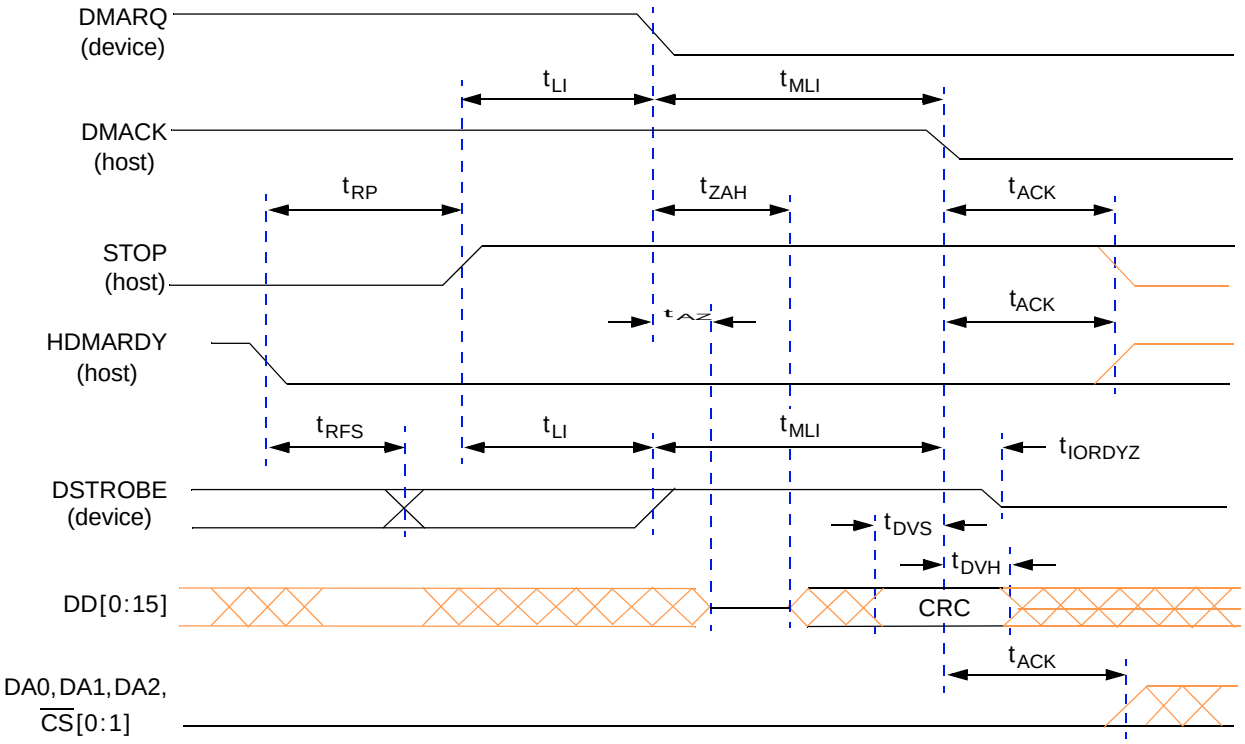


Figure 21. Timing Diagram—Host Terminating Ultra DMA Data In Burst

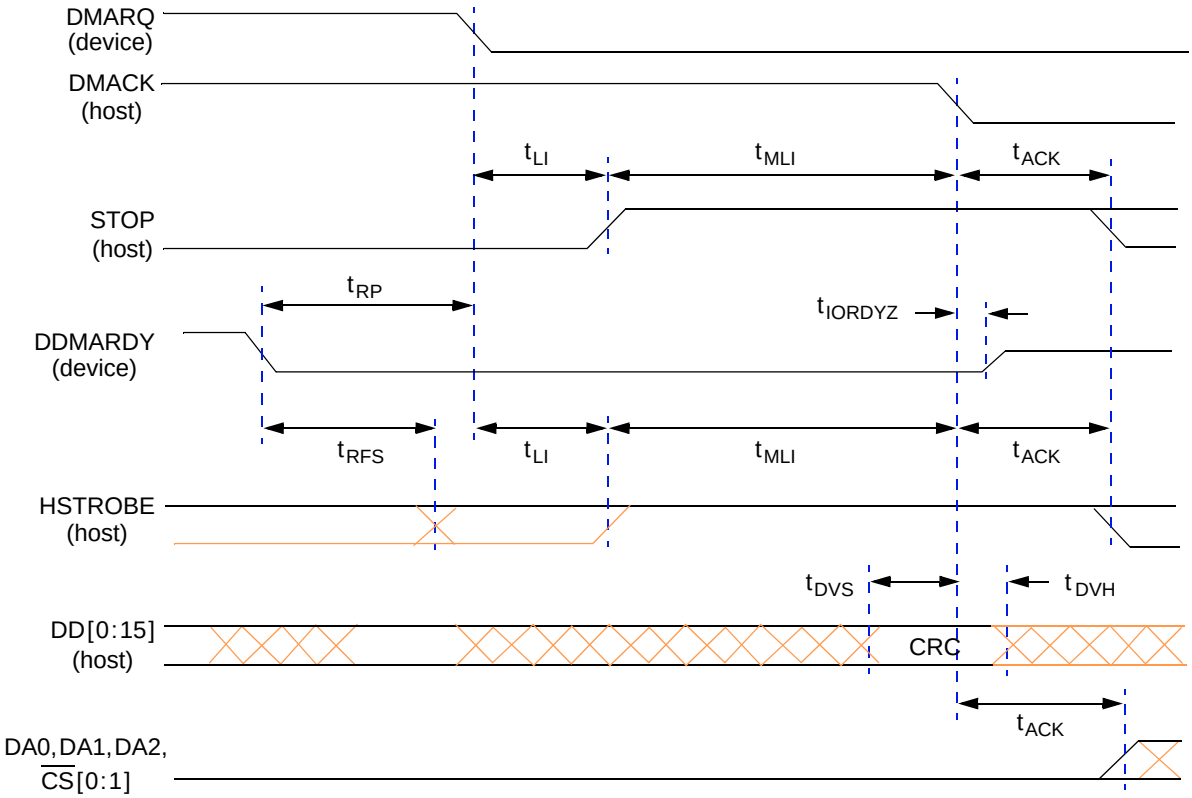


Figure 26. Timing Diagram—Drive Terminating Ultra DMA Data Out Burst

Table 30. Timing Specification ata_isolation

Sym	Description	Min	Max	Units	SpecID
1	ata_isolation setup time	7	-	IP Bus cycles	A8.48
2	ata_isolation hold time	-	19	IP Bus cycles	A8.49

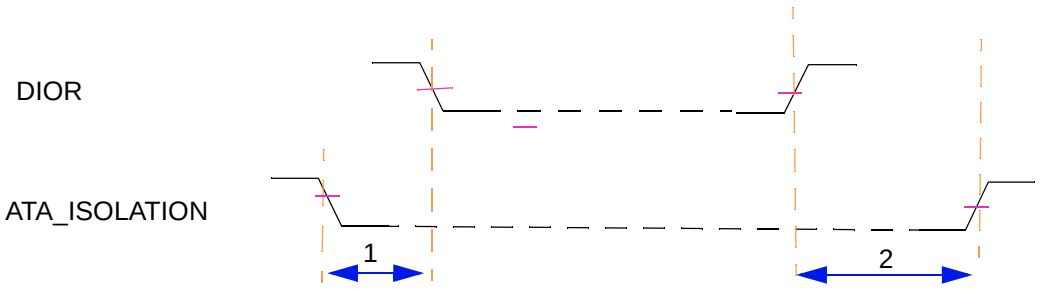


Figure 27. Timing Diagram-ATA-ISOLATION

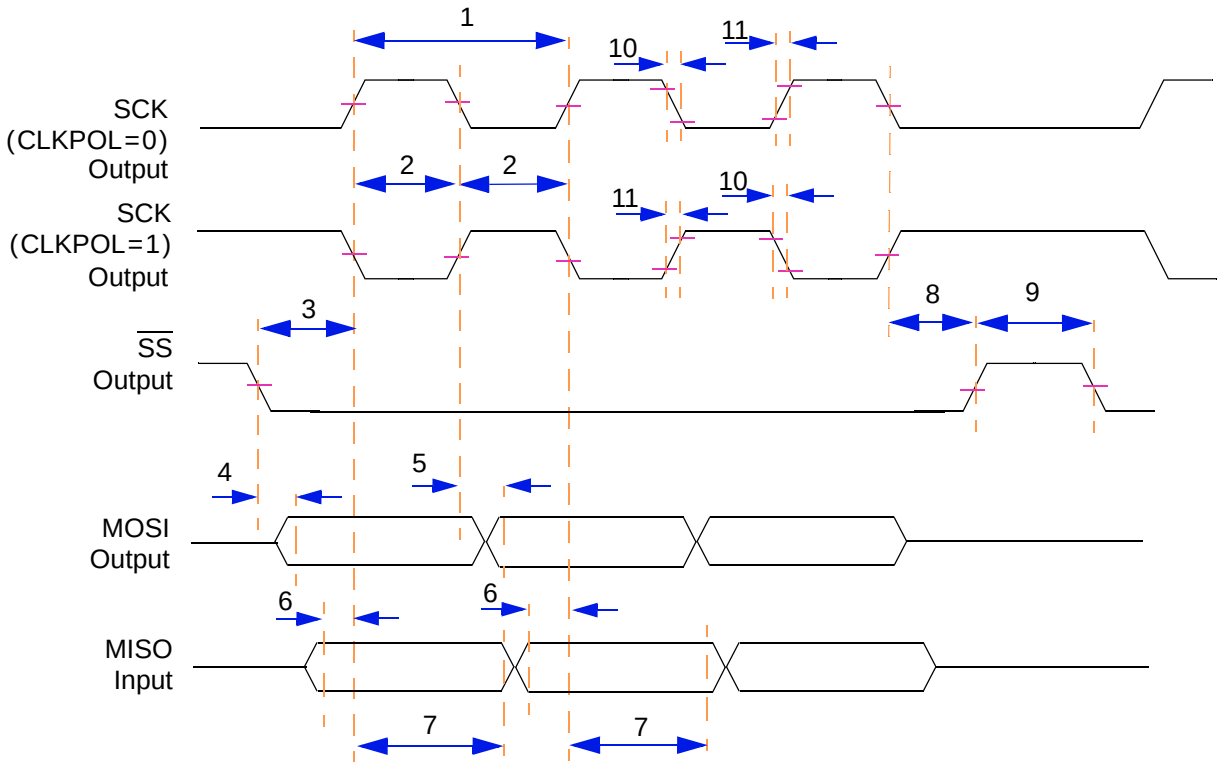


Figure 33. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 37. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.12
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.13
3	Slave select clock delay	15.0	—	ns	A11.14
4	Output Data valid after Slave Select ($\overline{SS}$)	—	50.0	ns	A11.15
5	Output Data valid after SCK	—	50.0	ns	A11.16
6	Input Data setup time	50.0	—	ns	A11.17
7	Input Data hold time	0.0	—	ns	A11.18
8	Slave disable lag time	15.0	—	ns	A11.19
9	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.20

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

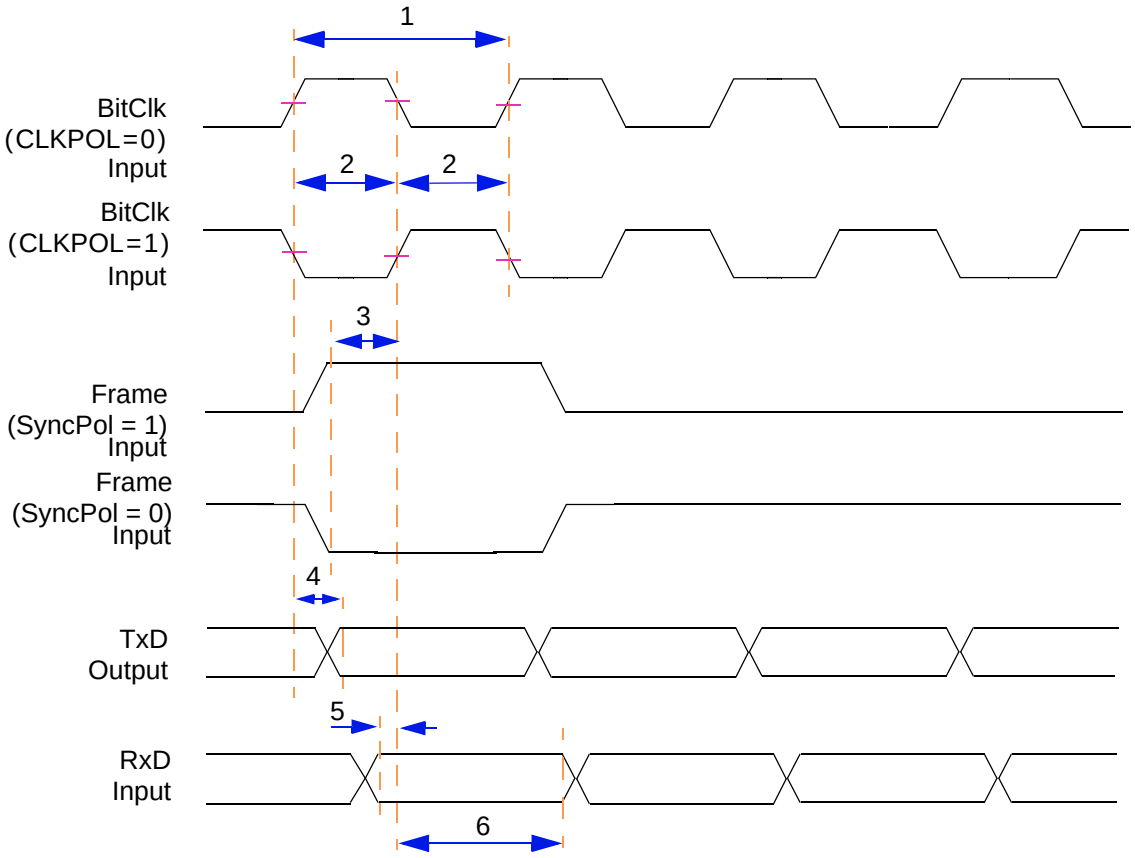


Figure 39. Timing Diagram — 8,16, 24, and 32-bit CODEC / I²S Slave Mode

3.3.15.2 AC97 Mode

Table 44. Timing Specifications — AC97 Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A15.15
2	Clock pulse high time	—	40.7	—	ns	A15.16
3	Clock pulse low time	—	40.7	—	ns	A15.17
4	Frame valid after rising clock edge	—	—	13.0	ns	A15.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A15.19
6	Input Data setup time	1.0	—	—	ns	A15.20
7	Input Data hold time	1.0	—	—	ns	A15.21

NOTE

Output timing was specified at a nominal 50 pF load.

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, TX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_2	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	TTL	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
TIMER_1		I/O	VDD_IO	DRV4	TTL	
TIMER_2	MOSI	I/O	VDD_IO	DRV4	TTL	
TIMER_3	MISO	I/O	VDD_IO	DRV4	TTL	
TIMER_4	SS	I/O	VDD_IO	DRV4	TTL	
TIMER_5	SCK	I/O	VDD_IO	DRV4	TTL	
TIMER_6		I/O	VDD_IO	DRV4	TTL	
TIMER_7		I/O	VDD_IO	DRV4	TTL	
Clock						
SYS_XTAL_IN		Input	VDD_IO			
SYS_XTAL_OUT		Output	VDD_IO			
RTC_XTAL_IN		Input	VDD_IO			
RTC_XTAL_OUT		Output	VDD_IO			
Misc						
$\overline{\text{PORRESET}}$		Input	VDD_IO	DRV4	Schmitt	
$\overline{\text{HRESET}}$		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
$\overline{\text{SRESET}}$		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
IRQ0		I/O	VDD_IO	DRV4	TTL	
IRQ1		I/O	VDD_IO	DRV4	TTL	
IRQ2		I/O	VDD_IO	DRV4	TTL	
IRQ3		I/O	VDD_IO	DRV4	TTL	
Test/Configuration						
SYS_PLL_TPA		I/O	VDD_IO	DRV4	TTL	
TEST_MODE_0		Input	VDD_IO	DRV4	TTL	
TEST_MODE_1		Input	VDD_IO	DRV4	TTL	
TEST_SEL_0		I/O	VDD_IO	DRV4	TTL	PULLUP
TEST_SEL_1		I/O	VDD_IO	DRV8	TTL	
JTAG_TCK	TCK	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDI	TDI	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDO	TDO	I/O	VDD_IO	DRV8	TTL	
JTAG_TMS	TMS	Input	VDD_IO	DRV4	TTL	PULLUP
$\overline{\text{JTAG\_TRST}}$	TRST	Input	VDD_IO	DRV4	TTL	PULLUP

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
Power and Ground						
VDD_IO		-				
VDD_MEM_IO		-				
VDD_CORE		-				
VSS_IO/CORE		-				
SYS_PLL_AVDD		-				
CORE_PLL_AVDD		-				

NOTES:
1 All “open drain” outputs of the MPC5200 are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200 I/O power rail if the external signal is driven above the MPC5200 I/O power rail voltage.

5 System Design Information

5.1 Power UP/Down Sequencing

Figure 52 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).

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