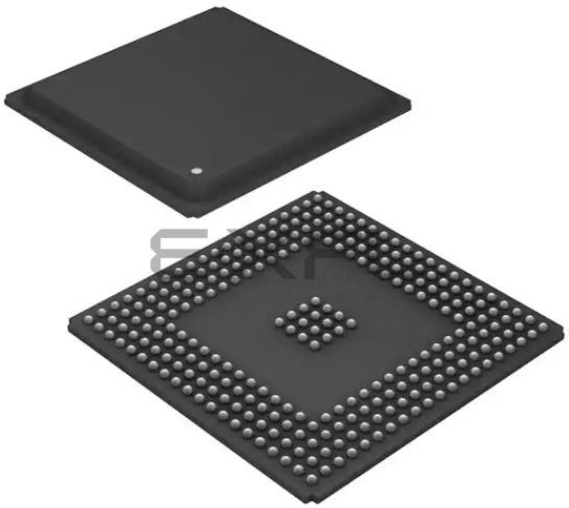

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5200vr400

2 Features

Key features are shown below.

- MPC603e series G2_LE core
  - Superscalar architecture
  - 760 MIPS at 400 MHz (-40 to +85 ^{o}C)
  - 16 k Instruction cache, 16 k Data cache
  - Double precision FPU
  - Instruction and Data MMU
  - Standard and Critical interrupt capability
- SDRAM / DDR Memory Interface
  - up to 132-MHz operation
  - SDRAM and DDR SDRAM support
  - 256-MByte addressing range per CS, two CS available
  - 32-bit data bus
  - Built-in initialization and refresh
- Flexible multi-function External Bus Interface
  - Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
  - 8 programmable Chip Selects
  - Non multiplexed data access using 8/16/32 bit databus with up to 26-bit address
  - Short or Long Burst capable
  - Multiplexed data access using 8/16/32 bit databus with up to 25-bit address
- Peripheral Component Interconnect (PCI) Controller
  - Version 2.2 PCI compatibility
  - PCI initiator and target operation
  - 32-bit PCI Address/Data bus
  - 33- and 66-MHz operation
  - PCI arbitration function
- ATA Controller
  - Version 4 ATA compatible external interface—IDE Disk Drive connectivity
- BestComm DMA subsystem
  - Intelligent virtual DMA Controller
  - Dedicated DMA channels to control peripheral reception and transmission
  - Local memory (SRAM 16 kBytes)
- 6 Programmable Serial Controllers (PSC), configurable for the following:
  - UART or RS232 interface

  - CODEC interface for Soft Modem, Master/Slave CODEC Mode, I^2S and AC97
  - Full duplex SPI mode
  - IrDA mode from 2400 bps to 4 Mbps
- Fast Ethernet Controller (FEC)
  - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII, 10 Mbps 7-wire interface
- Universal Serial Bus Controller (USB)
  - USB Revision 1.1 Host
  - Open Host Controller Interface (OHCI)
  - Integrated USB Hub, with two ports.
- Two Inter-Integrated Circuit Interfaces (I^2C)
- Serial Peripheral Interface (SPI)
- Dual CAN 2.0 A/B Controller (MSCAN)
  - —Freescale Scalable Controller Area Network (FSCAN) architecture
  - Implementation of version 2.0A/B CAN protocol
  - Standard and extended data frames
- J1850 Byte Data Link Controller (BDLC)
  - J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125 kbps) serial data communications in automotive applications.
  - Supports 4X mode, 41.6 kbps
  - In-frame response (IFR) types 0, 1, 2, and 3 supported
- Systems level features
  - Interrupt Controller supports four external interrupt request lines and 47 internal interrupt sources
  - GPIO/Timer functions
    - Up to 56 total GPIO pins (depending on functional multiplexing selections) that support a variety of interrupt/WakeUp capabilities.
    - Eight GPIO pins with timer capability supporting input capture, output compare, and pulse width modulation (PWM) functions
  - Real-time Clock with one-second resolution
  - Systems Protection (watch dog timer, bus monitor)
  - Individual control of functional block clock sources
  - Power management: Nap, Doze, Sleep, Deep Sleep modes
  - Support of WakeUp from low power modes by different sources (GPIO, RTC, CAN)

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	Vin = 0 or VDD_IO/VDD_IO_MEM$_{SDR}$ (depending on input type [1])	I_{IN}	—	±10	µA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.14
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor - memory I/O buffers	PULLUP_MEM VDD_IO_MEM$_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin[3]		I_{CS}	-1.0	1.0	mA	D3.23
Capacitance	Vin = 0V, f = 1 MHz	C_{in}	—	15	pF	D3.24

NOTES:
1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.
2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.
3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200 Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3V	8	8	mA	D3.26

NOTE

Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

3.3.4 External Interrupts

The MPC5200 provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:

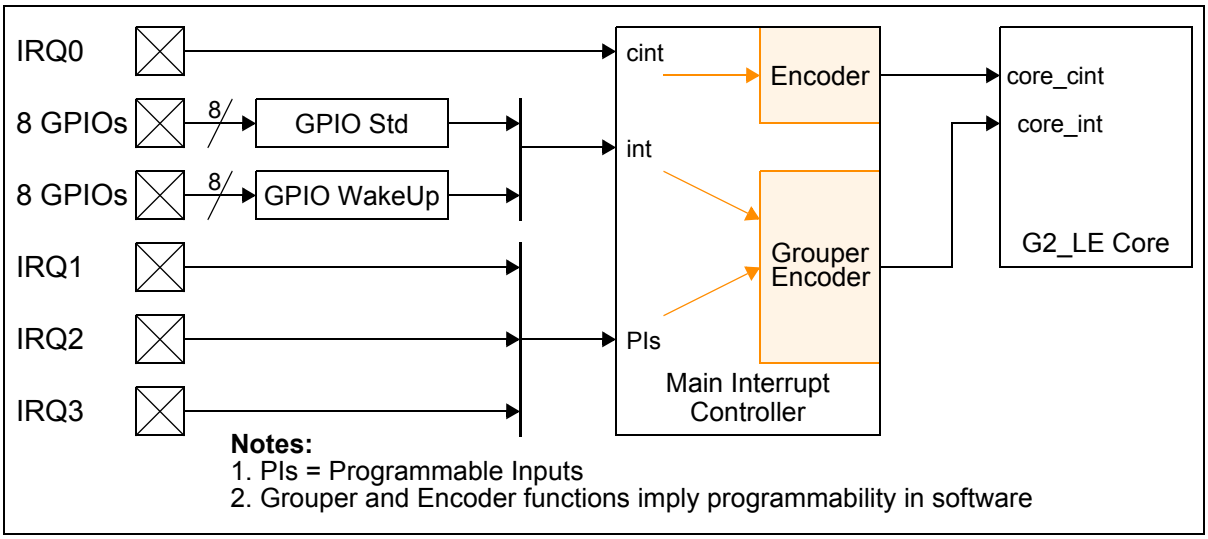


Figure 4. External interrupt scheme

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Note Table 16).

Table 16. External interrupt latencies

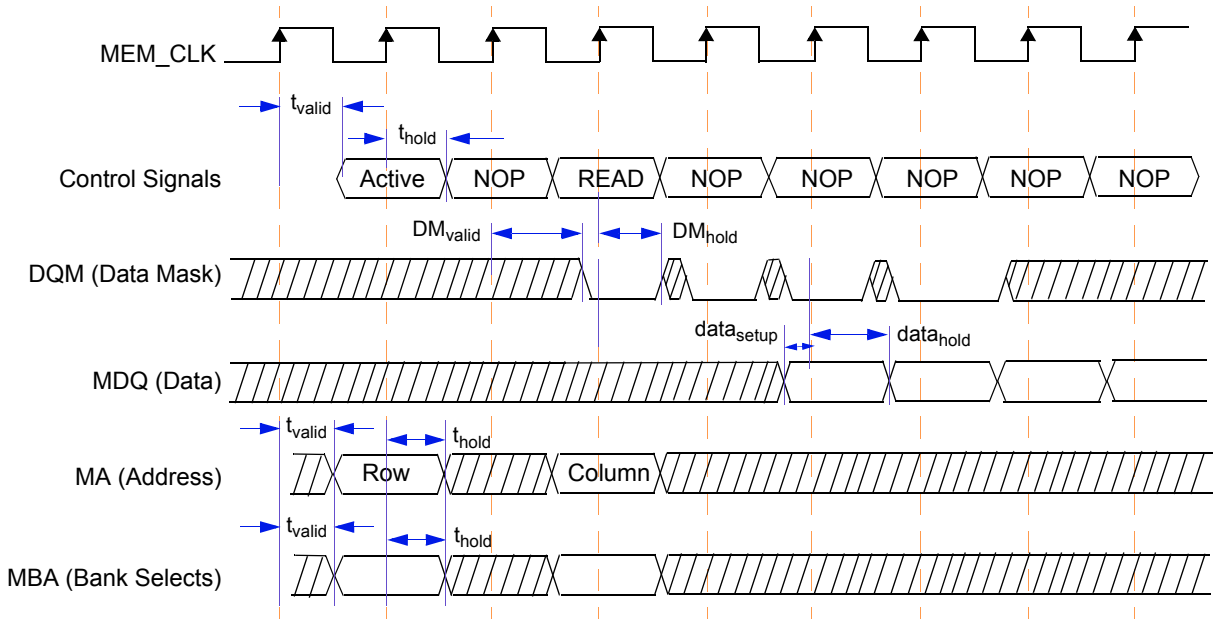
Interrupt Type	Pin Name	Clock Cycles	Reference Clock	Core Interrupt	SpecID
Interrupt Requests	IRQ0	10	IP_CLK	critical (cint)	A4.1
	IRQ0	10	IP_CLK	normal (int)	A4.2
	IRQ1	10	IP_CLK	normal (int)	A4.3
	IRQ2	10	IP_CLK	normal (int)	A4.5
	IRQ3	10	IP_CLK	normal (int)	A4.6

3.3.5 SDRAM

3.3.5.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.25+0.4	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	t_{mem_clk}*0.25-0.7	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

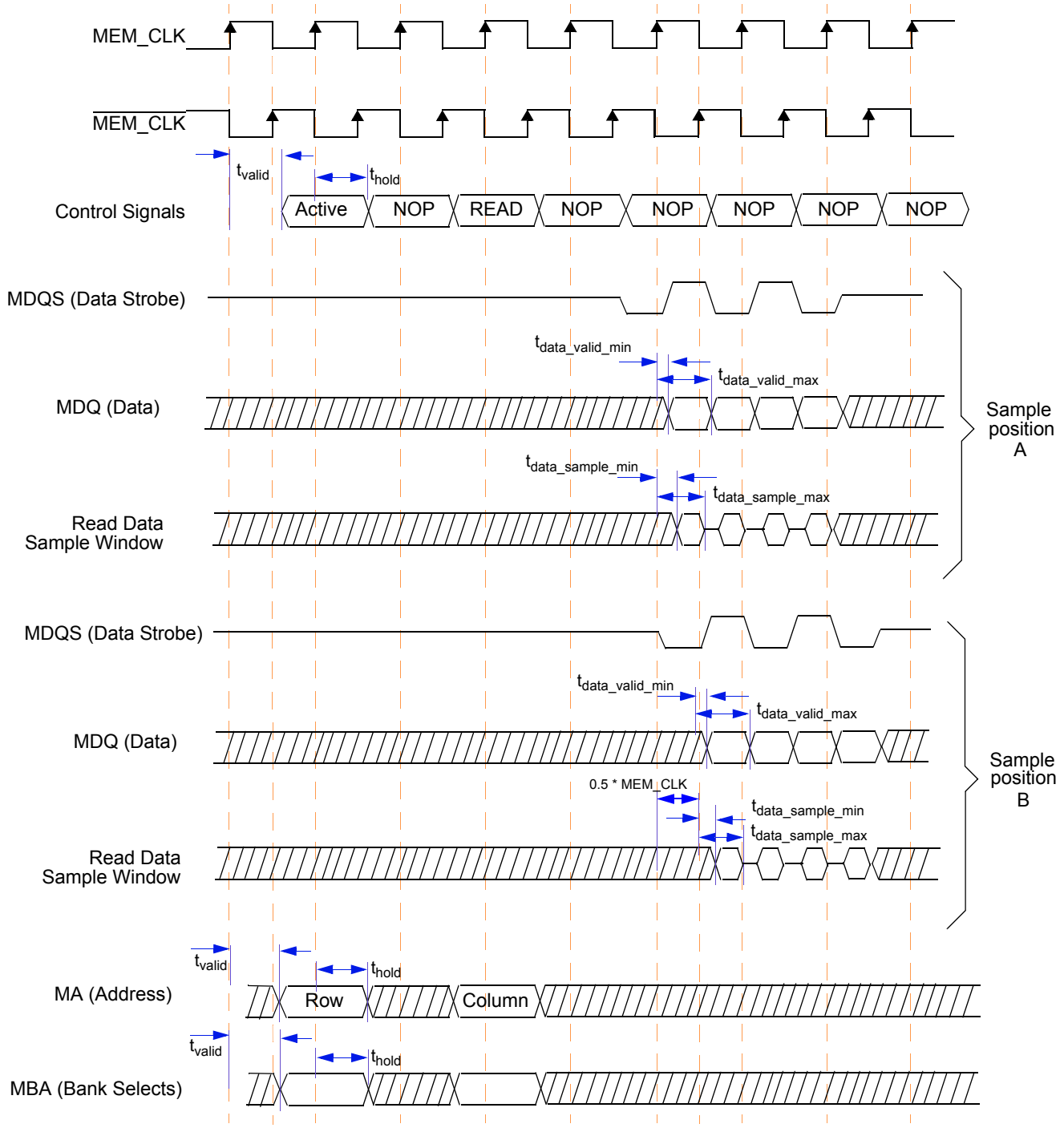
3.3.5.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the Mem_clk from the Memory Controller and captured on the Mem_clk clock at the memory device.

Table 20. DDR SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.15
t_{valid}	Control Signals, Address and MBA valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.16
t_{hold}	Control Signals, Address and MBA hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.17
$t_{data\_sample\_max}$	Read Data sample window	—	4.59[1]	ns	A5.18
$t_{data\_sample\_min}$	Read Data sample window	1.55[2]	—	ns	A5.19

NOTES:
1 Calculated with maximum number of Tap delay, 31 Tap delay are selected.
2 Calculated with minimum number of Tap delay, 0 Tap delay are selected.



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data
Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the vaild MDQS signal

NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

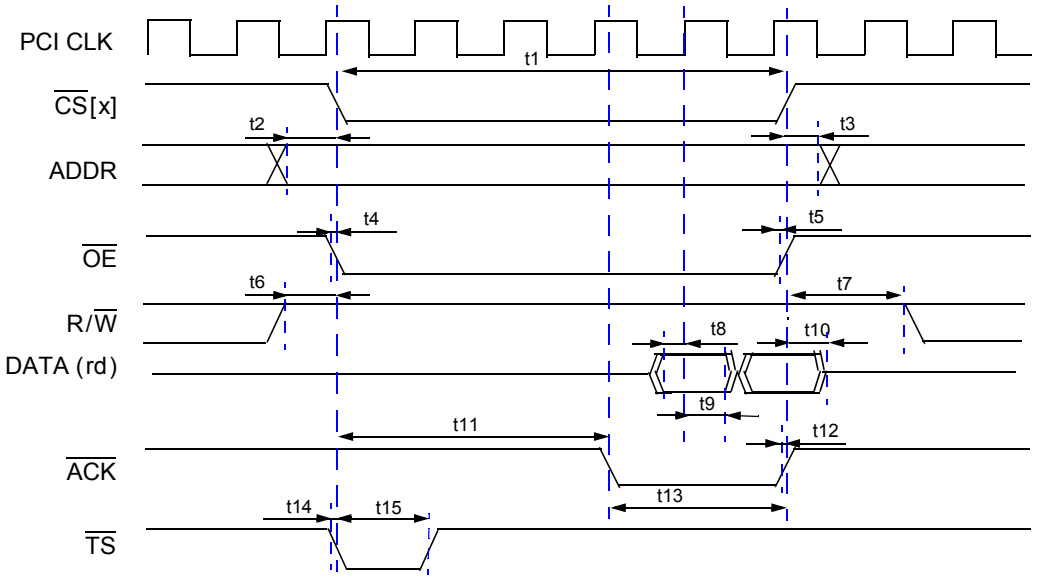


Figure 13. Timing Diagram—Burst Mode

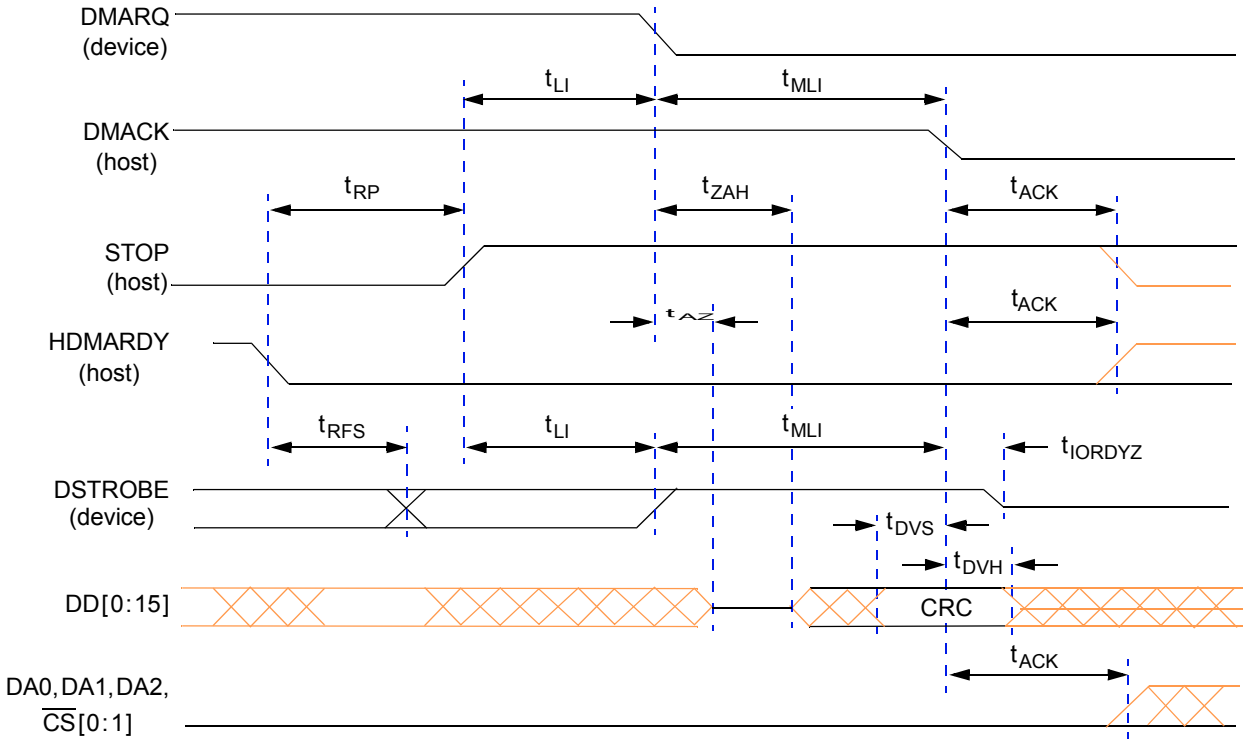


Figure 21. Timing Diagram—Host Terminating Ultra DMA Data In Burst

3.3.9 Ethernet

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 31. MII Rx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	10	—	ns	A9.1
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	10	—	ns	A9.2
M3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A9.3
M4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A9.4

NOTES:
1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification [6].

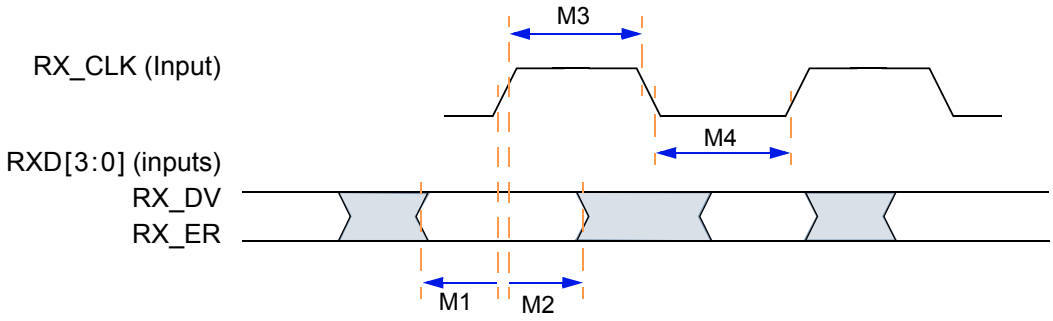


Figure 28. Ethernet Timing Diagram—MII Rx Signal

3.3.15 PSC

3.3.15.1 Codec Mode (8,16,24 and 32-bit) / I²S Mode

Table 42. Timing Specifications—8,16, 24 and 32-bit CODEC / I²S Master Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A15.1
2	Clock pulse width	—	50	—	%[1]	A15.2
3	Bit Clock fall time	—	—	7.9	ns	A15.3
4	Bit Clock rise time	—	—	7.9	ns	A15.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A15.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A15.6
7	Output Data valid after clock edge	—	—	9.3	ns	A15.7
8	Input Data setup time	6.0	—	—	ns	A15.8

NOTES:
1 Bit Clock cycle time

NOTE

Output timing was specified at a nominal 50 pF load.

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

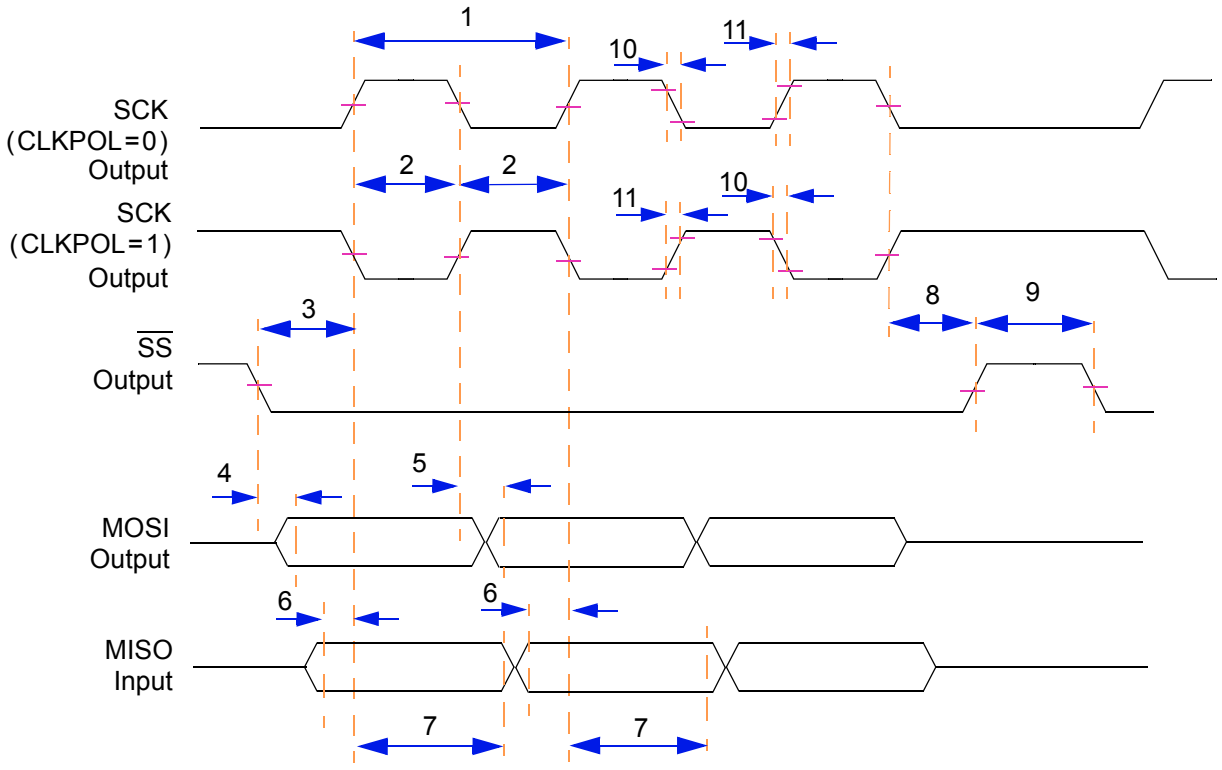
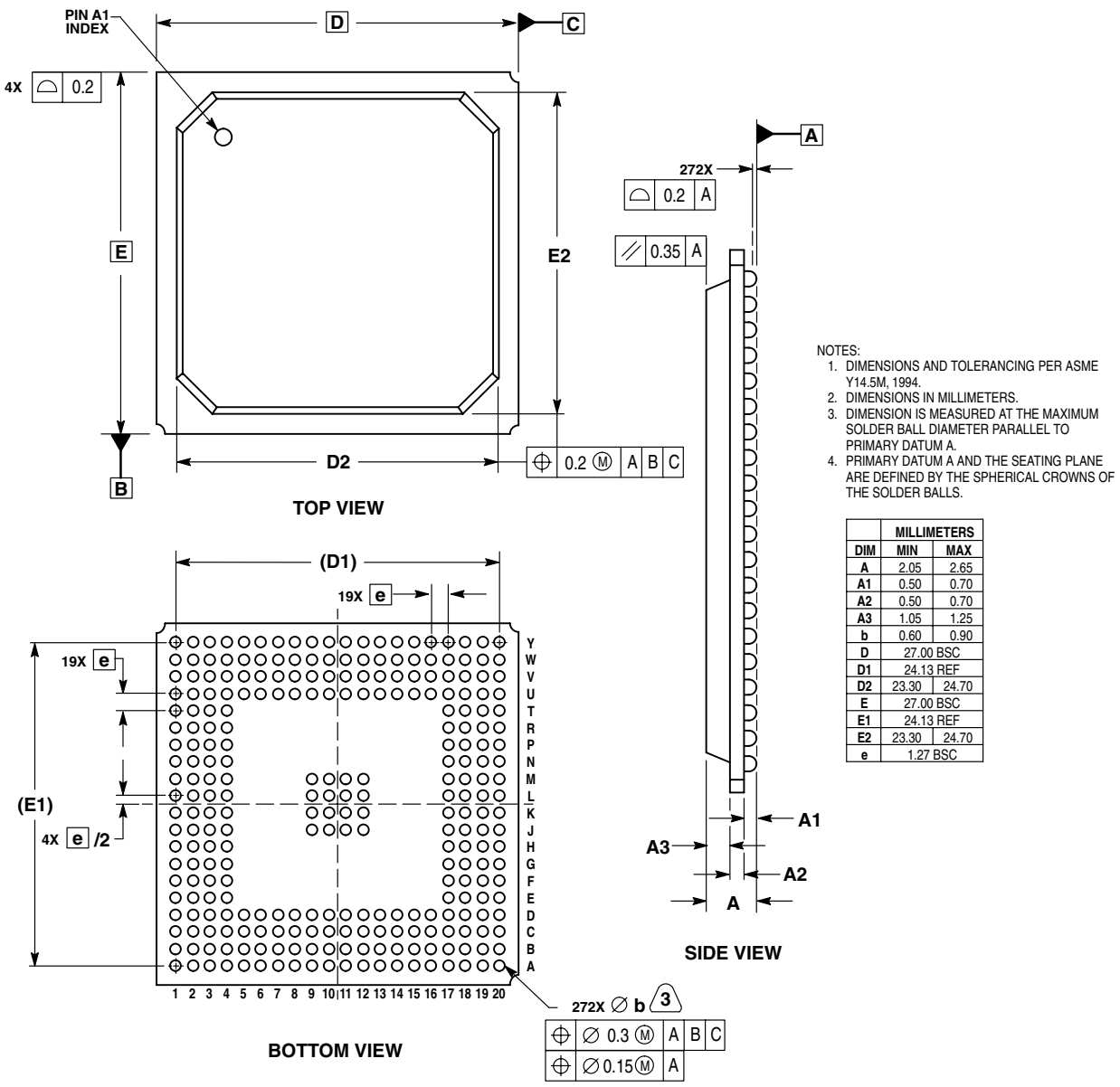


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135A–01
ISSUE B

Figure 51. Mechanical Dimensions and Pinout Assignments for the MPC5200, 272 TE-PBGA

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, TX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
I2C_3	SDA	I/O	VDD_IO	DRV4	Schmitt	
PSC						
PSC1_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC1_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	TTL	
PSC1_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC2_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC2_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	TTL	
PSC2_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_0	USB_OE, TxDS, TX	I/O	VDD_IO	DRV4	TTL	
PSC3_1	USB_TXN, RxD, RX	I/O	VDD_IO	DRV4	TTL	
PSC3_2	USB_TXP, BitClk, RTS	I/O	VDD_IO	DRV4	TTL	
PSC3_3	USB_RXD, Frame, $\overline{SS}$, CTS	I/O	VDD_IO	DRV4	TTL	
PSC3_4	USB_RXP, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
PSC3_6	USB_PRTPWR, Mclk, MOSI	I/O	VDD_IO	DRV4	TTL	
PSC3_7	USB_SPEED. MISO	I/O	VDD_IO	DRV4	TTL	
PSC3_8	USB_SUPEND, $\overline{SS}$	I/O	VDD_IO	DRV4	TTL	
PSC3_9	USB_OVRCNT, SCK	I/O	VDD_IO	DRV4	TTL	
GPIO/TIMER						
GPIO_WKUP_6	$\overline{MEM\_CS1}$	I/O	VDD_MEM_IO	DRV16_MEM	TTL	PULLUP_MEM
GPIO_WKUP_7		I/O	VDD_IO	DRV8	TTL	
TIMER_0		I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
Power and Ground						
VDD_IO		-				
VDD_MEM_IO		-				
VDD_CORE		-				
VSS_IO/CORE		-				
SYS_PLL_AVDD		-				
CORE_PLL_AVDD		-				

NOTES:
1 All “open drain” outputs of the MPC5200 are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200 I/O power rail if the external signal is driven above the MPC5200 I/O power rail voltage.

5 System Design Information

5.1 Power UP/Down Sequencing

Figure 52 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).

5.3.2 Pull-up Requirements for the PCI Control Lines

If the PCI interface is NOT used (and internally disabled) the PCI control pins must be terminated as indicated by the PCI Local Bus specification [4]. This is also required for MOST/Graphics and Large Flash Mode.

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

5.3.3 Pull-up/Pull-down Requirements for MEM_MDQS pins (SDRAM)

The MEM_MDQS[3:0] signals are not used with SDR memories and require pull-up or pull-down resistors in SDRAM mode.

5.4 JTAG

The MPC5200 provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200's imbedded Freescale (formerly Motorola) MPC603e G2_LE processor. This interface provides a means for executing test routines and for performing software development & debug functions.

5.4.1 JTAG_TRST

Boundary scan testing is enabled through the JTAG interface signals. The JTAG_TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

5.4.1.1 JTAG_TRST and PORRESET

The JTAG interface can control the direction of the MPC5200 I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5200 comes out of power-on reset; do this by asserting JTAG_TRST before PORRESET is released.

For more details refer to the Reset and JTAG Timing Specification.

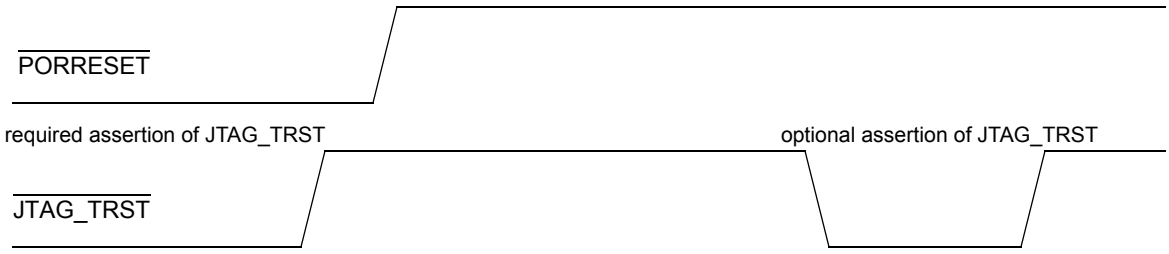


Figure 54. PORRESET vs. JTAG_TRST

5.4.1.2 Connecting JTAG_TRST

The wiring of the JTAG_TRST depends on the existence of a board-related debug interface (see Table 53 below).

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200.

5.4.2 G2_LE COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.4.2.1 Boards interfacing the JTAG port via a COP connector

The MPC5200 functional pin interface and internal logic provides access to the embedded G2_LE processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset		10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset		10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O

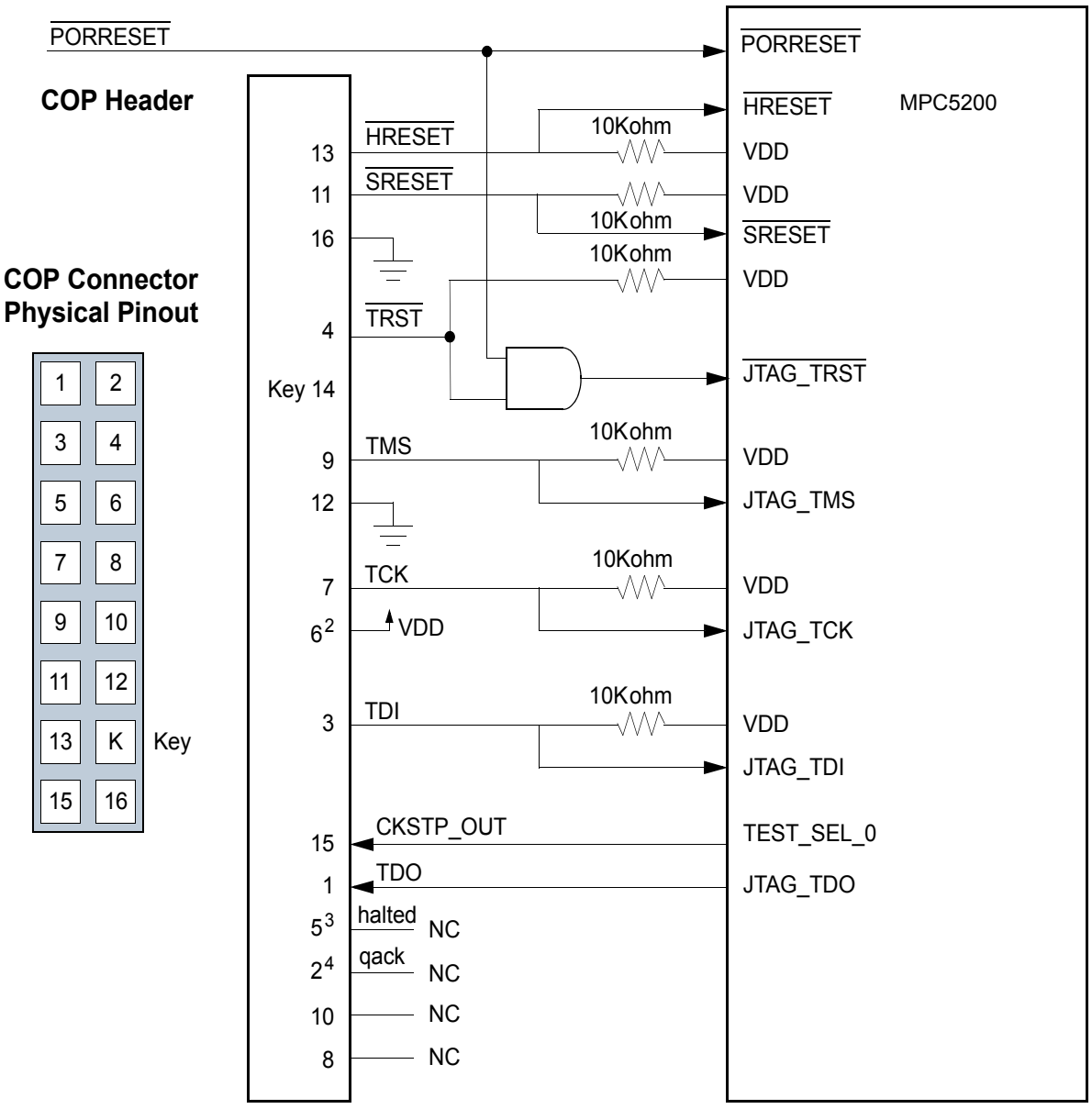


Figure 55. COP Connector Diagram

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