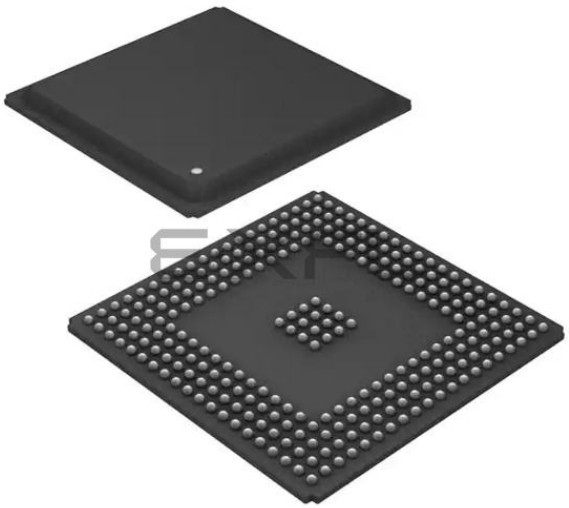

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cbv400

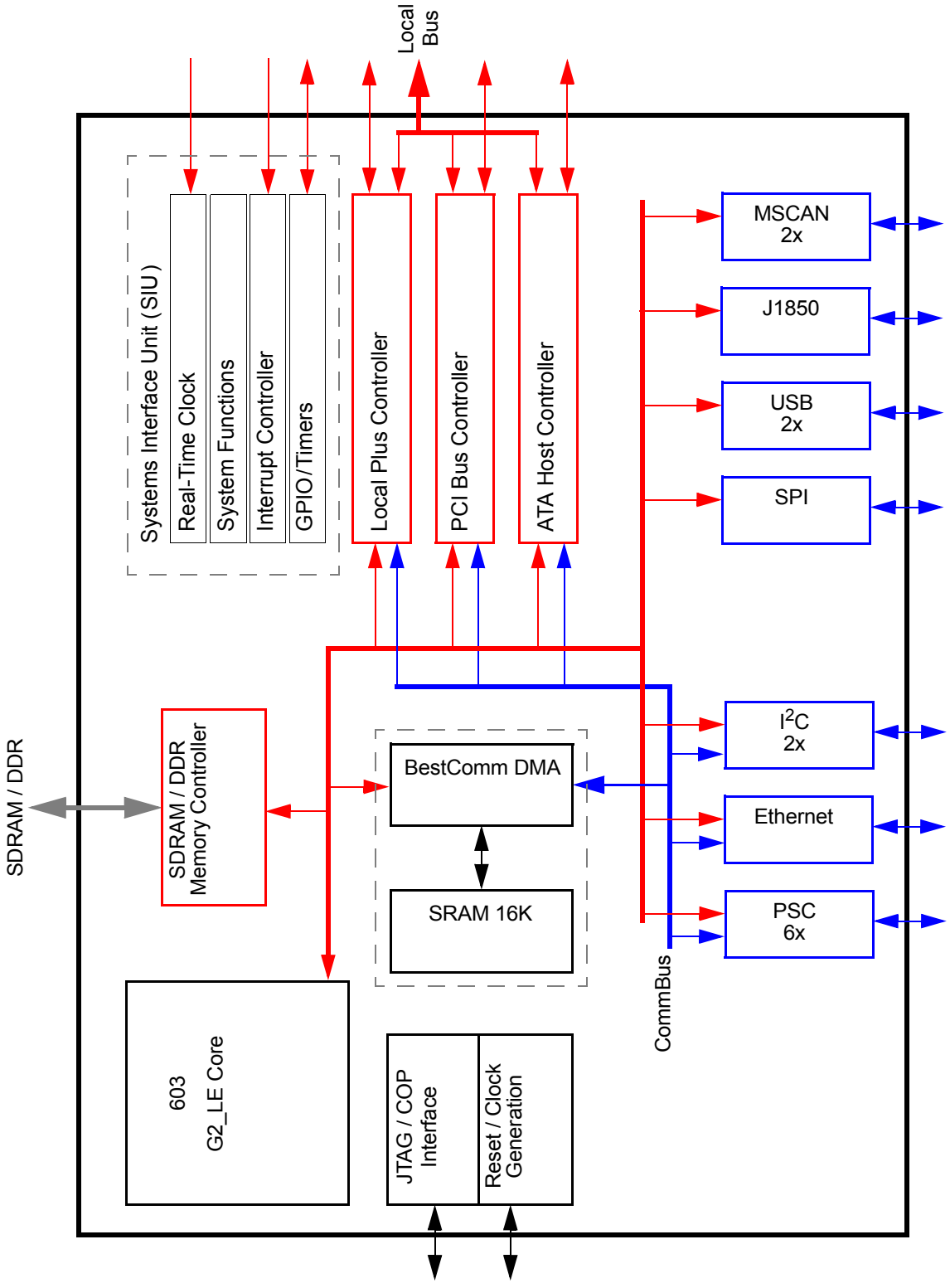


Figure 1. Simplified Block Diagram—MPC5200

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	Vin = 0 or VDD_IO/VDD_IO_MEM$_{SDR}$ (depending on input type [1])	I_{IN}	—	±10	µA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.14
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor - memory I/O buffers	PULLUP_MEM VDD_IO_MEM$_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin[3]		I_{CS}	-1.0	1.0	mA	D3.23
Capacitance	Vin = 0V, f = 1 MHz	C_{in}	—	15	pF	D3.24

NOTES:
1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.
2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.
3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200 Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3V	8	8	mA	D3.26

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The G2_LE core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The G2_LE core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

3.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	100	µs	O1.2

3.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	1	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	T_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	2	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	3	—	—	100	µs	O3.5

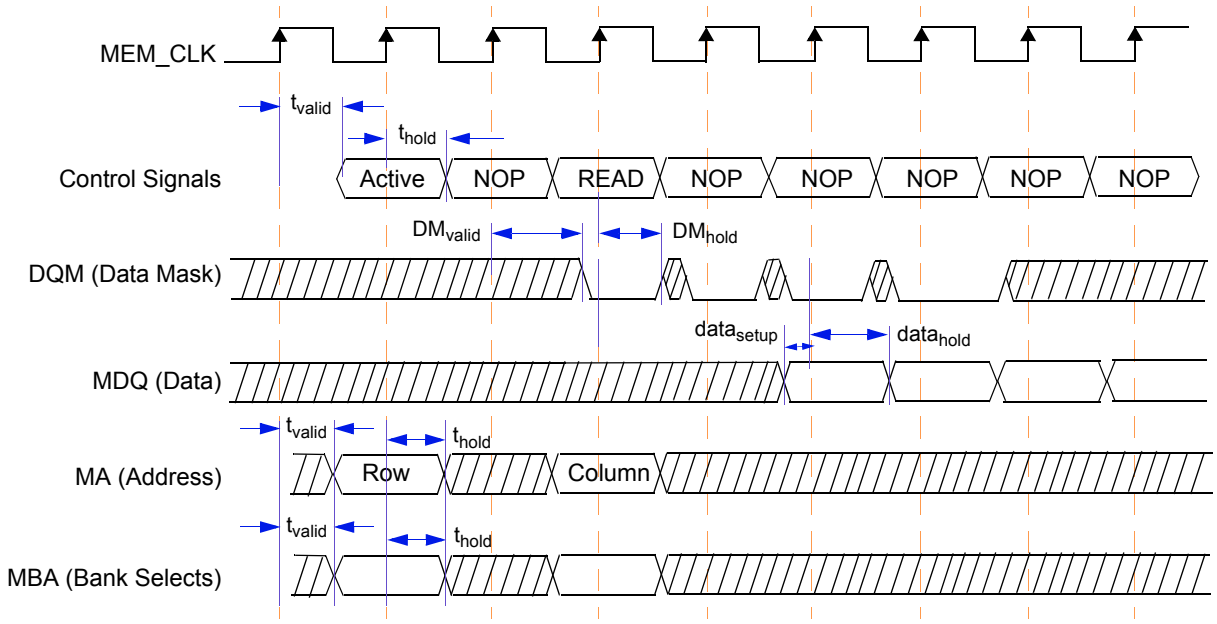
NOTES:
1. The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2. This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3. Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3.5 SDRAM

3.3.5.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.25+0.4	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	t_{mem_clk}*0.25-0.7	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

3.3.5.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the Mem_clk from the Memory Controller and captured on the Mem_clk clock at the memory device.

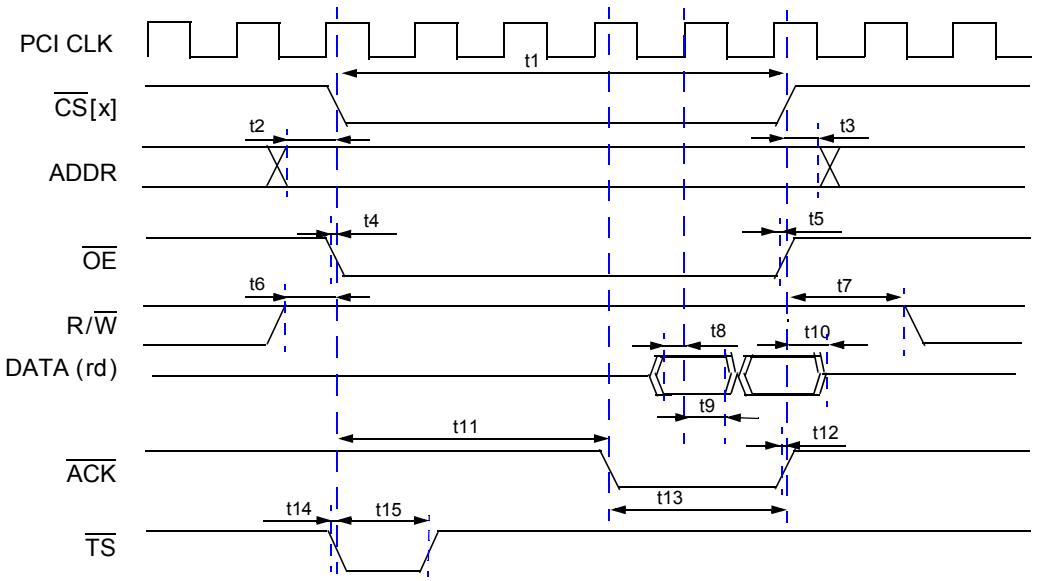


Figure 13. Timing Diagram—Burst Mode

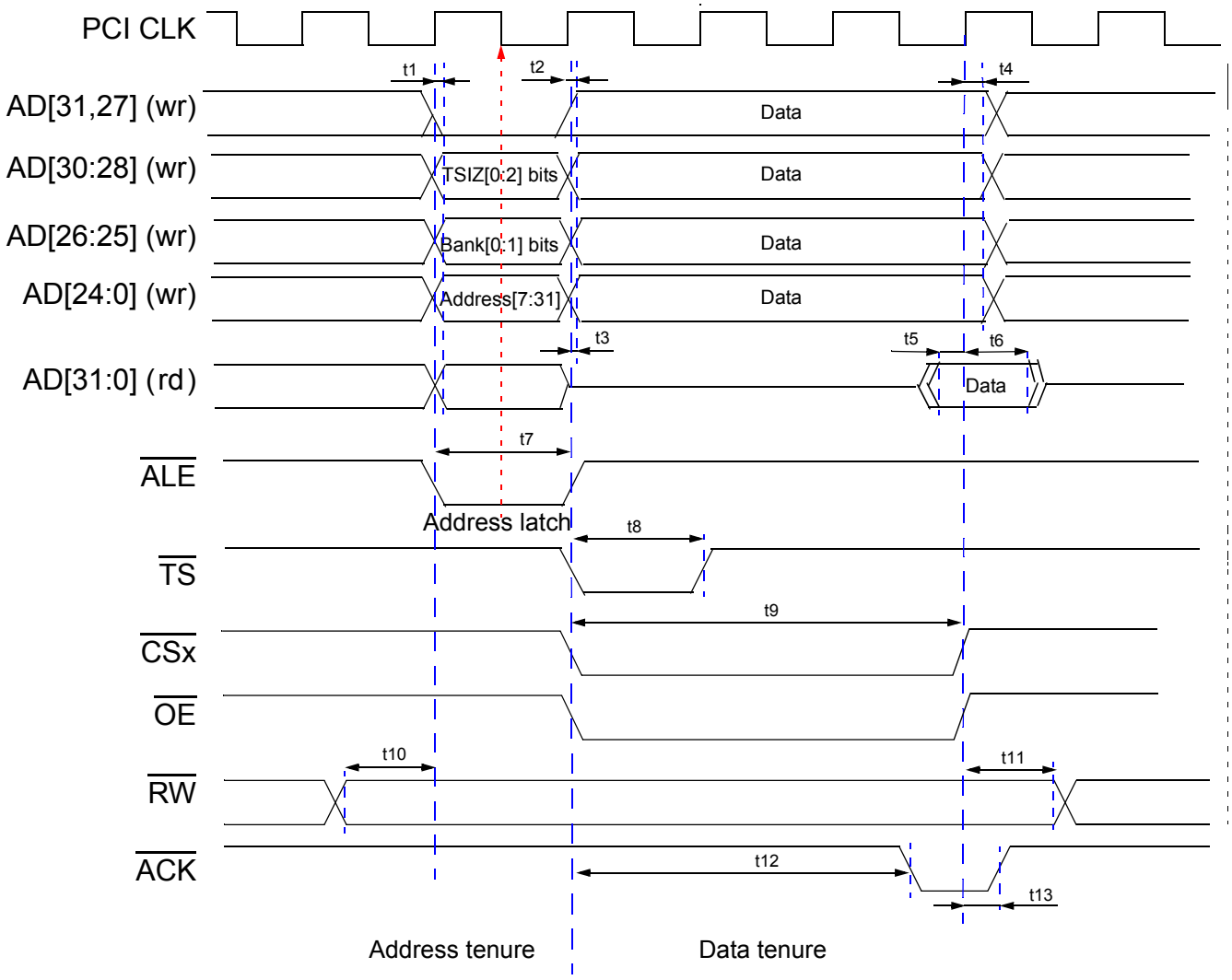
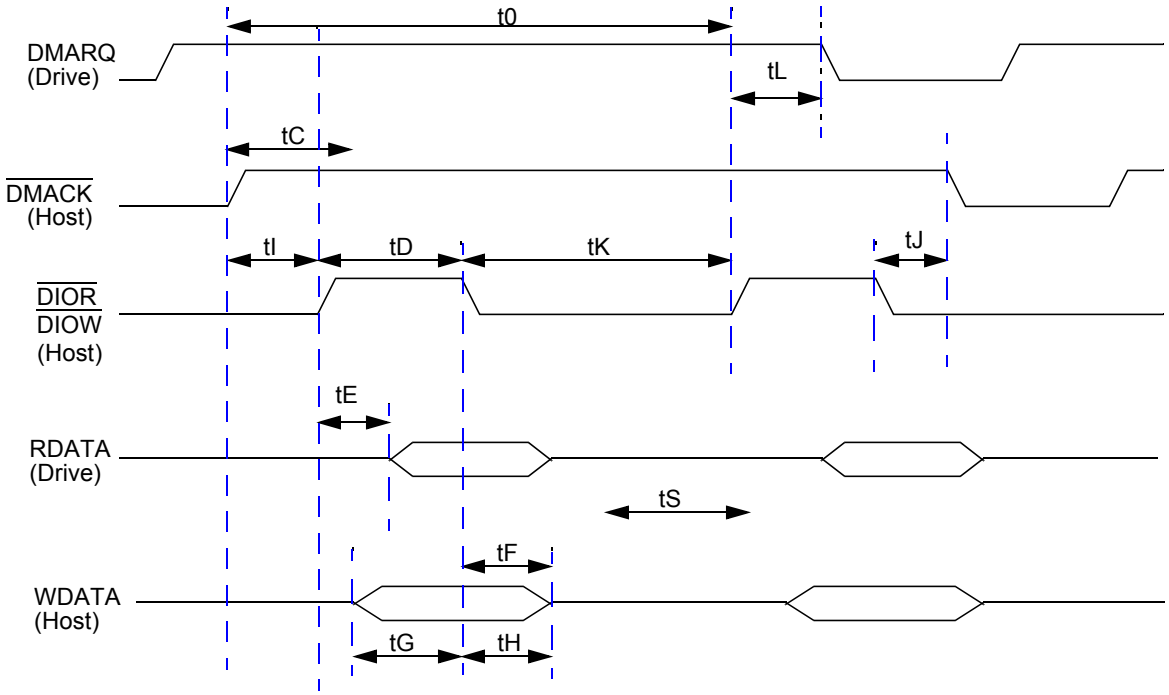


Figure 14. Timing Diagram—MUXed Mode

3.3.8 ATA

The MPC5200 ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nano seconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification [5] and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the MPC5200 User Manual [1].



NOTE: The direction of signal assertion is towards the top of the page, and the direction of negation is towards the bottom of the page, irrespective of the electrical properties of the signal.

Figure 16. Multiword DMA Timing

Table 29. Ultra DMA Timing Specification

Name	MODE 0 (ns)		MODE 1 (ns)		MODE 2 (ns)		Comment	SpecID
	Min	Max	Min	Max	Min	Max		
$(t)_{2CYC}$	240	—	160	—	120	—	Typical sustained average two cycle time. For information only, do not test.	A8.26
$(t)_{CYC}$	114	—	75	—	55	—	Cycle time allowing for asymmetry and clock variations from STROBE edge to STROBE edge	A8.27
$(t)_{2CYC}$	235	—	156	—	117	—	Two-cycle time allowing for clock variations, from rising edge to next rising edge or from falling edge to next falling edge of STROBE.	A8.28
$(t)_{DS}$	15	—	10	—	7	—	Data setup time at recipient.	A8.29
$(t)_{DH}$	5	—	5	—	5	—	Data hold time at recipient.	A8.30
$(t)_{DVS}$	70	—	48	—	34	—	Data valid setup time at sender, to STROBE edge.	A8.31
$(t)_{DVH}$	6	—	6	—	6	—	Data valid hold time at sender, from STROBE edge.	A8.32
$(t)_{FS}$	0	230	0	200	0	170	First STROBE time for drive to first negate DSTROBE from STOP during a data-in burst.	A8.33

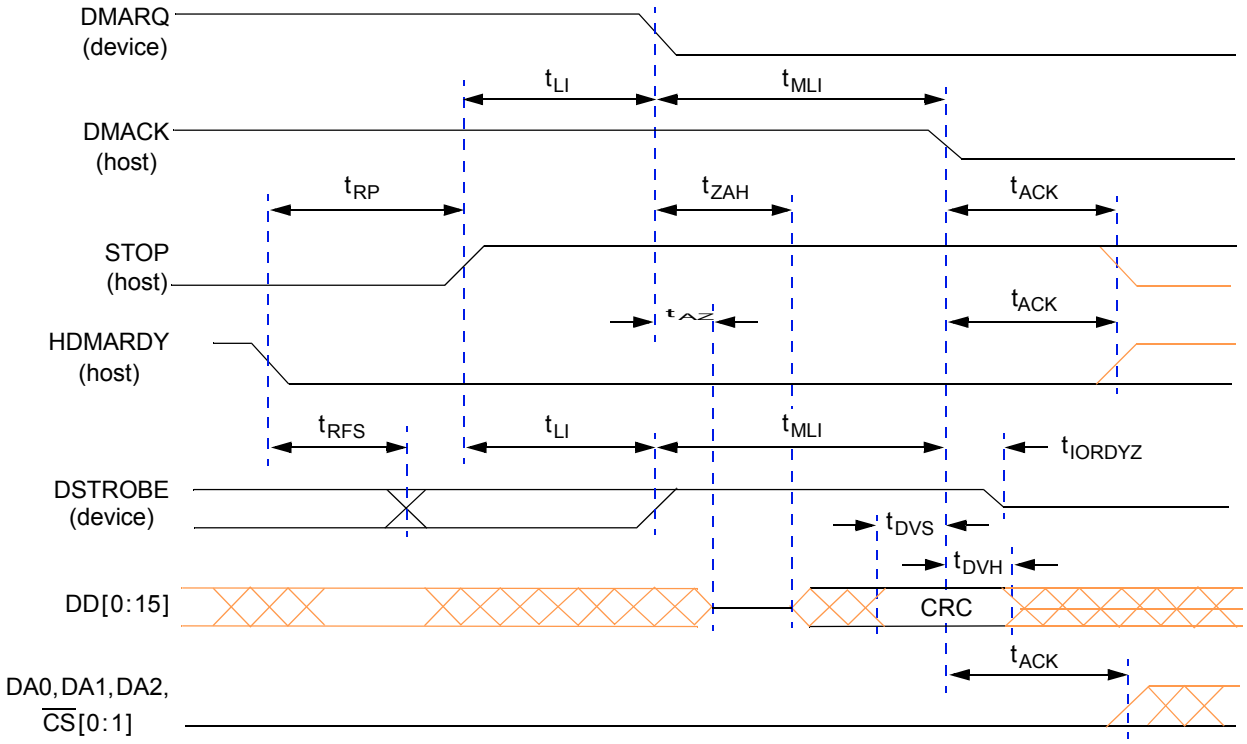


Figure 21. Timing Diagram—Host Terminating Ultra DMA Data In Burst

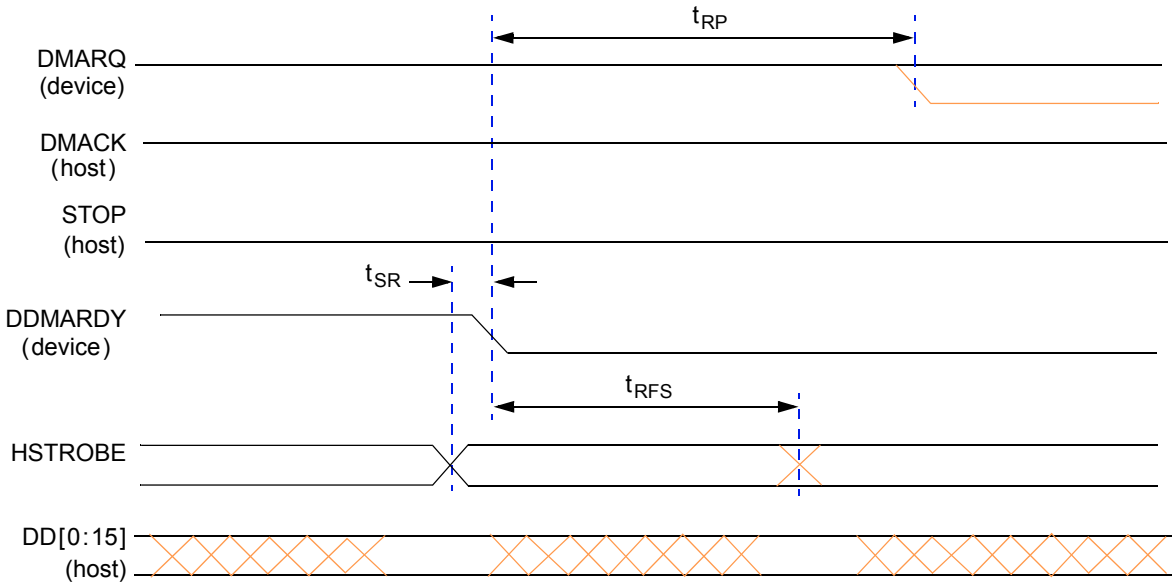


Figure 24. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

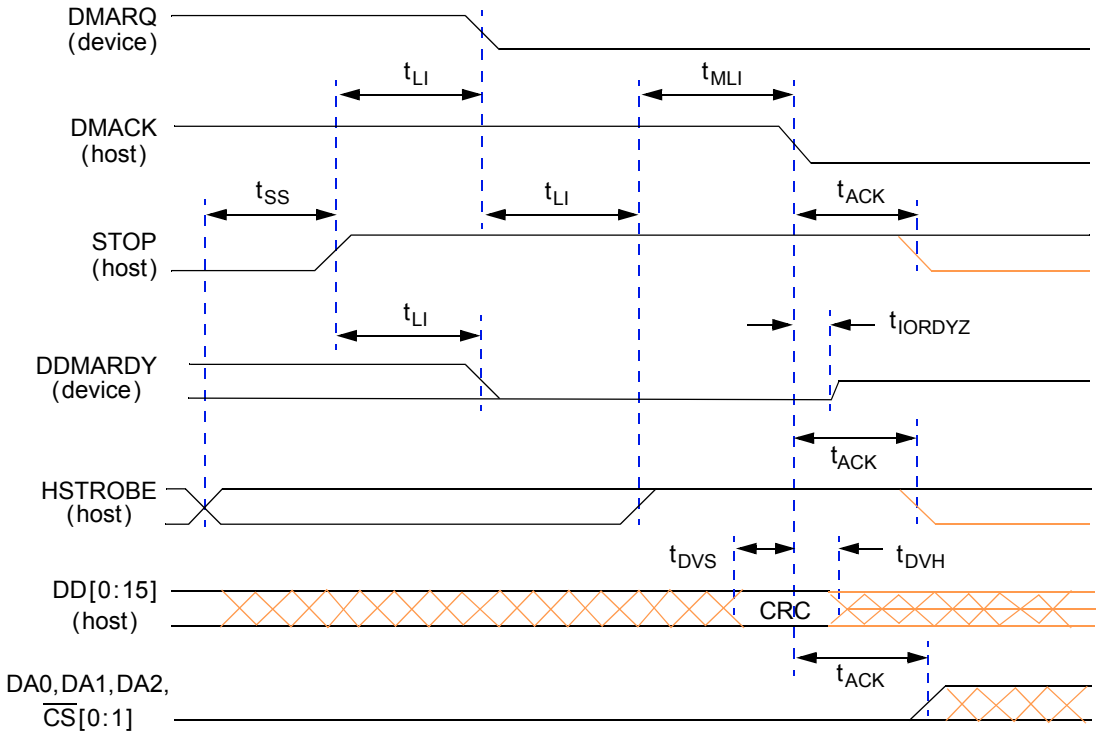


Figure 25. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

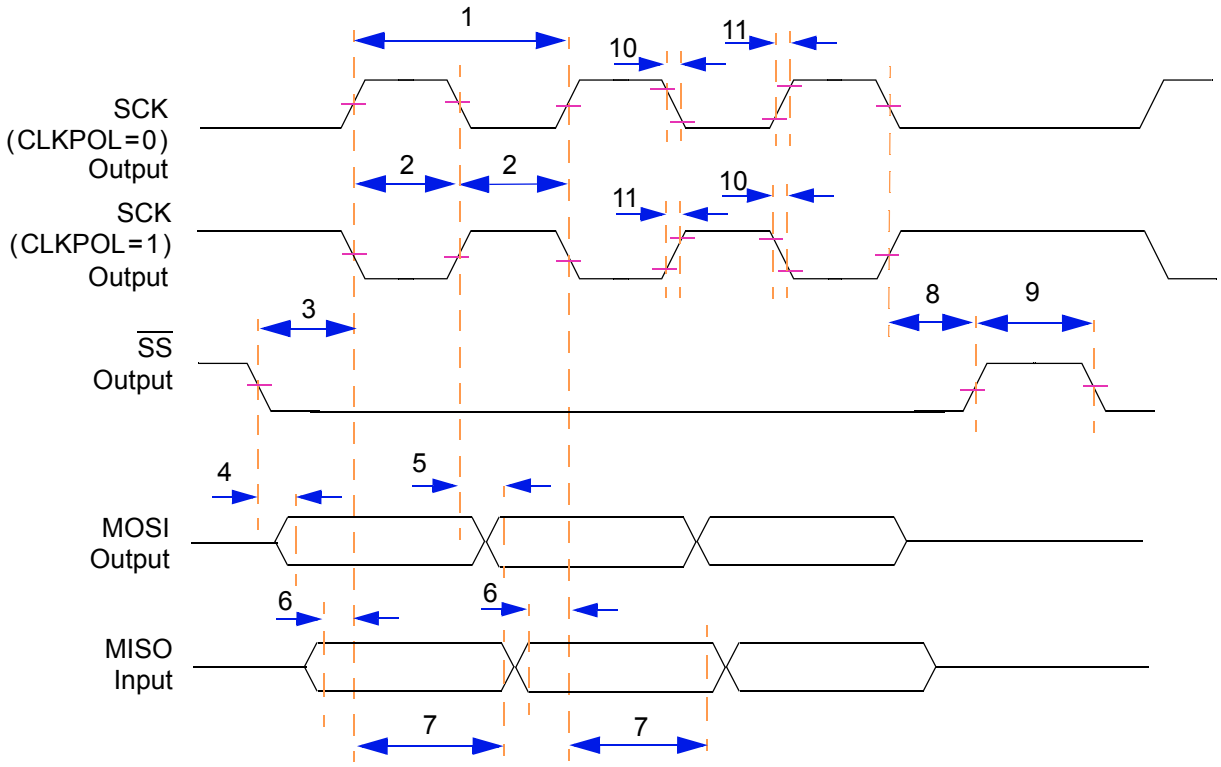


Figure 33. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 37. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.12
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.13
3	Slave select clock delay	15.0	—	ns	A11.14
4	Output Data valid after Slave Select ($\overline{SS}$)	—	50.0	ns	A11.15
5	Output Data valid after SCK	—	50.0	ns	A11.16
6	Input Data setup time	50.0	—	ns	A11.17
7	Input Data hold time	0.0	—	ns	A11.18
8	Slave disable lag time	15.0	—	ns	A11.19
9	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.20

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

Table 41. I²C Output Timing Specifications—SCL and SDA

Sym	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[3]	A13.8
2[1]	Clock low period	10	—	IP-Bus Cycle[3]	A13.9
3[2]	SCL/SDA rise time	—	7.9	ns	A13.10
4[1]	Data hold time	7	—	IP-Bus Cycle[3]	A13.11
5[1]	SCL/SDA fall time	—	7.9	ns	A13.12
6[1]	Clock high time	10	—	IP-Bus Cycle[3]	A13.13
7[1]	Data setup time	2	—	IP-Bus Cycle[3]	A13.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[3]	A13.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[3]	A13.16

NOTES:
1. Programming IFDR with the maximum frequency (IFDR=0x20) results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.
2. Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values
3. Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

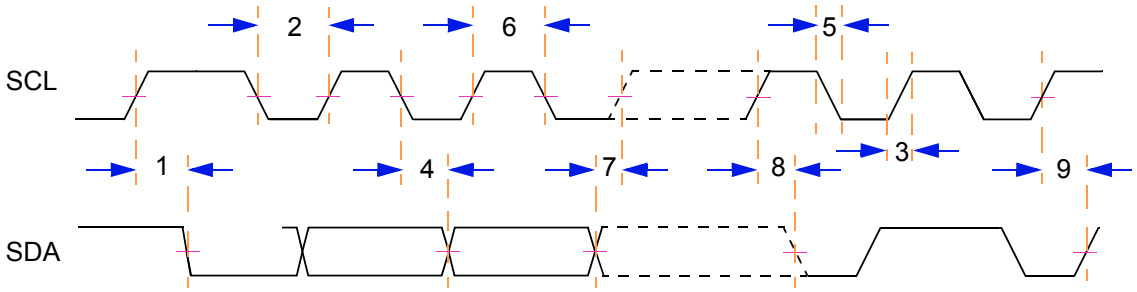


Figure 37. Timing Diagram—I²C Input/Output

3.3.14 J1850

See the MPC5200 User Manual [1].

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

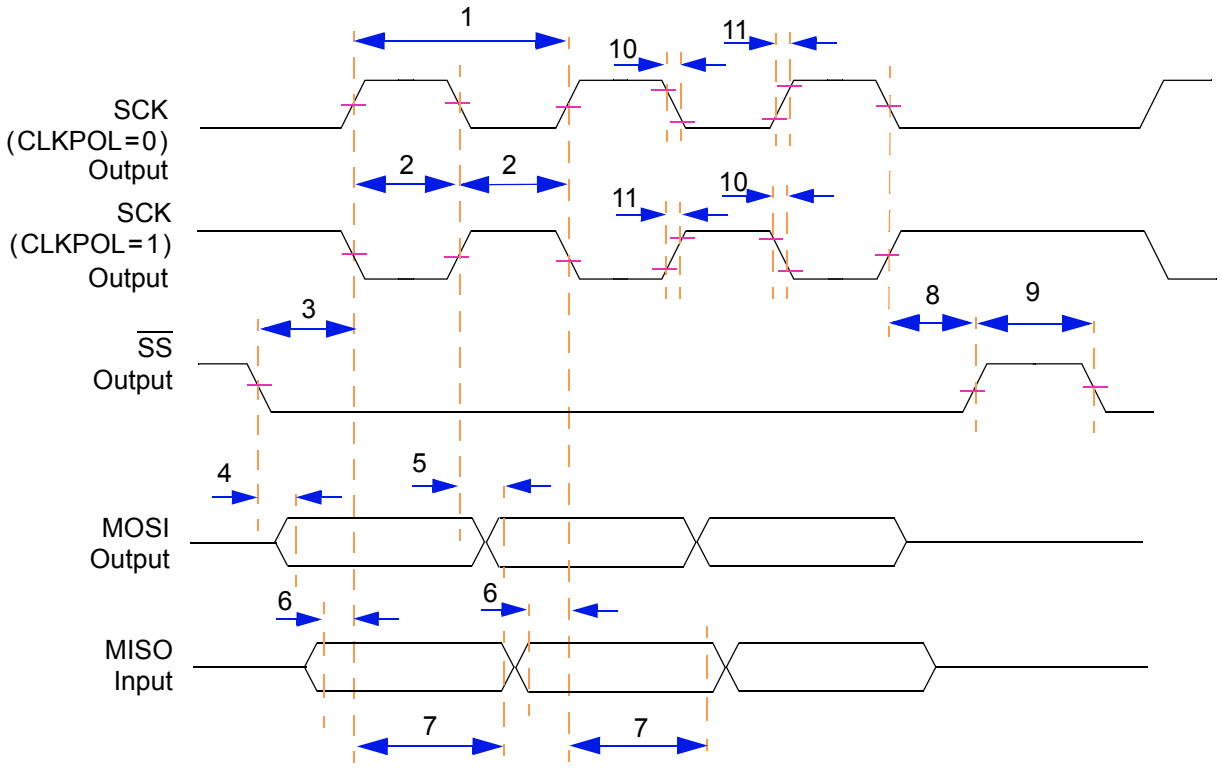
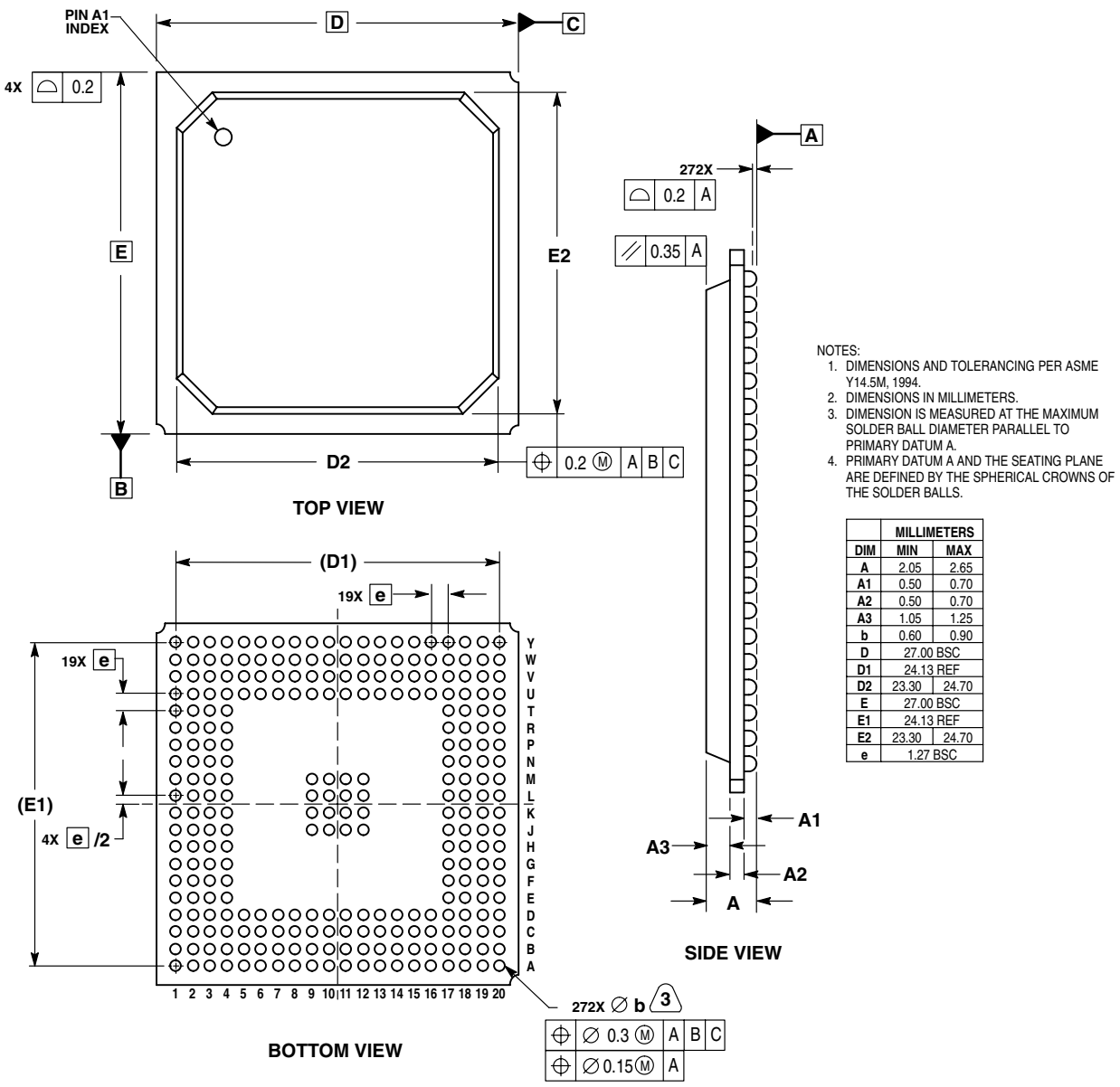


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

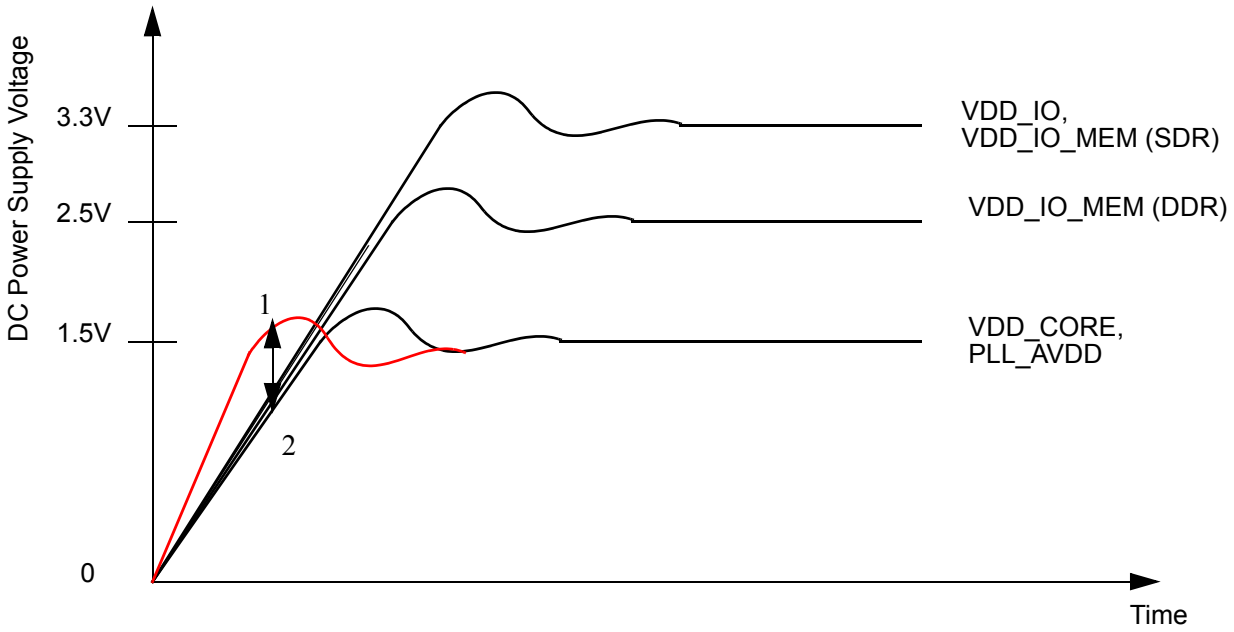
	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135A–01
ISSUE B

Figure 51. Mechanical Dimensions and Pinout Assignments for the MPC5200, 272 TE-PBGA

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_2	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	TTL	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	



Note:

1. VDD_CORE should not exceed VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V at any time, including power-up.
2. It is recommended that VDD_CORE/PLL_AVDD should track VDD_IO/VDD_IO_MEM up to 0.9 V then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (VDD_IO, VDD_IO_MEM, VDD_CORE, or PLL_AVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 52. Supply Voltage Sequencing

The relationship between VDD_IO_MEM and VDD_IO is non-critical during power-up and power-down sequences. Both VDD_IO_MEM (2.5 V or 3.3 V) and VDD_IO are specified relative to VDD_CORE.

5.1.1 Power Up Sequence

If VDD_IO/VDD_IO_MEM are powered up with the VDD_CORE at 0V, the sense circuits in the I/O pads will cause all pad output drivers connected to the VDD_IO/VDD_IO_MEM to be in a high-impedance state. There is no limit to how long after VDD_IO/VDD_IO_MEM powers up before VDD_CORE must power up. VDD_CORE should not lead the VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

Use one microsecond or slower rise time for all supplies.

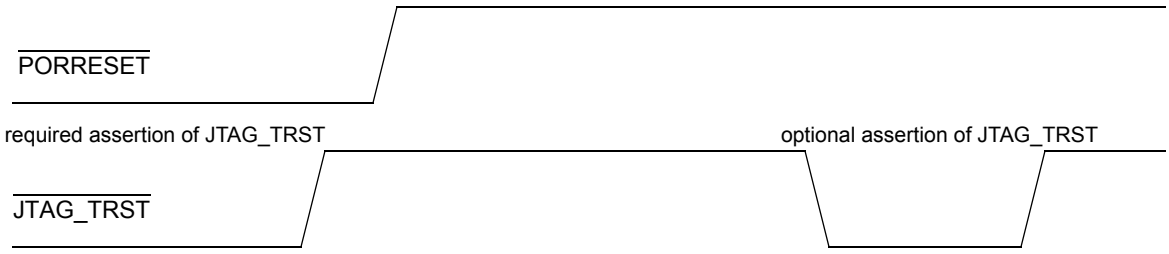


Figure 54. PORRESET vs. JTAG_TRST

5.4.1.2 Connecting JTAG_TRST

The wiring of the JTAG_TRST depends on the existence of a board-related debug interface (see Table 53 below).

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200.

5.4.2 G2_LE COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.4.2.1 Boards interfacing the JTAG port via a COP connector

The MPC5200 functional pin interface and internal logic provides access to the embedded G2_LE processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset		10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset		10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O

Table 53. COP/BDM Interface Signals (continued)

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
8	—	N/C	—	—	—
7	JTAG_TCK	tck	100k Pull-Up	10k Pull-Up	O
6	—	VDD[2]	—	—	—
5	See Note [3].	halted[3]	—	—	I
4	$\overline{\text{JTAG\_TRST}}$	trst	100k Pull-Up	10k Pull-Up	O
3	JTAG_TDI	tdi	100k Pull-Up	10k Pull-Up	O
2	See Note [4].	qack[4]	—	—	O
1	JTAG_TDO	tdo	—	—	I

NOTES:
1 With respect to the emulator tool's perspective:
Input is really an output from the embedded G2_LE core.
Output is really an input to the core.
2 From the board under test, power sense for chip power.
3 HALTED is not available from G2_LE core.
4 Input to the G2_LE core to enable/disable soft-stop condition during breakpoints. MPC5200 internal ties core_qack_ to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector, which accesses the JTAG interface and which needs to reset the JTAG module, simply wiring $\overline{\text{JTAG\_TRST}}$ and $\overline{\text{PORRESET}}$ is not recommended.

To reset the MPC5200 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5200. The circuitry shown in Figure 55 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{JTAG\_TRST}}$ separately, while any other board sources can drive $\overline{\text{PORRESET}}$.

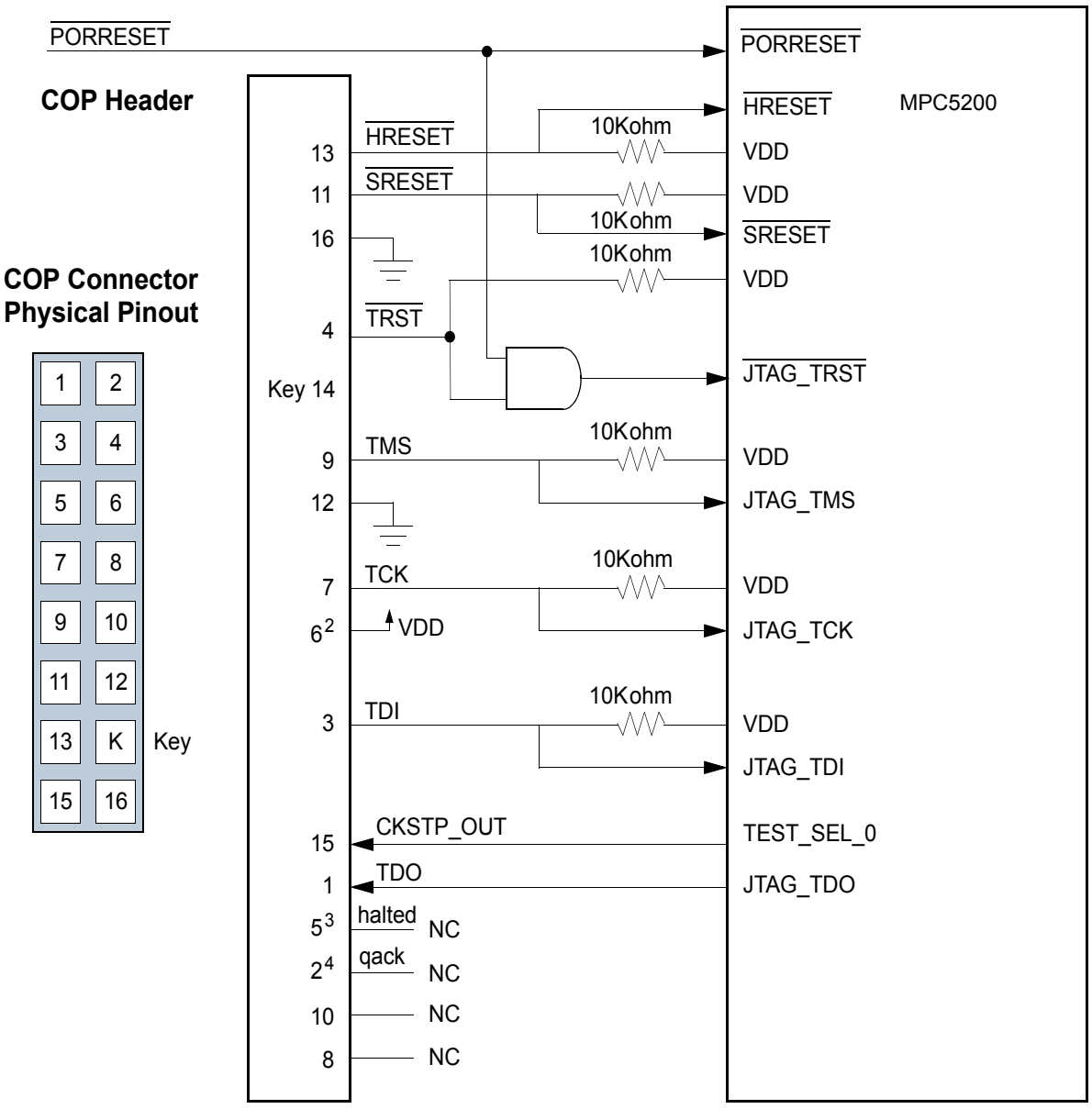


Figure 55. COP Connector Diagram

6 Ordering Information

Table 54. Ordering Information

Part Number	Speed	Ambient Temp	Qualification
MPC5200BV400	400	0C to 70C	Commercial
MPC5200CBV266	266	-40C to 85C	Industrial
MPC5200CBV400	400	-40C to 85C	Industrial
SPC5200CBV400	400	-40C to 85C	Automotive - AEC

7 Document Revision History

Table 55 provides a revision history for this hardware specification.

Table 55. Document Revision History

Rev. No.	Substantive Change(s)
0.1	First Preliminary release with some TBD's in spec tables (6/2003)
0.2	Added AC specs for missing modules, power-on sequence, misc other updates (7/2003)
0.2.1	Corrected maximum core operating frequency (7/2003)
0.3	Added Memory Interface Timing values, misc other updates (8/2003)
1.0	Added Information about JTAG_TRST (11/2003)
2.0	Added Power Numbers (Section 3.1.5), updated Oscillator and PLL Characteristics (Section 3.2), updated SDRAM AC Characteristics (Section 3.3.5)
3.0	Change to Freescale brand and format (8/2004)
4.0	Updates to LPC timing, DDR SDRAM timing, JTAG section, replaced TBD's (1/2005)
	Rev 4 has been regenerated with the new Freescale appearance guidelines, the title was changed and the reference to www.mobilegt.com in the first paragraph (Note) was changed to www. freescale.com (3/2006).

For more detailed information, refer to the following documentation:

[1] MPC5200 User Manual MPC5200UM

[2] PowerPC Microprocessor Family: The Programming Environments for 32-bit Microprocessors, Rev. 2: MPCFPE32B/AD

[3] G2 Core Reference Manual, Rev. 0: G2CORERM/D

[4] PCI Local Bus Specification, Revision 2.2, December 18, 1998

[5] ANSI ATA-4 Specification

[6] IEEE 802.3 Specification (ETHERNET)

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