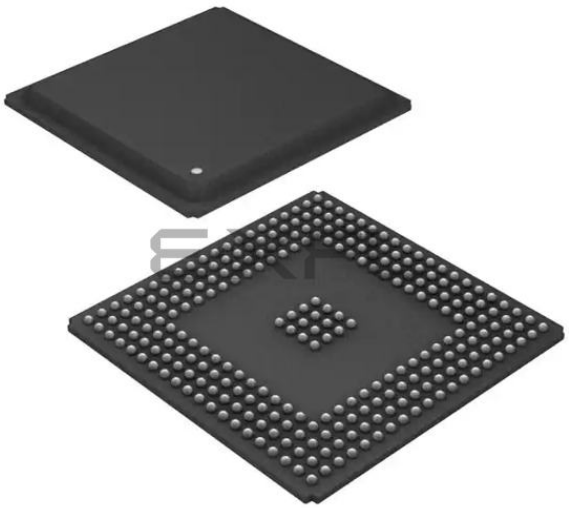

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cbv400r2

2 Features

Key features are shown below.

- MPC603e series G2_LE core
  - Superscalar architecture
  - 760 MIPS at 400 MHz (-40 to +85 ^{o}C)
  - 16 k Instruction cache, 16 k Data cache
  - Double precision FPU
  - Instruction and Data MMU
  - Standard and Critical interrupt capability
- SDRAM / DDR Memory Interface
  - up to 132-MHz operation
  - SDRAM and DDR SDRAM support
  - 256-MByte addressing range per CS, two CS available
  - 32-bit data bus
  - Built-in initialization and refresh
- Flexible multi-function External Bus Interface
  - Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
  - 8 programmable Chip Selects
  - Non multiplexed data access using 8/16/32 bit databus with up to 26-bit address
  - Short or Long Burst capable
  - Multiplexed data access using 8/16/32 bit databus with up to 25-bit address
- Peripheral Component Interconnect (PCI) Controller
  - Version 2.2 PCI compatibility
  - PCI initiator and target operation
  - 32-bit PCI Address/Data bus
  - 33- and 66-MHz operation
  - PCI arbitration function
- ATA Controller
  - Version 4 ATA compatible external interface—IDE Disk Drive connectivity
- BestComm DMA subsystem
  - Intelligent virtual DMA Controller
  - Dedicated DMA channels to control peripheral reception and transmission
  - Local memory (SRAM 16 kBytes)
- 6 Programmable Serial Controllers (PSC), configurable for the following:
  - UART or RS232 interface

3 Electrical and Thermal Characteristics

3.1 DC Electrical Characteristics

3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200 DC Electrical characteristics. Table 1 gives the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Min	Max	Unit	SpecID
Supply voltage - G2_LE core and peripheral logic	VDD_CORE	–0.3	1.8	V	D1.1
Supply voltage - I/O buffers	VDD_IO, VDD_MEM_IO	–0.3	3.6	V	D1.2
Supply voltage - System APLL	SYS_PLL_AVDD	–0.3	2.1	V	D1.3
Supply voltage - G2_LE APLL	CORE_PLL_AVDD	–0.3	2.1	V	D1.4
Input voltage (VDD_IO)	Vin	–0.3	VDD_IO + 0.3	V	D1.5
Input voltage (VDD_MEM_IO)	Vin	–0.3	VDD_MEM_IO + 0.3	V	D1.6
Input voltage overshoot	Vinos	–	1.0	V	D1.7
Input voltage undershoot	Vinus	–	1.0	V	D1.8
Storage temperature range	Tstg	–55	150	°C	D1.9

NOTES:
1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

3.1.2 Recommended Operating Conditions

Table 2 gives the recommended operating conditions.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min[1]	Max[(1)]	Unit	SpecID
Supply voltage - G2_LE core and peripheral logic	VDD_CORE	1.42	1.58	V	D2.1
Supply voltage - standard I/O buffers	VDD_IO	3.0	3.6	V	D2.2
Supply voltage - memory I/O buffers (SDR)	$VDD\_MEM\_IO_{SDR}$	3.0	3.6	V	D2.3
Supply voltage - memory I/O buffers (DDR)	$VDD\_MEM\_IO_{DDR}$	2.42	2.63	V	D2.4
Supply voltage - System APLL	SYS_PLL_AVDD	1.42	1.58	V	D2.5
Supply voltage - G2_LE APLL	CORE_PLL_AVDD	1.42	1.58	V	D2.6
Input voltage - standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage - memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	Vin = 0 or VDD_IO/VDD_IO_MEM$_{SDR}$ (depending on input type [1])	I_{IN}	—	±10	µA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.14
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor - memory I/O buffers	PULLUP_MEM VDD_IO_MEM$_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent[2] VDD_IO_MEM$_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin[3]		I_{CS}	-1.0	1.0	mA	D3.23
Capacitance	Vin = 0V, f = 1 MHz	C_{in}	—	15	pF	D3.24

NOTES:
1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.
2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.
3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200 Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3V	8	8	mA	D3.26

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The G2_LE core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The G2_LE core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

3.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	100	µs	O1.2

3.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	1	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	T_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	2	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	3	—	—	100	µs	O3.5

NOTES:
1. The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2. This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3. Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 G2_LE Core PLL Electrical Characteristics

The internal clocking of the G2_LE core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. G2_LE PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
G2_LE frequency	f_{core}	1	50	—	550	MHz	O4.1
G2_LE cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
G2_LE VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
G2_LE input clock frequency	f_{XLB_CLK}		25	—	367	MHz	O4.4
G2_LE input clock cycle time	t_{XLB_CLK}		2.73	—	50.0	ns	O4.5
G2_LE input clock jitter	t_{jitter}	2	—	—	150	ps	O4.6
G2_LE PLL relock time	t_{lock}	3	—	—	100	µs	O4.7

NOTES:
1 The XLB_CLK frequency and G2_LE PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and G2_LE PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.[1]	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).[2]	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

NOTES:
1 **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0-6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the MPC5200 User Manual [1].
2 SYS_XTAL_IN duty cycle is measured at V_M.

3.3.3 Resets

The MPC5200 has three reset pins:

- $\overline{\text{PORRESET}}$ - Power on Reset
- $\overline{\text{HRESET}}$ - Hard Reset
- $\overline{\text{SRESET}}$ - Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200 inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

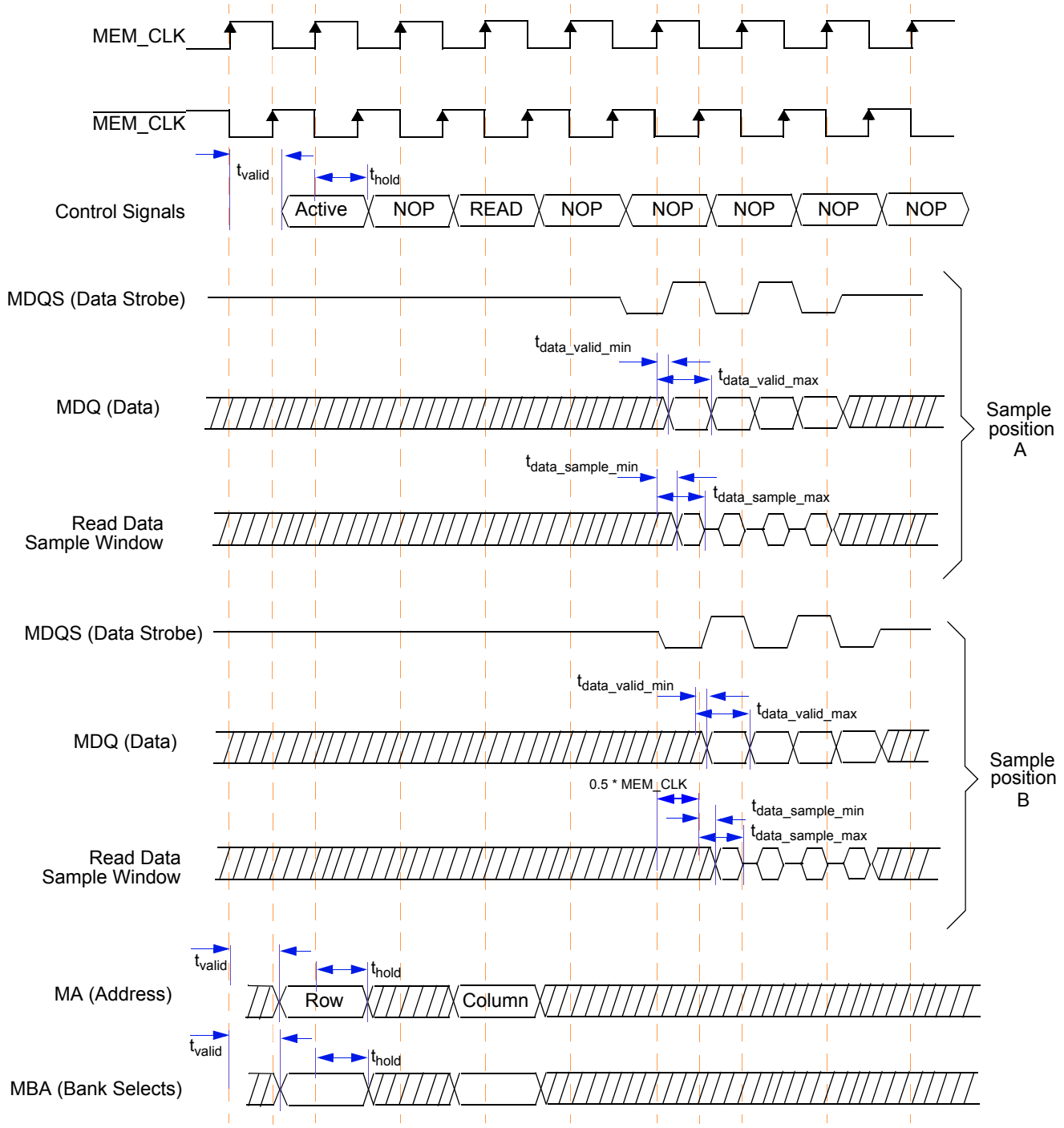
Table 14. Reset Pulse Width

Name	Description	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
$\overline{\text{PORRESET}}$	Power On Reset	$t_{VDD\_stable}+t_{up\_osc}+t_{lock}$	—	SYS_XTAL_IN	A3.1
$\overline{\text{HRESET}}$	Hardware Reset	4 clock cycles	—	SYS_XTAL_IN	A3.2
$\overline{\text{SRESET}}$	Software Reset	4 clock cycles	—	SYS_XTAL_IN	A3.3

Notes:
1. For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.
2. The t_{VDD_stable} describes the time which is needed to get all power supplies stable.
3. For t_{lock}, refer to the Oscillator/PLL section of this specification for further details.
4. For t_{up_osc}, refer to the Oscillator/PLL section of this specification for further details.
5. Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.
6. The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data
Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the vaild MDQS signal

NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

3.3.7 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200. Maximum eight configurable Chip-selects are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:
WS = Wait State
DC = Dead Cycle
LB = Long Burst
DS = Data size in Byte
tPCIck = PCI clock period
tIPBIck = IPBI clock period

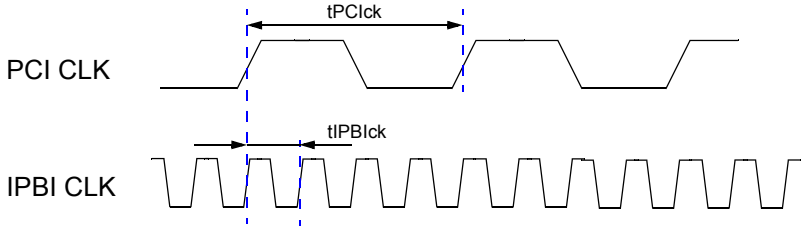


Figure 11. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

3.3.7.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.1
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.2
t_1	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns	1	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	-	ns	2	A7.5
t_4	OE assertion before CS assertion	-	0.4	ns		A7.6
t_5	OE negation before CS negation	-	0.4	ns		A7.7
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.8
t_7	RW hold after CS negation	t_{IPBIck}	-	ns		A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	-	ns		A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	-	ns		A7.11
t_{10}	DATA input setup before CS negation	2.8	-	ns		A7.12
t_{11}	DATA input hold after CS negation	0	(DC+1)*t_{PCIck}	ns		A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	-	ns	3	A7.14
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	3	A7.15

The MPC5200 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5200 operating frequency (IP bus clock frequency)
- Internal MPC5200 bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5200. See the MPC5200 User Manual [1].

NOTE

All output timing numbers are specified for nominal 50 pF loads.

Table 27. PIO Mode Timing Specifications

	PIO Timing Parameter	Min/Max (ns)	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	SpecID
t0	Cycle Time	min	600	383	240	180	120	A8.1
t1	Address valid to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	70	50	30	30	25	A8.2
t2	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width 16-bit 8-bit	min min	165 290	125 290	100 290	80 80	70 70	A8.3
t2i	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ recovery time	min	—	—	—	70	25	A8.4
t3	$\overline{\text{DIOW}}$ data setup	min	60	45	30	30	20	A8.5
t4	$\overline{\text{DIOW}}$ data hold	min	30	20	15	10	10	A8.6
t5	$\overline{\text{DIOR}}$ data setup	min	50	35	20	20	20	A8.7
t6	$\overline{\text{DIOR}}$ data hold	min	5	5	5	5	5	A8.8
t9	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to address valid hold	min	20	15	10	10	10	A8.9
tA	IORDY setup	max	35	35	35	35	35	A8.10
tB	IORDY pulse width	max	1250	1250	1250	1250	1250	A8.11

NOTE

Output timing was specified at a nominal 50 pF load.

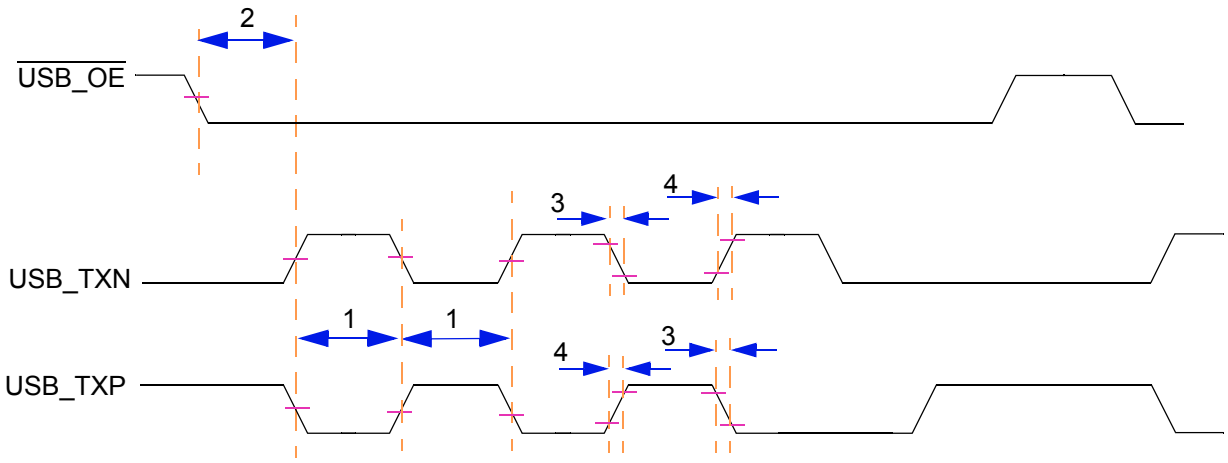


Figure 32. Timing Diagram—USB Output Line

3.3.11 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.1
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.2
3	Slave select clock delay	15.0	—	ns	A11.3
4	Output Data valid after Slave Select ($\overline{SS}$)	—	20.0	ns	A11.4
5	Output Data valid after SCK	—	20.0	ns	A11.5
6	Input Data setup time	20.0	—	ns	A11.6
7	Input Data hold time	20.0	—	ns	A11.7
8	Slave disable lag time	15.0	—	ns	A11.8
9	Sequential transfer delay	1	—	IP-Bus Cycle[1]	A11.9
10	Clock falling time	—	7.9	ns	A11.10
11	Clock rising time	—	7.9	ns	A11.11

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

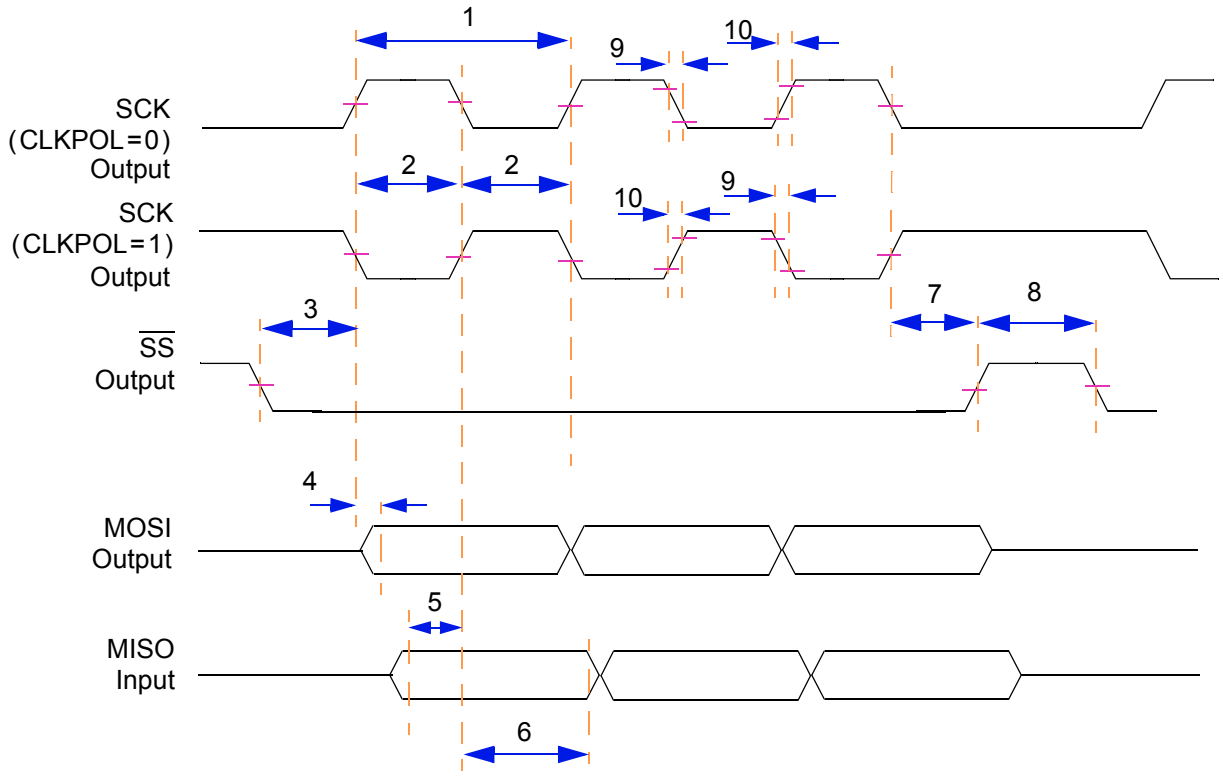


Figure 35. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 39. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.31
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.32
3	Slave select clock delay	15.0	—	ns	A11.33
4	Output data valid	—	50.0	ns	A11.34
5	Input Data setup time	50.0	—	ns	A11.35
6	Input Data hold time	0.0	—	ns	A11.36
7	Slave disable lag time	15.0	—	ns	A11.37
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.38

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

3.3.15 PSC

3.3.15.1 Codec Mode (8,16,24 and 32-bit) / I²S Mode

Table 42. Timing Specifications—8,16, 24 and 32-bit CODEC / I²S Master Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A15.1
2	Clock pulse width	—	50	—	%[1]	A15.2
3	Bit Clock fall time	—	—	7.9	ns	A15.3
4	Bit Clock rise time	—	—	7.9	ns	A15.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A15.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A15.6
7	Output Data valid after clock edge	—	—	9.3	ns	A15.7
8	Input Data setup time	6.0	—	—	ns	A15.8

NOTES:
1 Bit Clock cycle time

NOTE

Output timing was specified at a nominal 50 pF load.

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

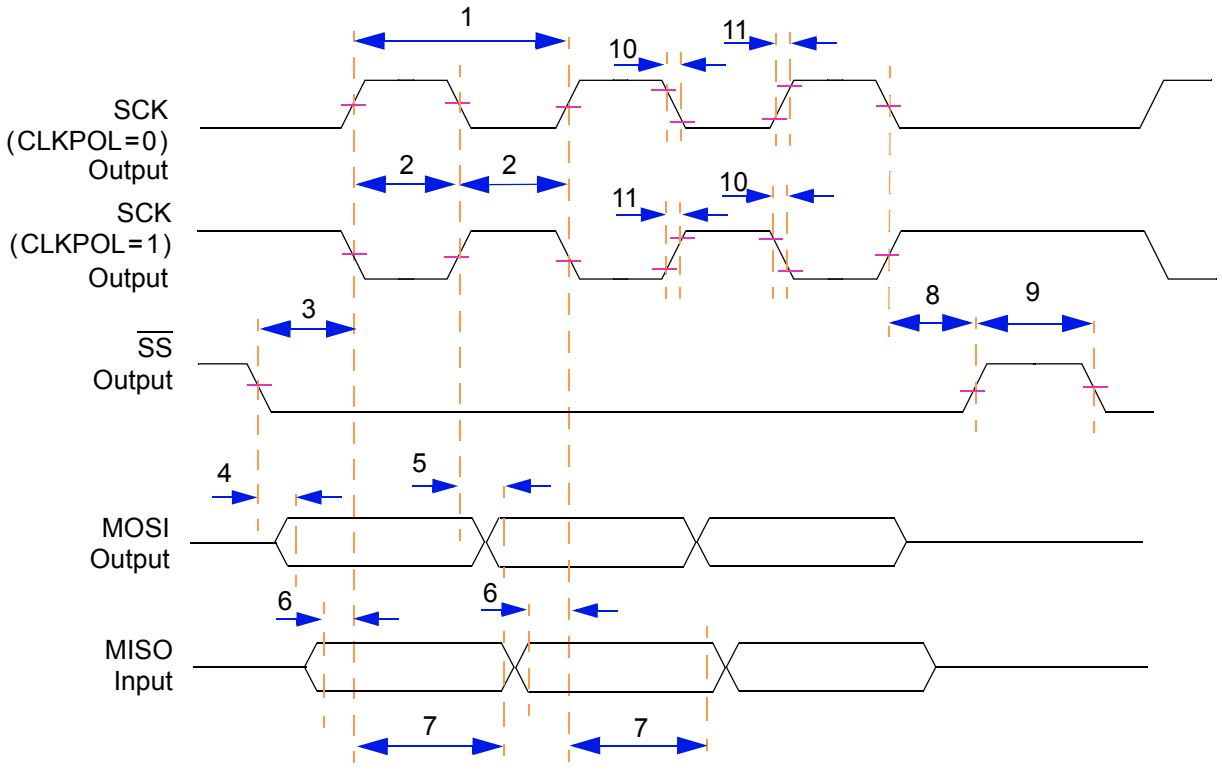


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.37
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.38
3	Slave select clock delay	1.0	—	ns	A15.39
4	Input Data setup time	1.0	—	ns	A15.40
5	Input Data hold time	1.0	—	ns	A15.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A15.42
7	Output data valid after SCK	—	14.0	ns	A15.43
8	Slave disable lag time	0.0	—	ns	A15.44
9	Minimum Sequential Transfer delay = 2 * IP Bus clock cycle time	30.0	—	—	A15.45

NOTE

Output timing was specified at a nominal 50 pF load.

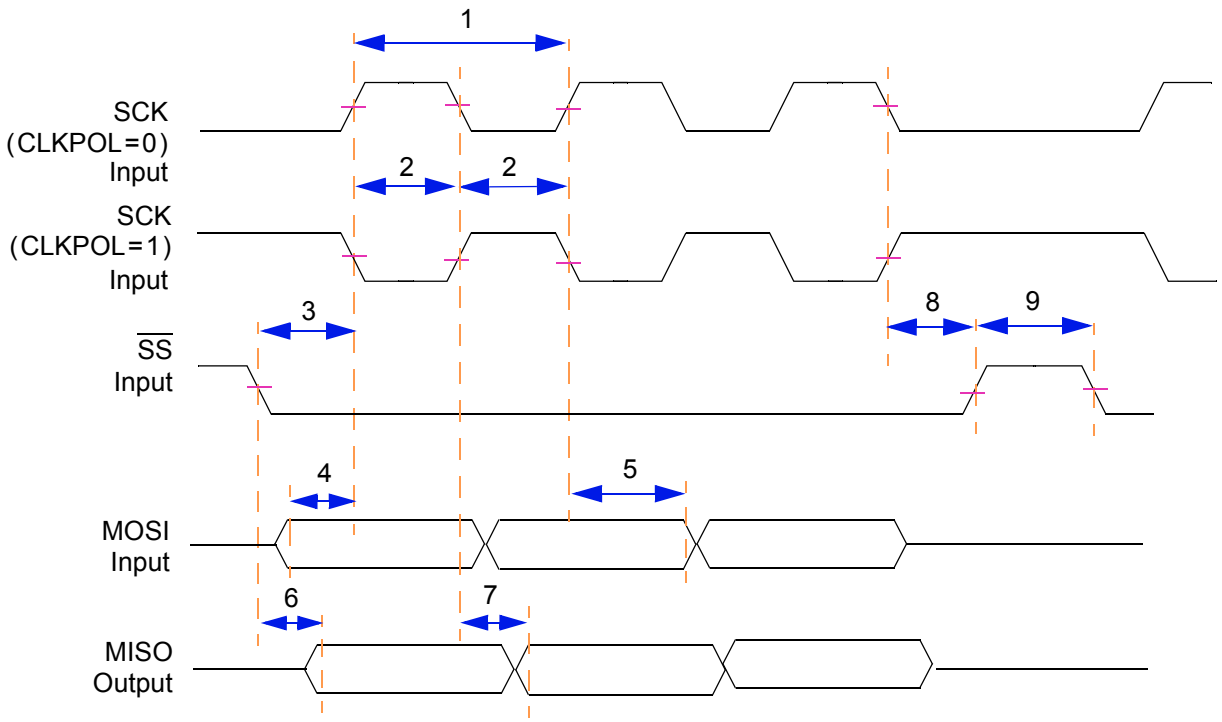


Figure 43. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.56
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.57
3	Slave select clock delay	0.0	—	ns	A15.58
4	Output data valid	—	14.0	ns	A15.59
5	Input Data setup time	2.0	—	ns	A15.60
6	Input Data hold time	1.0	—	ns	A15.61
7	Slave disable lag time	0.0	—	ns	A15.62
8	Minimum Sequential Transfer delay = 2 * IP-Bus clock cycle time	30.0	—	ns	A15.63

NOTE

Output timing was specified at a nominal 50 pF load.

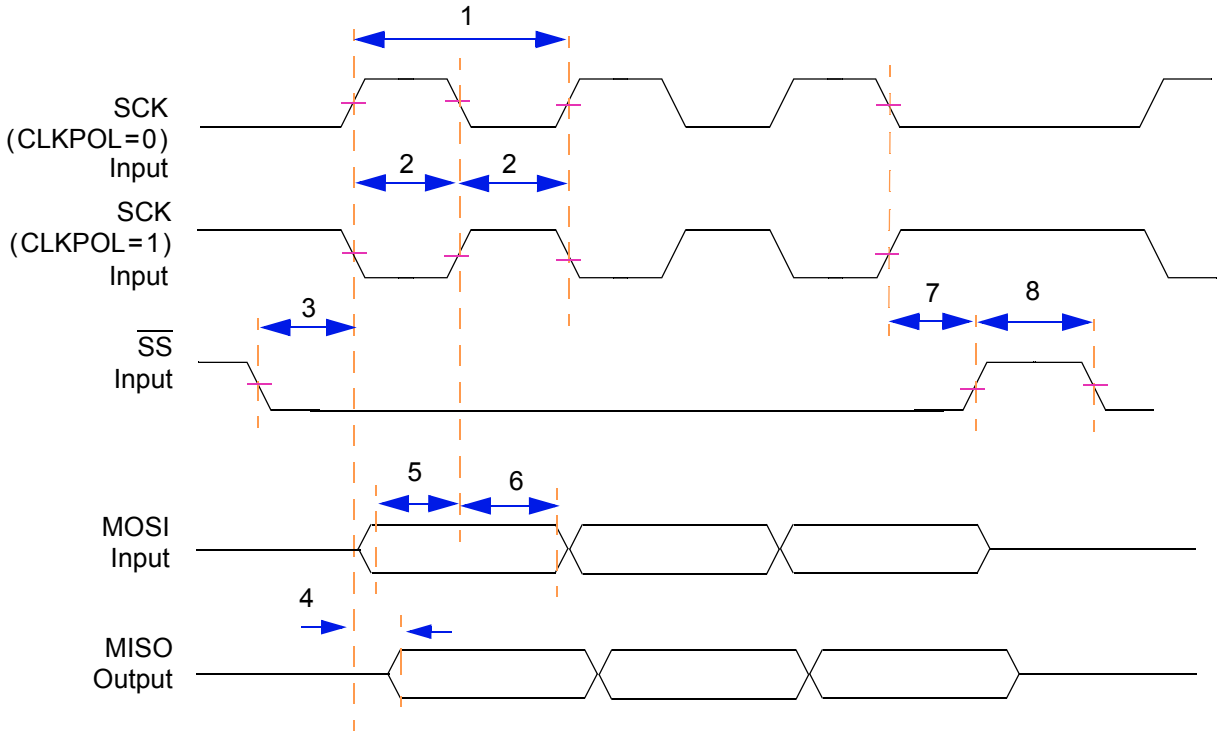


Figure 45. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

3.3.16 GPIOs and Timers

3.3.16.1 General and Asynchronous Signals

The MPC5200 contains several sets if I/Os that do not require special setup, hold, or valid requirements. Most of these are asynchronous to the system clock. The following numbers are provided for test and validation purposes only, and they assume a 133 MHz internal bus frequency.

Figure 46 shows the GPIO Timing Diagram. Table 50 gives the timing specifications.

Table 50. Asynchronous Signals

Sym	Description	Min	Max	Units	SpecID
t_{CK}	Clock Period	7.52	—	ns	A16.1
t_{IS}	Input Setup for Async Signal	12	—	ns	A16.2
t_{IH}	Input Hold for Async Signals	1	—	ns	A16.3
t_{DV}	Output Valid	—	15.33	ns	A16.4
t_{DH}	Output Hold	1	—	ns	A16.5

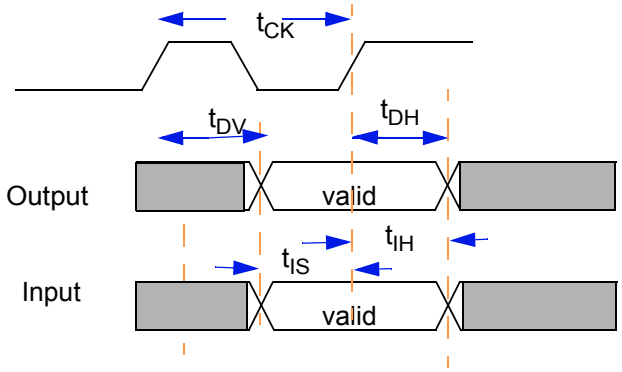


Figure 46. Timing Diagram—Asynchronous Signals

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, TX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
TIMER_1		I/O	VDD_IO	DRV4	TTL	
TIMER_2	MOSI	I/O	VDD_IO	DRV4	TTL	
TIMER_3	MISO	I/O	VDD_IO	DRV4	TTL	
TIMER_4	SS	I/O	VDD_IO	DRV4	TTL	
TIMER_5	SCK	I/O	VDD_IO	DRV4	TTL	
TIMER_6		I/O	VDD_IO	DRV4	TTL	
TIMER_7		I/O	VDD_IO	DRV4	TTL	
Clock						
SYS_XTAL_IN		Input	VDD_IO			
SYS_XTAL_OUT		Output	VDD_IO			
RTC_XTAL_IN		Input	VDD_IO			
RTC_XTAL_OUT		Output	VDD_IO			
Misc						
$\overline{\text{PORRESET}}$		Input	VDD_IO	DRV4	Schmitt	
$\overline{\text{HRESET}}$		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
$\overline{\text{SRESET}}$		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
IRQ0		I/O	VDD_IO	DRV4	TTL	
IRQ1		I/O	VDD_IO	DRV4	TTL	
IRQ2		I/O	VDD_IO	DRV4	TTL	
IRQ3		I/O	VDD_IO	DRV4	TTL	
Test/Configuration						
SYS_PLL_TPA		I/O	VDD_IO	DRV4	TTL	
TEST_MODE_0		Input	VDD_IO	DRV4	TTL	
TEST_MODE_1		Input	VDD_IO	DRV4	TTL	
TEST_SEL_0		I/O	VDD_IO	DRV4	TTL	PULLUP
TEST_SEL_1		I/O	VDD_IO	DRV8	TTL	
JTAG_TCK	TCK	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDI	TDI	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDO	TDO	I/O	VDD_IO	DRV8	TTL	
JTAG_TMS	TMS	Input	VDD_IO	DRV4	TTL	PULLUP
$\overline{\text{JTAG\_TRST}}$	TRST	Input	VDD_IO	DRV4	TTL	PULLUP

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
Power and Ground						
VDD_IO		-				
VDD_MEM_IO		-				
VDD_CORE		-				
VSS_IO/CORE		-				
SYS_PLL_AVDD		-				
CORE_PLL_AVDD		-				

NOTES:
1 All “open drain” outputs of the MPC5200 are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200 I/O power rail if the external signal is driven above the MPC5200 I/O power rail voltage.

5 System Design Information

5.1 Power UP/Down Sequencing

Figure 52 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).

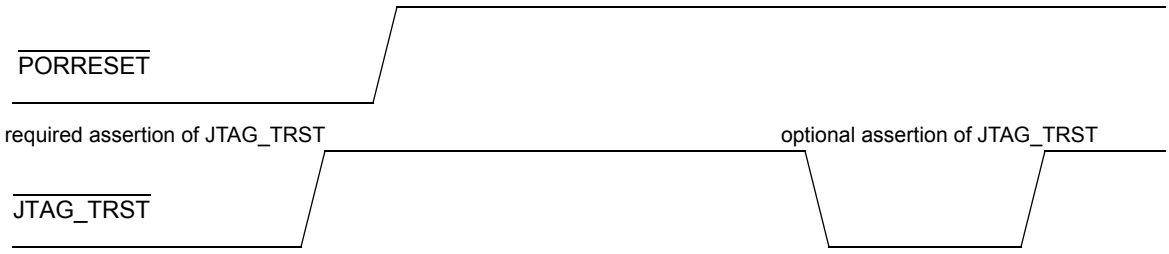


Figure 54. PORRESET vs. JTAG_TRST

5.4.1.2 Connecting JTAG_TRST

The wiring of the JTAG_TRST depends on the existence of a board-related debug interface (see Table 53 below).

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200.

5.4.2 G2_LE COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.4.2.1 Boards interfacing the JTAG port via a COP connector

The MPC5200 functional pin interface and internal logic provides access to the embedded G2_LE processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset		10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset		10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O