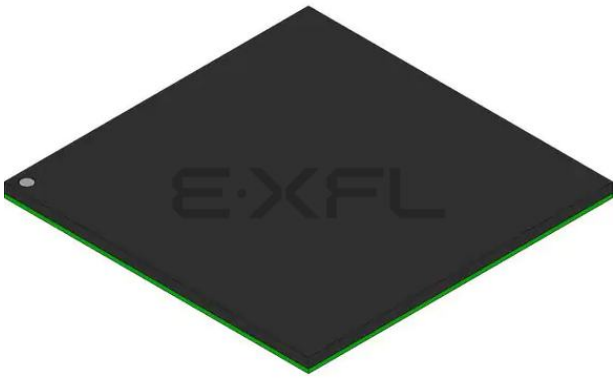

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Mounting Type	-
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  - JTAG (IEEE 1149.1 test access port)
  - Common On-chip Processor (COP) debug port
- On-board PLL and clock generation

Figure 1 shows a simplified MPC5200 block diagram.

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Min[1]	Max[(1)]	Unit	SpecID
Input voltage - memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	-40	+85	°C	D2.10
Extended ambient operating temperature range[3]	T_{Aext}	-40	+105	°C	D2.11
Die junction operating temperature range	Tj	-40	+115	°C	D2.12
Extended die junction operating temperature range	Tjext	-40	+125	°C	D2.13

NOTES:
1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.
2 Maximum G2_LE core operating frequency is 400 MHz
3 Maximum G2_LE core operating frequency is 264 MHz

3.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200 at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12

NOTE

Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

3.3.4 External Interrupts

The MPC5200 provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:

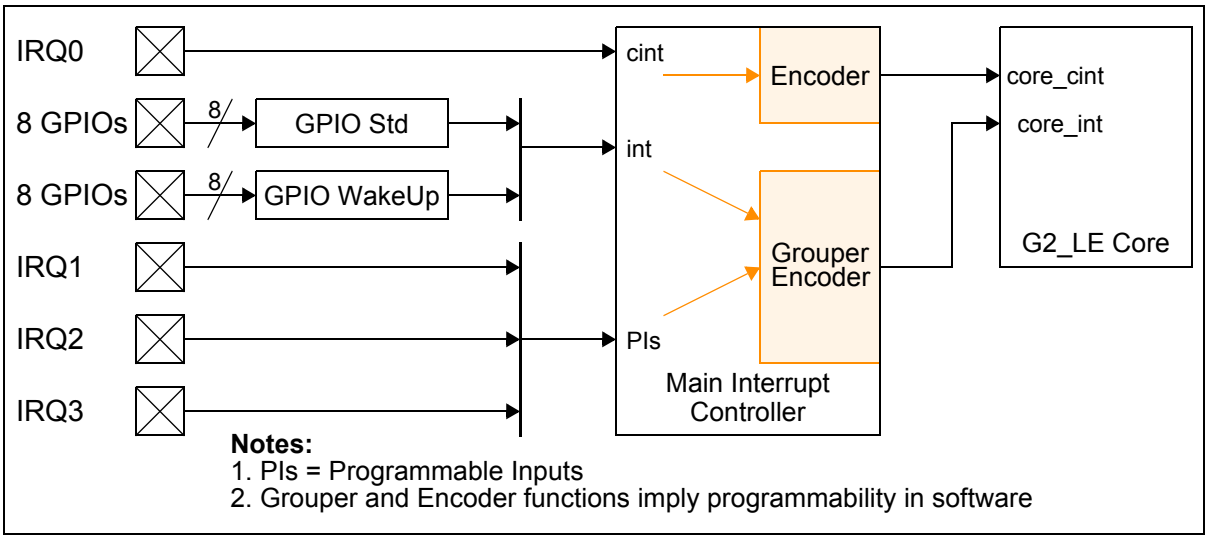


Figure 4. External interrupt scheme

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Note Table 16).

Table 16. External interrupt latencies

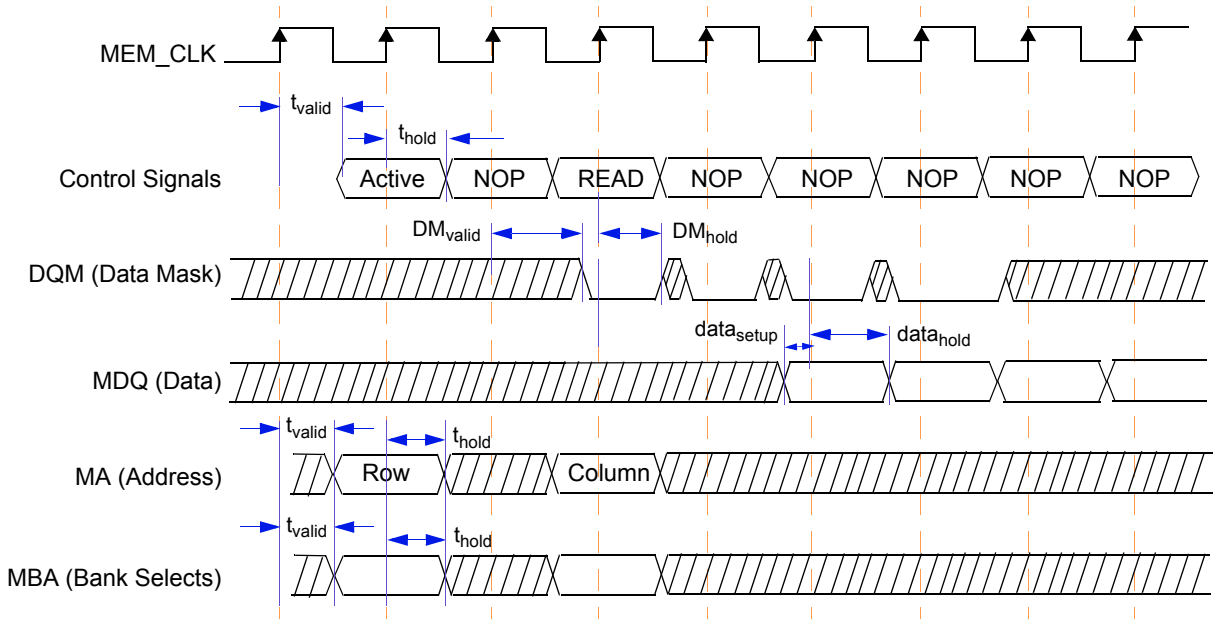
Interrupt Type	Pin Name	Clock Cycles	Reference Clock	Core Interrupt	SpecID
Interrupt Requests	IRQ0	10	IP_CLK	critical (cint)	A4.1
	IRQ0	10	IP_CLK	normal (int)	A4.2
	IRQ1	10	IP_CLK	normal (int)	A4.3
	IRQ2	10	IP_CLK	normal (int)	A4.5
	IRQ3	10	IP_CLK	normal (int)	A4.6

3.3.5 SDRAM

3.3.5.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.25+0.4	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	t_{mem_clk}*0.25-0.7	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

3.3.5.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the Mem_clk from the Memory Controller and captured on the Mem_clk clock at the memory device.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
T_{val}	CLK to Signal Valid Delay - bused signals	2	6	2	11	ns	1,2,3	A6.5
T_{val}(ptp)	CLK to Signal Valid Delay - point to point	2	6	2	12	ns	1,2,3	A6.6
T_{on}	Float to Active Delay	2		2		ns	1	A6.7
T_{off}	Active to Float Delay		14		28	ns	1	A6.8
T_{su}	Input Setup Time to CLK - bused signals	3		7		ns	3,4	A6.9
T_{su}(ptp)	Input Setup Time to CLK - point to point	5		10,12		ns	3,4	A6.10
T_{h}	Input Hold Time from CLK	0		0		ns	4	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification [4]. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.
2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification [4].
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification [4].

For Measurement and Test Conditions, see the PCI Local Bus Specification [4].

3.3.7 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200. Maximum eight configurable Chip-selects are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:
WS = Wait State
DC = Dead Cycle
LB = Long Burst
DS = Data size in Byte
tPCIck = PCI clock period
tIPBIck = IPBI clock period

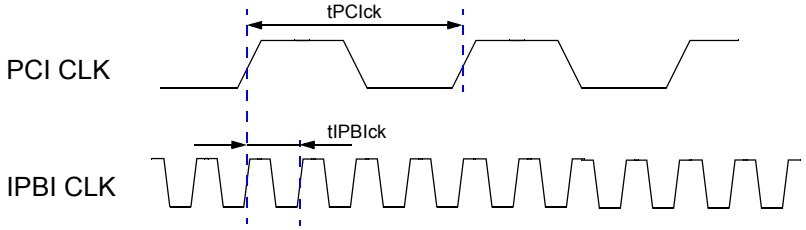


Figure 11. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

3.3.7.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.1
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.2
t_1	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns	1	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns		A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	-	ns	2	A7.5
t_4	OE assertion before CS assertion	-	0.4	ns		A7.6
t_5	OE negation before CS negation	-	0.4	ns		A7.7
t_6	RW valid before CS assertion	t_{PCIck}	-	ns		A7.8
t_7	RW hold after CS negation	t_{IPBIck}	-	ns		A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	-	ns		A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	-	ns		A7.11
t_{10}	DATA input setup before CS negation	2.8	-	ns		A7.12
t_{11}	DATA input hold after CS negation	0	(DC+1)*t_{PCIck}	ns		A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	-	ns	3	A7.14
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	3	A7.15

3.3.7.3 MUXed Mode

Table 26. MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.15
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.16
t_{ALEA}	PCI CLK to ALE assertion	-	1	ns		A7.16
t_1	ALE assertion before Address, Bank, TSIZ assertion	-	0.8	ns		A7.17
t_2	CS assertion before Address, Bank, TSIZ negation	-	0.7	ns		A7.18
t_3	CS assertion before Data wr valid	-	0.7	ns		A7.19
t_4	Data wr hold after CS negation	t_{IPBIck}	-	ns		A7.20
t_5	Data rd setup before CS negation	2.8	-	ns		A7.21
t_6	Data rd hold after CS negation	0	(DC+1)*t_{PCIck}	ns	1	A7.22
t_7	ALE pulse width	-	t_{PCIck}	ns		A7.23
t_{TSA}	CS assertion after TS assertion	-	0.8	ns		A7.24
t_8	TS pulse width	-	t_{PCIck}	ns		A7.24
t_9	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns		A7.25
t_{OEA}	OE assertion before CS assertion	-	0.4	ns		A7.26
t_{OEN}	OE negation before CS negation	-	0.4	ns		A7.27
t_{10}	RW assertion before ALE assertion	t_{IPBIck}	-	ns		A7.26
t_{11}	RW negation after CS negation	-	t_{PCIck}	ns		A7.27
t_{12}	ACK assertion after CS assertion	t_{IPBIck}	-	ns	2	A7.28
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	2	A7.28

Note:
1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified 0 - 65535.
2. ACK is input and can be used to shorten the CS pulse width.

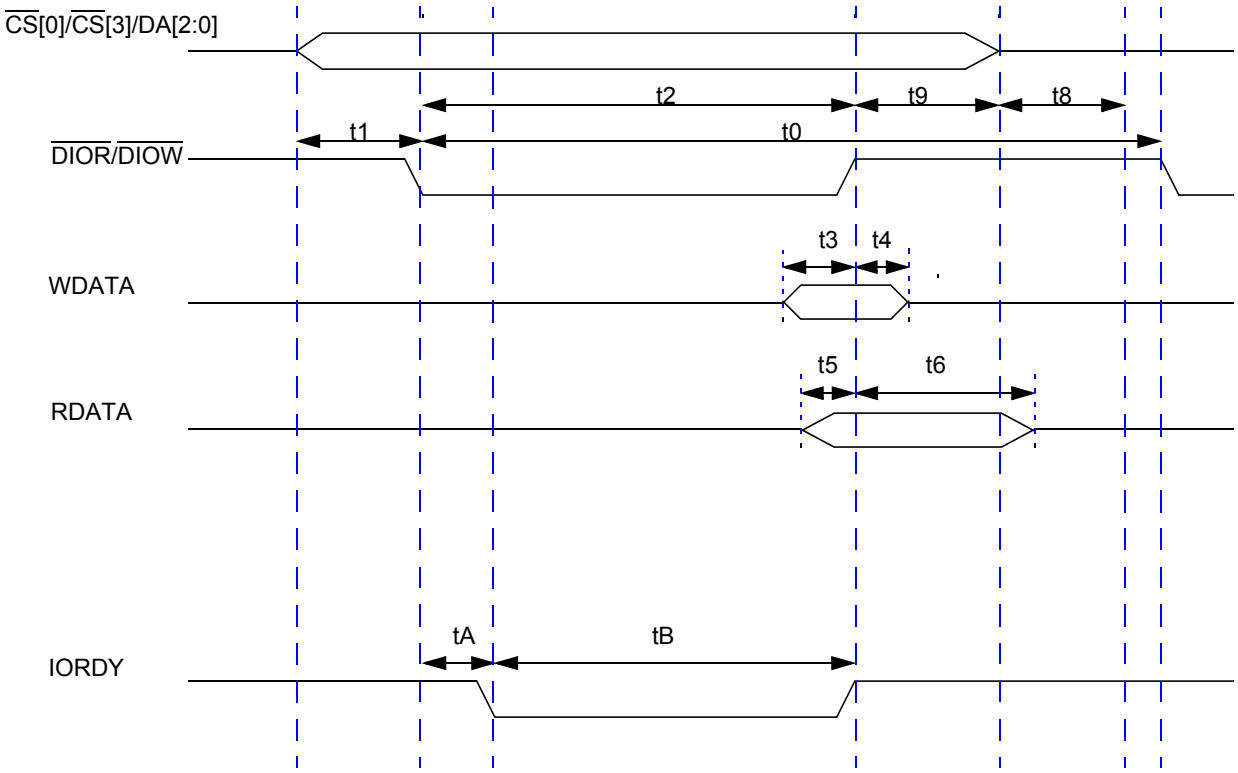


Figure 15. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

	Multiword DMA Timing Parameters	Min/Max	Mode 0(ns)	Mode 1(ns)	Mode 2(ns)	SpecID
t0	Cycle Time	min	480	150	120	A8.12
tC	$\overline{\text{DMACK}}$ to DMARQ delay	max	—	—	—	A8.13
tD	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width (16-bit)	min	215	80	70	A8.14
tE	$\overline{\text{DIOR}}$ data access	max	150	60	50	A8.15
tG	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ data setup	min	100	30	20	A8.16
tF	$\overline{\text{DIOR}}$ data hold	min	5	5	5	A8.17
tH	$\overline{\text{DIOW}}$ data hold	min	20	15	10	A8.18
tI	DMACK to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	0	0	0	A8.19
tJ	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to $\overline{\text{DMACK}}$ hold	min	20	5	5	A8.20
tKr	$\overline{\text{DIOR}}$ negated pulse width	min	50	50	25	A8.21
tKw	$\overline{\text{DIOW}}$ negated pulse width	min	215	50	25	A8.22
tLr	$\overline{\text{DIOR}}$ to DMARQ delay	max	120	40	35	A8.23
tLw	$\overline{\text{DIOW}}$ to DMARQ delay	max	40	40	35	A8.24

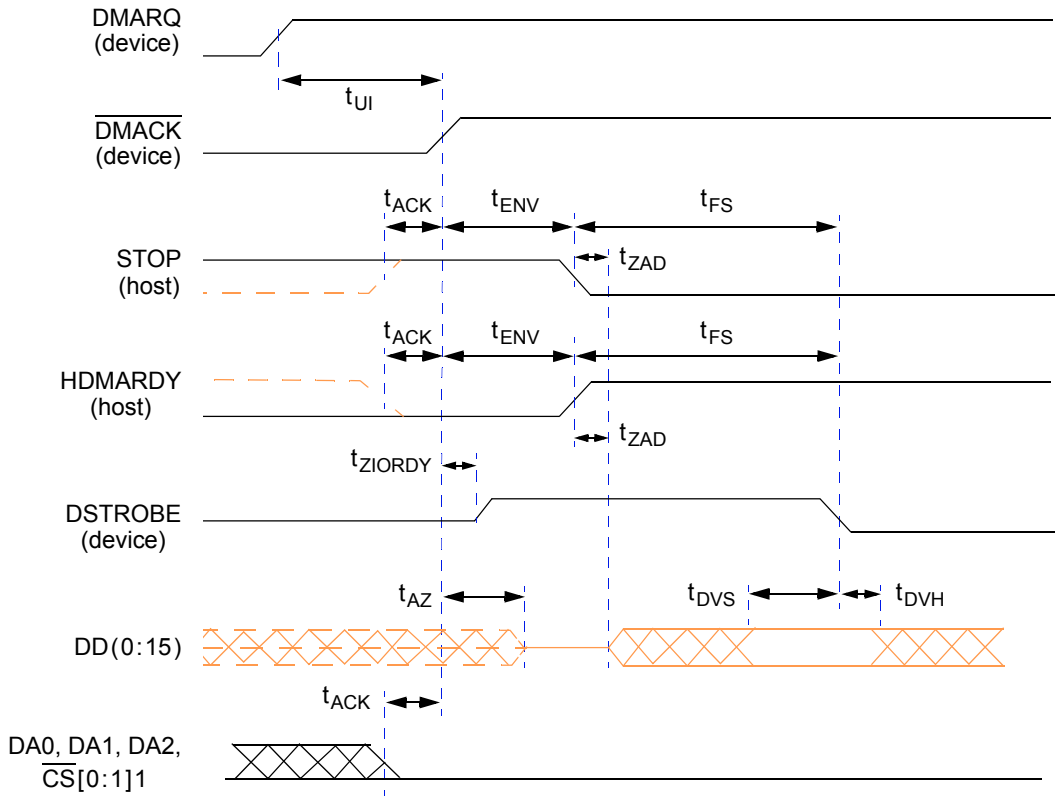


Figure 17. Timing Diagram—Initiating an Ultra DMA Data In Burst

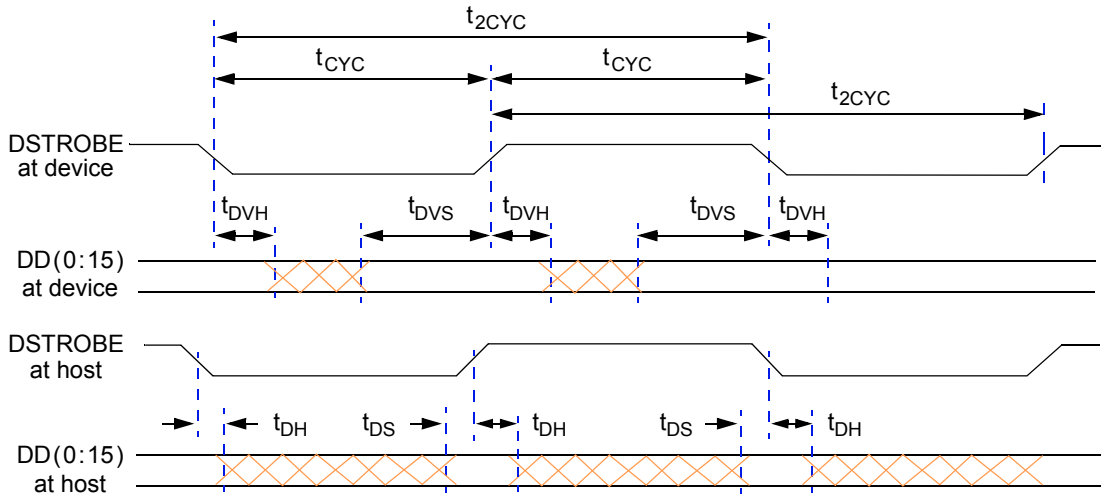


Figure 18. Timing Diagram—Sustained Ultra DMA Data In Burst

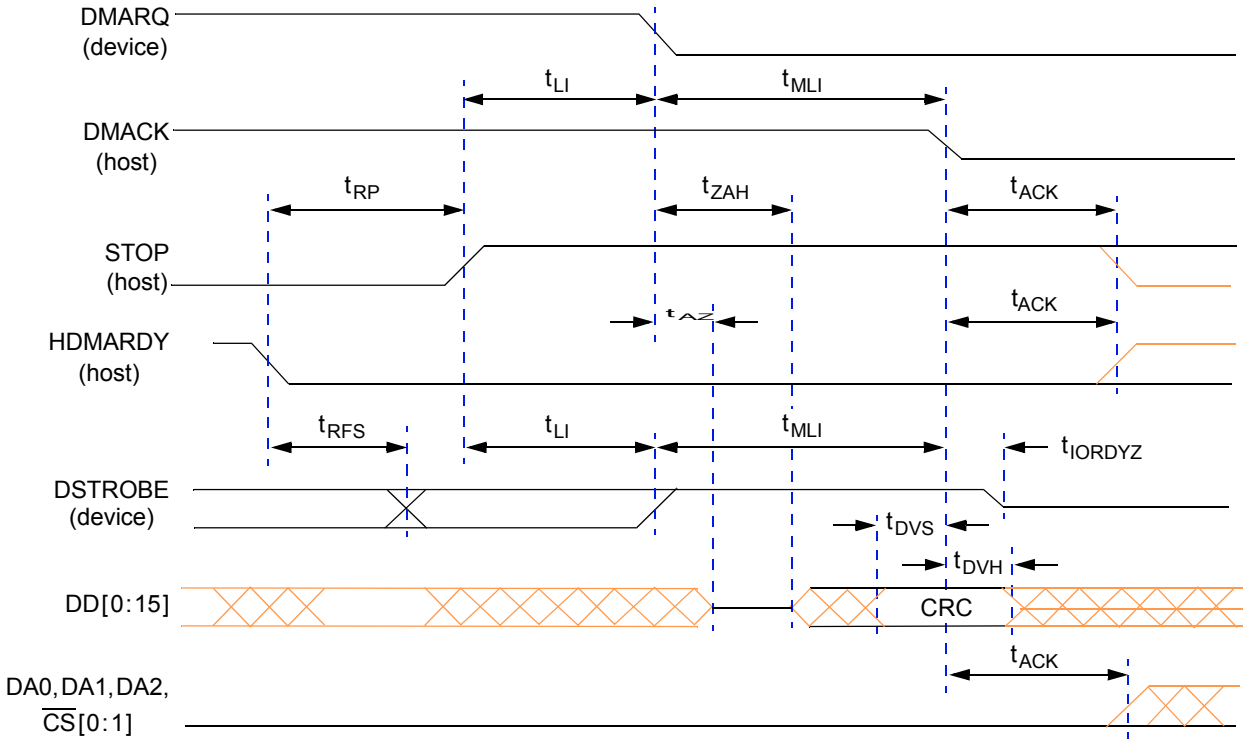


Figure 21. Timing Diagram—Host Terminating Ultra DMA Data In Burst

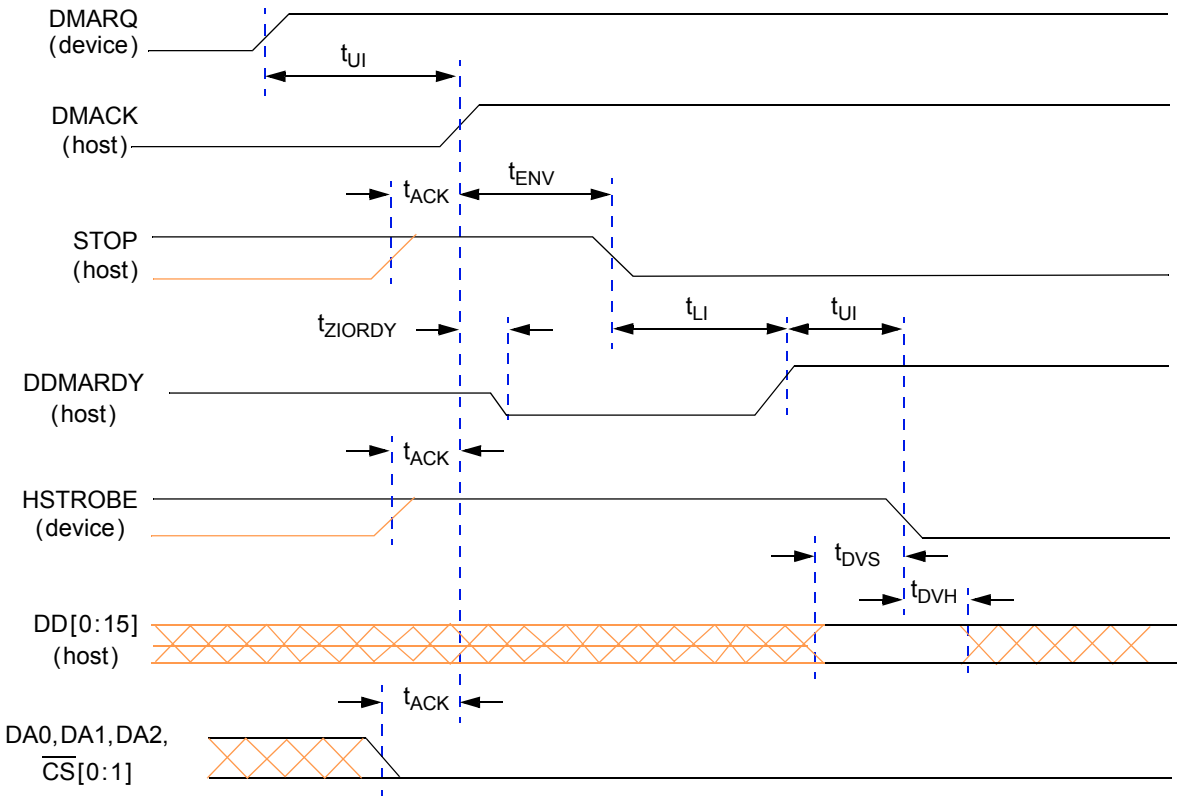


Figure 22. Timing Diagram—Initiating an Ultra DMA Data Out Burst

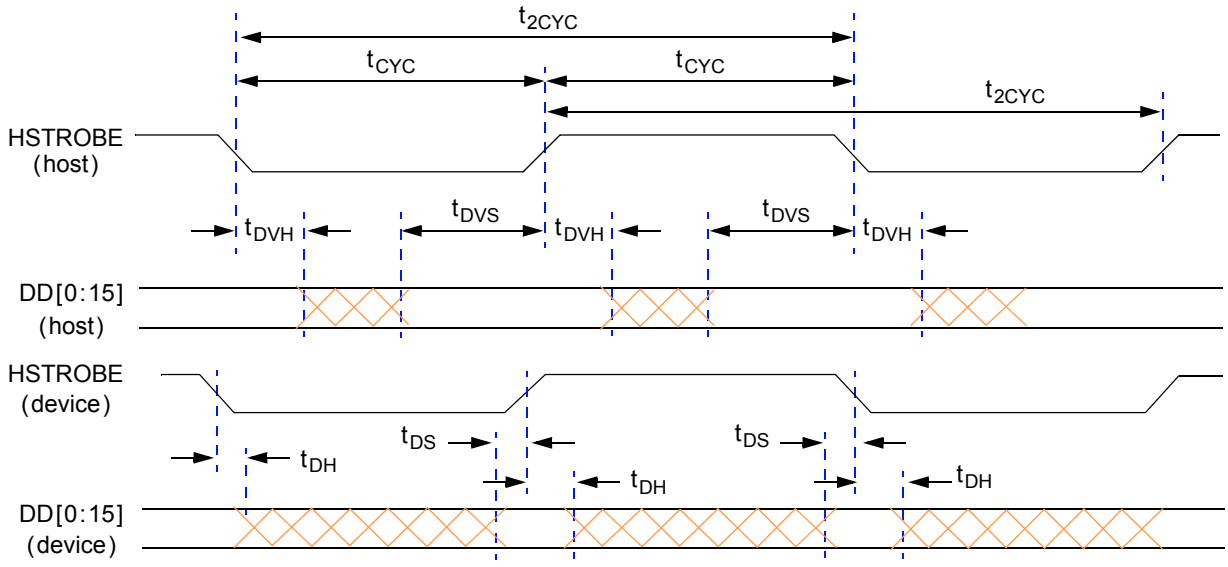


Figure 23. Timing Diagram—Sustained Ultra DMA Data Out Burst

NOTE

Output timing was specified at a nominal 50 pF load.

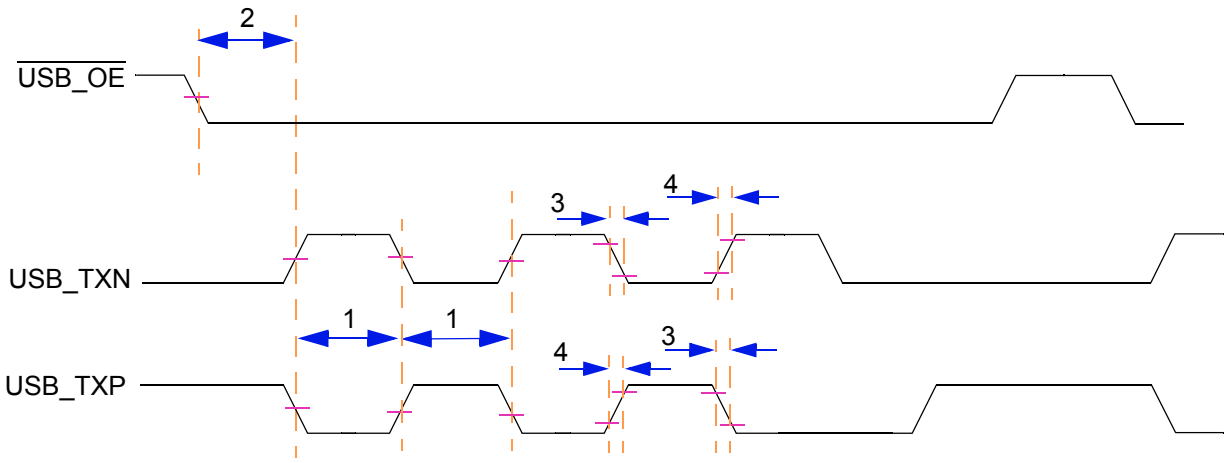


Figure 32. Timing Diagram—USB Output Line

3.3.11 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.1
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.2
3	Slave select clock delay	15.0	—	ns	A11.3
4	Output Data valid after Slave Select ($\overline{SS}$)	—	20.0	ns	A11.4
5	Output Data valid after SCK	—	20.0	ns	A11.5
6	Input Data setup time	20.0	—	ns	A11.6
7	Input Data hold time	20.0	—	ns	A11.7
8	Slave disable lag time	15.0	—	ns	A11.8
9	Sequential transfer delay	1	—	IP-Bus Cycle[1]	A11.9
10	Clock falling time	—	7.9	ns	A11.10
11	Clock rising time	—	7.9	ns	A11.11

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

NOTE

Output timing was specified at a nominal 50 pF load.

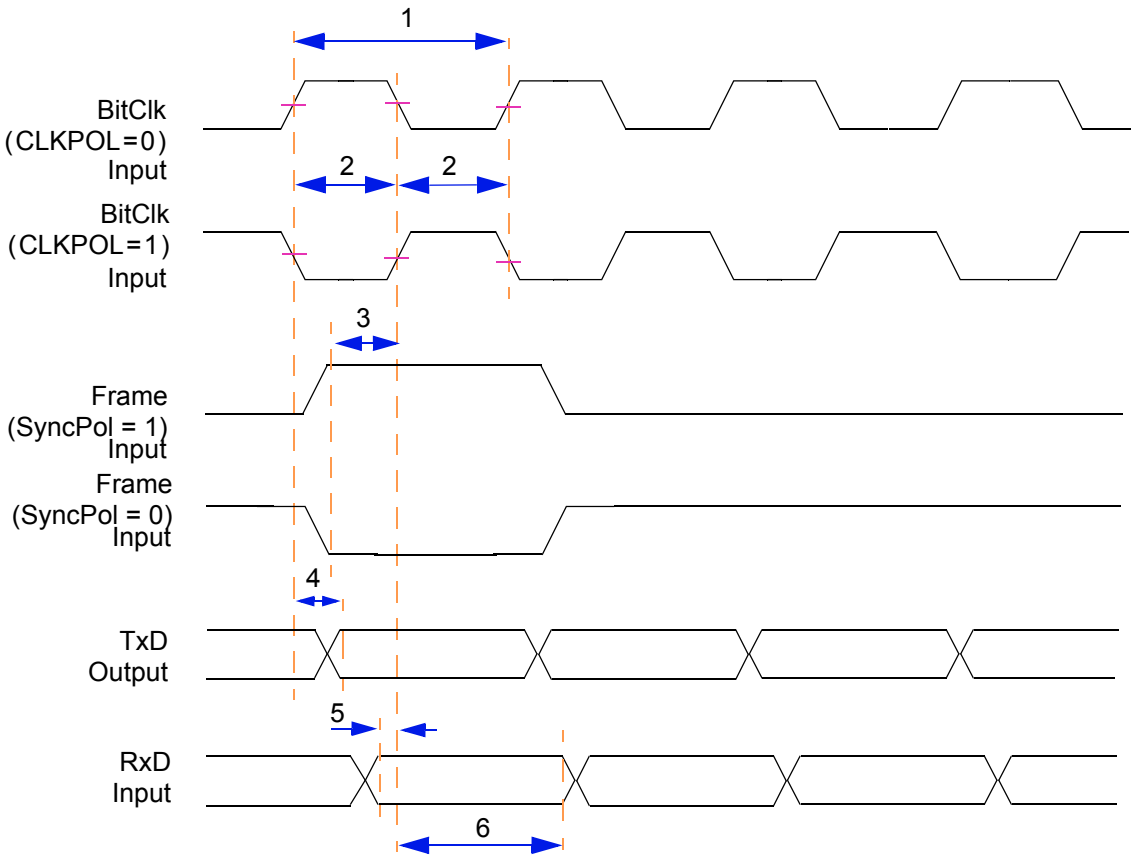


Figure 39. Timing Diagram — 8,16, 24, and 32-bit CODEC / I²S Slave Mode

3.3.15.2 AC97 Mode

Table 44. Timing Specifications — AC97 Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A15.15
2	Clock pulse high time	—	40.7	—	ns	A15.16
3	Clock pulse low time	—	40.7	—	ns	A15.17
4	Frame valid after rising clock edge	—	—	13.0	ns	A15.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A15.19
6	Input Data setup time	1.0	—	—	ns	A15.20
7	Input Data hold time	1.0	—	—	ns	A15.21

NOTE

Output timing was specified at a nominal 50 pF load.

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.56
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.57
3	Slave select clock delay	0.0	—	ns	A15.58
4	Output data valid	—	14.0	ns	A15.59
5	Input Data setup time	2.0	—	ns	A15.60
6	Input Data hold time	1.0	—	ns	A15.61
7	Slave disable lag time	0.0	—	ns	A15.62
8	Minimum Sequential Transfer delay = 2 * IP-Bus clock cycle time	30.0	—	ns	A15.63

NOTE

Output timing was specified at a nominal 50 pF load.

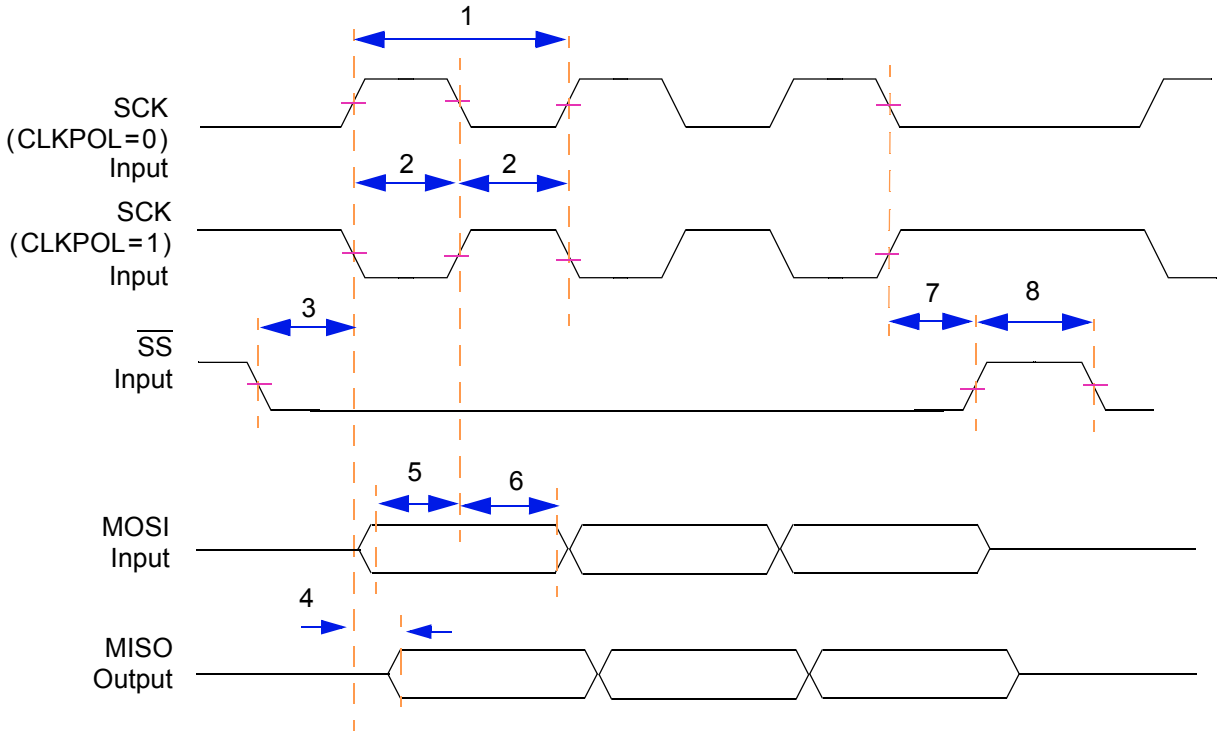


Figure 45. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

3.3.16 GPIOs and Timers

3.3.16.1 General and Asynchronous Signals

The MPC5200 contains several sets if I/Os that do not require special setup, hold, or valid requirements. Most of these are asynchronous to the system clock. The following numbers are provided for test and validation purposes only, and they assume a 133 MHz internal bus frequency.

Figure 46 shows the GPIO Timing Diagram. Table 50 gives the timing specifications.

Table 50. Asynchronous Signals

Sym	Description	Min	Max	Units	SpecID
t_{CK}	Clock Period	7.52	—	ns	A16.1
t_{IS}	Input Setup for Async Signal	12	—	ns	A16.2
t_{IH}	Input Hold for Async Signals	1	—	ns	A16.3
t_{DV}	Output Valid	—	15.33	ns	A16.4
t_{DH}	Output Hold	1	—	ns	A16.5

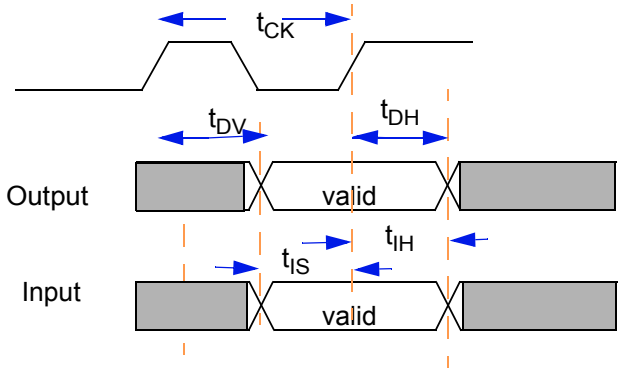


Figure 46. Timing Diagram—Asynchronous Signals

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, TX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_2	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	TTL	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Table 52. MPC5200 Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
Power and Ground						
VDD_IO		-				
VDD_MEM_IO		-				
VDD_CORE		-				
VSS_IO/CORE		-				
SYS_PLL_AVDD		-				
CORE_PLL_AVDD		-				

NOTES:
1 All “open drain” outputs of the MPC5200 are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200 I/O power rail if the external signal is driven above the MPC5200 I/O power rail voltage.

5 System Design Information

5.1 Power UP/Down Sequencing

Figure 52 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).

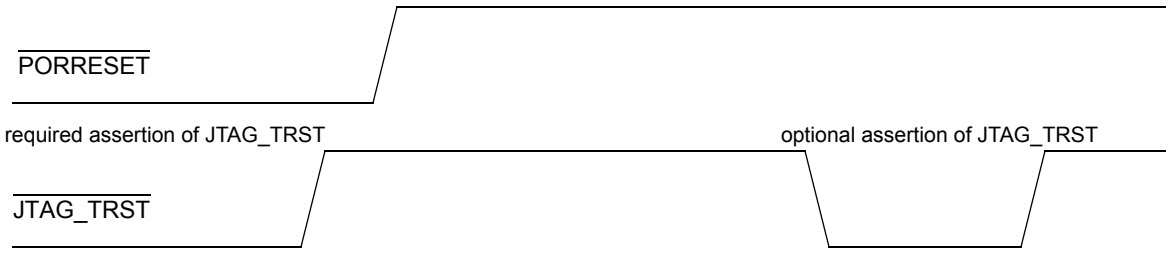


Figure 54. PORRESET vs. JTAG_TRST

5.4.1.2 Connecting JTAG_TRST

The wiring of the JTAG_TRST depends on the existence of a board-related debug interface (see Table 53 below).

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200.

5.4.2 G2_LE COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.4.2.1 Boards interfacing the JTAG port via a COP connector

The MPC5200 functional pin interface and internal logic provides access to the embedded G2_LE processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200 I/O Pin	BDM Connector	Internal PullUp/Down	External PullUp/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset		10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset		10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O

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