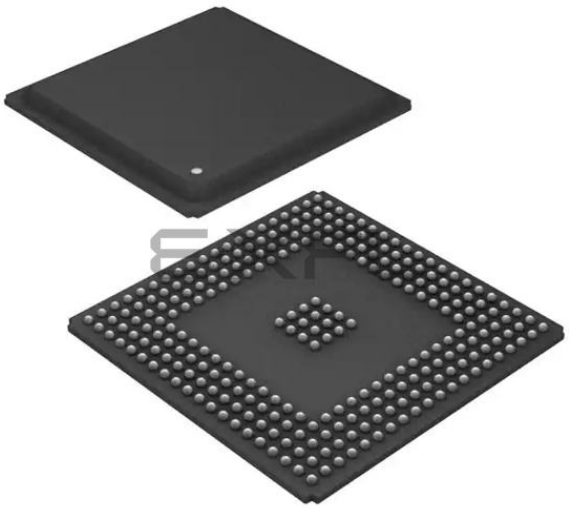

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cvr400r2

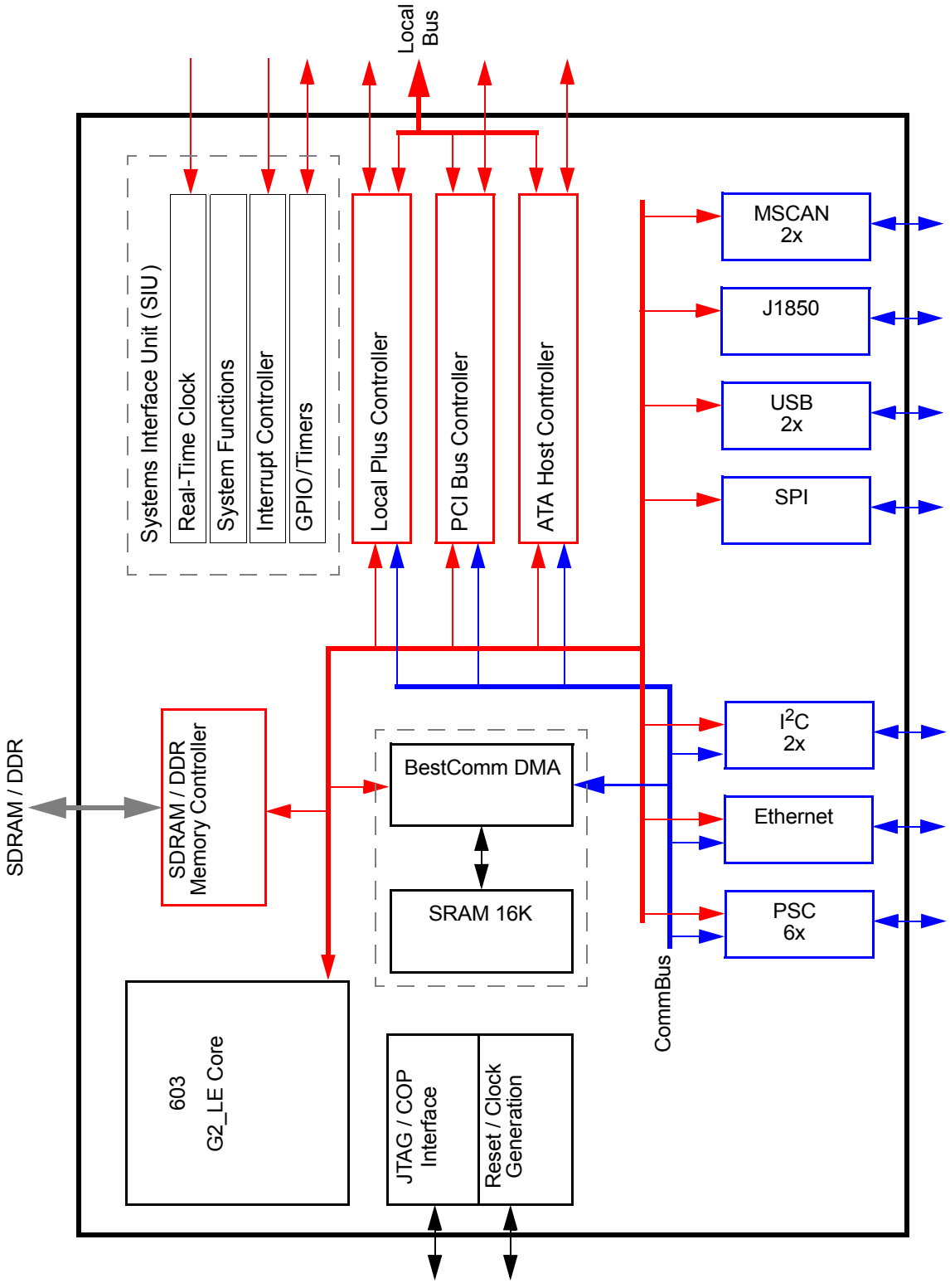


Figure 1. Simplified Block Diagram—MPC5200

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200 processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{\text{analog}} + P_{IO}$$

Table 6. Power Dissipation

Core Power Supply (VDD_CORE)					
Mode	SYS_XTAL/XLB/PCI/IPG/CORE (MHz)		Unit	Notes	SpecID
	33/66/33/33/264	33/132/66/132/396			
	Typ	Typ			
Operational	727.5	1080	mW	[1],[2]	D5.1
Doze	—	600	mW	[1],[3]	D5.2
Nap	—	225	mW	[1],[4]	D5.3
Sleep	—	225	mW	[1],[5]	D5.4
Deep-Sleep	52.5	52.5	mW	[1],[6]	D5.5
PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)					
Mode	**Typ**		**Unit**	**Notes**	
Typical	2		mW	[7]	D5.6
Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8])					
Mode	**Typ**		**Unit**	**Notes**	
Typical	33		mW	[9]	D5.7

NOTES:
1. Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 C
2. Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.
3. Doze power is measured with the G2_LE core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive
4. Nap power is measured with the G2_LE core in Nap mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
5. Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive
6. Deep-Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL, Core PLL and all other system modules are inactive
7. Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 C
8. IO power figures given in the table represent the worst case scenario. For the mem_io rail connected to 2.5V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3V.
9. Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD\_MEM\_IO_{SDR}$= 3.3 V, Tj = 25 C

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The G2_LE core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The G2_LE core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

3.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	100	µs	O1.2

3.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Symbol	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	1	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	T_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	2	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	3	—	—	100	µs	O3.5

NOTES:
1. The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2. This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.
3. Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.[1]	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).[2]	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

NOTES:
1 **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0-6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the MPC5200 User Manual [1].
2 SYS_XTAL_IN duty cycle is measured at V_M.

3.3.3 Resets

The MPC5200 has three reset pins:

- $\overline{\text{PORRESET}}$ - Power on Reset
- $\overline{\text{HRESET}}$ - Hard Reset
- $\overline{\text{SRESET}}$ - Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200 inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

Table 14. Reset Pulse Width

Name	Description	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
$\overline{\text{PORRESET}}$	Power On Reset	$t_{VDD\_stable}+t_{up\_osc}+t_{lock}$	—	SYS_XTAL_IN	A3.1
$\overline{\text{HRESET}}$	Hardware Reset	4 clock cycles	—	SYS_XTAL_IN	A3.2
$\overline{\text{SRESET}}$	Software Reset	4 clock cycles	—	SYS_XTAL_IN	A3.3

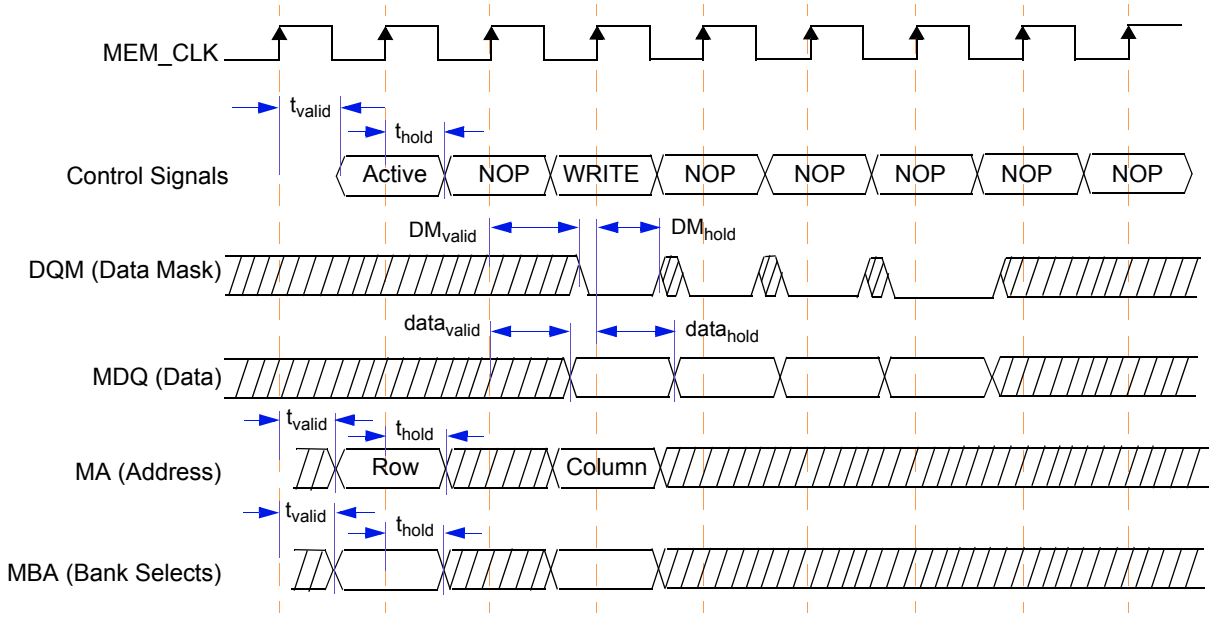
Notes:
1. For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.
2. The t_{VDD_stable} describes the time which is needed to get all power supplies stable.
3. For t_{lock}, refer to the Oscillator/PLL section of this specification for further details.
4. For t_{up_osc}, refer to the Oscillator/PLL section of this specification for further details.
5. Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.
6. The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 19. Standard SDRAM Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.8
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.9
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.10
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.25+0.4	ns	A5.11
DM_{hold}	DQM hold after rising edge of Mem_clk	t_{mem_clk}*0.25-0.7	—	ns	A5.12
$data_{valid}$	MDQ valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.75+0.4	ns	A5.13
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	t_{mem_clk}*0.75-0.7	—	ns	A5.14



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 6. Timing Diagram—Standard SDRAM Memory Write Timing

3.3.5.3 Memory Interface Timing-DDR SDRAM Read Command

The SDRAM Memory Controller uses an internally skewed clock for reading DDR memory. The programmable bits in the Reset Configuration Register used to account for unknown board delays are in the CDM module. The internal read clock can be delayed up to 3 ns under worst operating conditions in 32 increments of 95 ps, (1.4 ns in 45 ps increments under best case operating conditions) by programming the CDM Reset Configuration Register tap delay bits. Note: These bits in the CDM Reset Configuration register are not ‘reset configured’ but have a hard coded reset value **and** are writable during operation.

Table 20. DDR SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.15
t_{valid}	Control Signals, Address and MBA valid after rising edge of MEM_CLK	—	t_{mem_clk}*0.5+0.4	ns	A5.16
t_{hold}	Control Signals, Address and MBA hold after rising edge of MEM_CLK	t_{mem_clk}*0.5	—	ns	A5.17
$t_{data\_sample\_max}$	Read Data sample window	—	4.59[1]	ns	A5.18
$t_{data\_sample\_min}$	Read Data sample window	1.55[2]	—	ns	A5.19

NOTES:
1 Calculated with maximum number of Tap delay, 31 Tap delay are selected.
2 Calculated with minimum number of Tap delay, 0 Tap delay are selected.

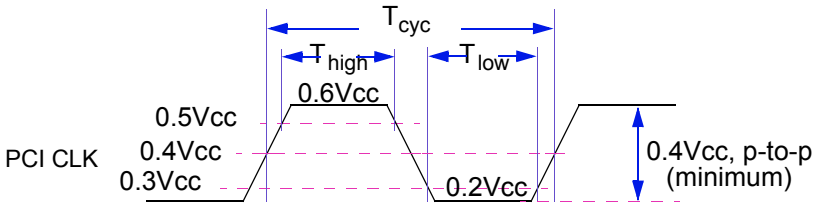


Figure 10. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
T_{cyc}	PCI CLK Cycle Time	15	30	30		ns	1,3	A6.1
T_{high}	PCI CLK High Time	6		11		ns		A6.2
t_{low}	PCI CLK Low Time	6						A6.3
-	PCI CLK Slew Rate	1.5	4	1	4	V/ns	2	A6.4

NOTES:
1. In general, all 66-MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 10.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

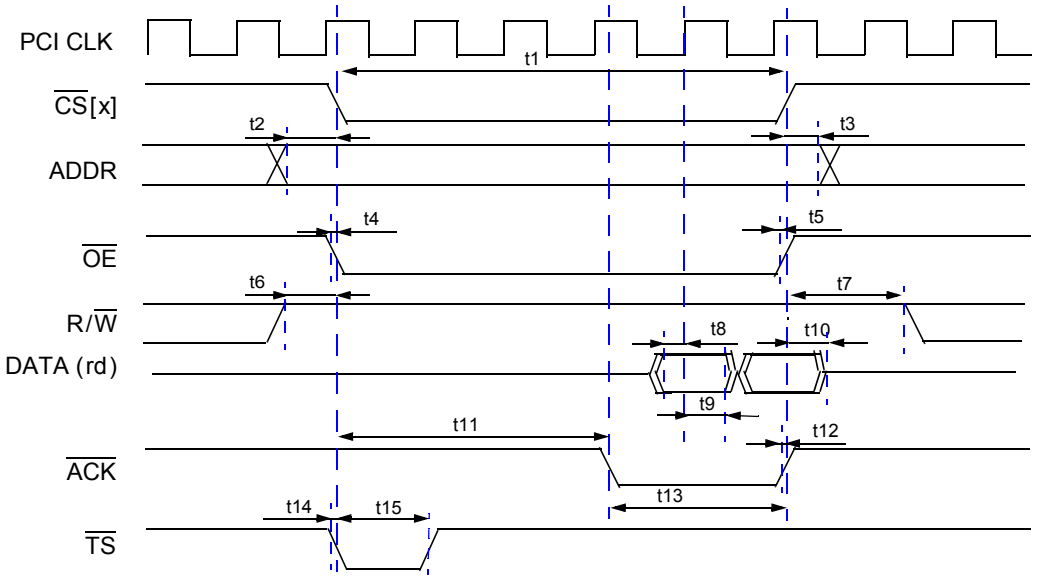


Figure 13. Timing Diagram—Burst Mode

3.3.7.3 MUXed Mode

Table 26. MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	-	1.8	ns		A7.15
t_{CSN}	PCI CLK to CS negation	-	1.8	ns		A7.16
t_{ALEA}	PCI CLK to ALE assertion	-	1	ns		A7.16
t_1	ALE assertion before Address, Bank, TSIZ assertion	-	0.8	ns		A7.17
t_2	CS assertion before Address, Bank, TSIZ negation	-	0.7	ns		A7.18
t_3	CS assertion before Data wr valid	-	0.7	ns		A7.19
t_4	Data wr hold after CS negation	t_{IPBIck}	-	ns		A7.20
t_5	Data rd setup before CS negation	2.8	-	ns		A7.21
t_6	Data rd hold after CS negation	0	(DC+1)*t_{PCIck}	ns	1	A7.22
t_7	ALE pulse width	-	t_{PCIck}	ns		A7.23
t_{TSA}	CS assertion after TS assertion	-	0.8	ns		A7.24
t_8	TS pulse width	-	t_{PCIck}	ns		A7.24
t_9	CS pulse width	(2+WS)*t_{PCIck}	(2+WS)*t_{PCIck}	ns		A7.25
t_{OEA}	OE assertion before CS assertion	-	0.4	ns		A7.26
t_{OEN}	OE negation before CS negation	-	0.4	ns		A7.27
t_{10}	RW assertion before ALE assertion	t_{IPBIck}	-	ns		A7.26
t_{11}	RW negation after CS negation	-	t_{PCIck}	ns		A7.27
t_{12}	ACK assertion after CS assertion	t_{IPBIck}	-	ns	2	A7.28
t_{13}	ACK negation after CS negation	-	t_{PCIck}	ns	2	A7.28

Note:
1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified 0 - 65535.
2. ACK is input and can be used to shorten the CS pulse width.

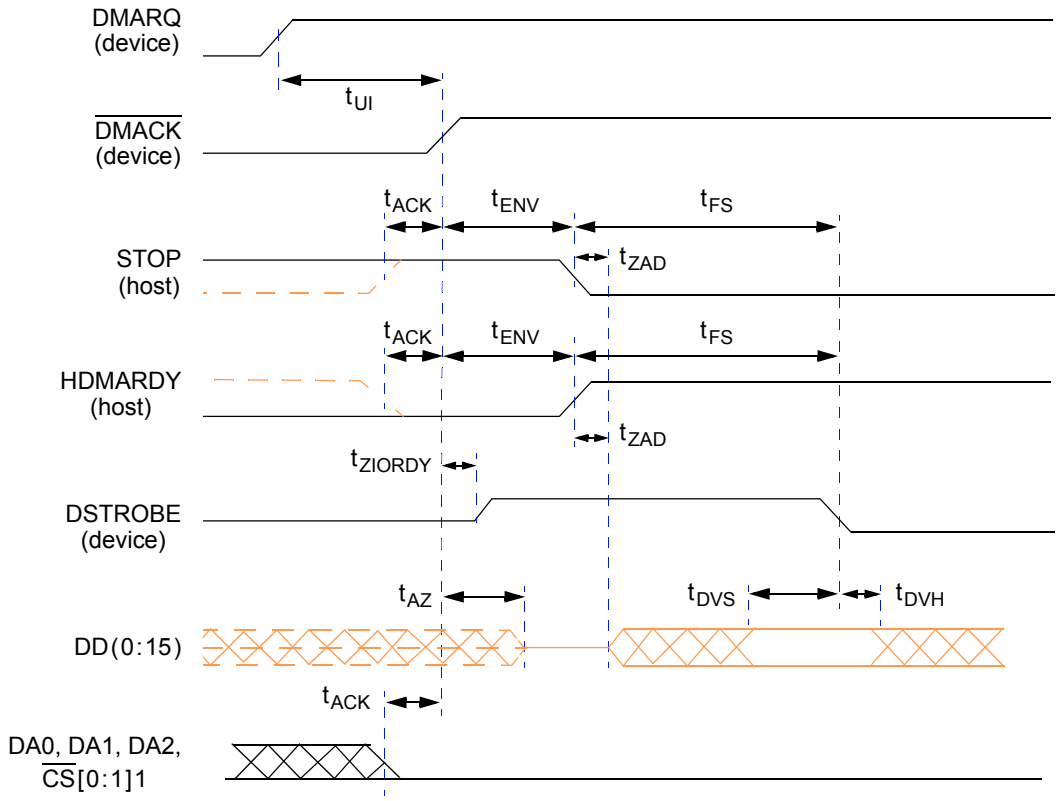


Figure 17. Timing Diagram—Initiating an Ultra DMA Data In Burst

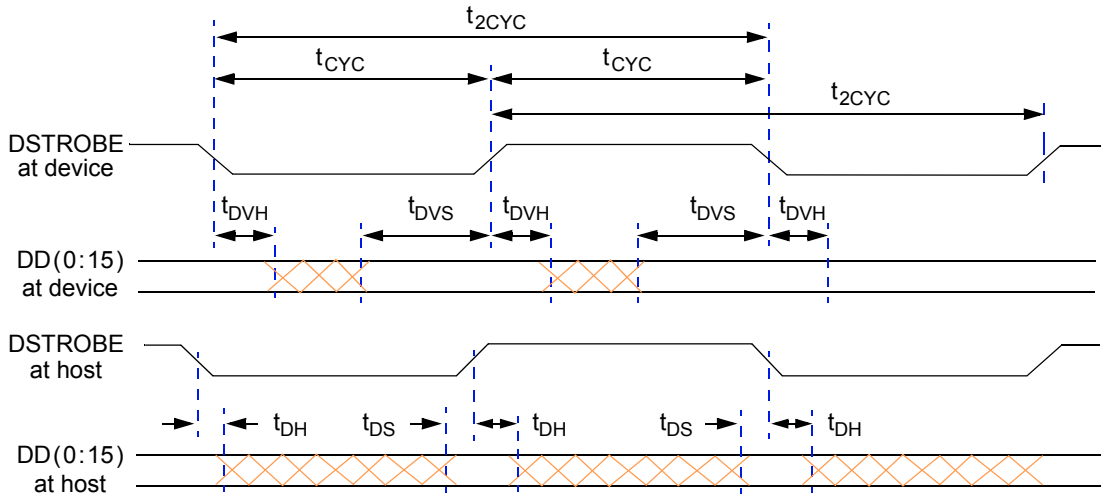


Figure 18. Timing Diagram—Sustained Ultra DMA Data In Burst

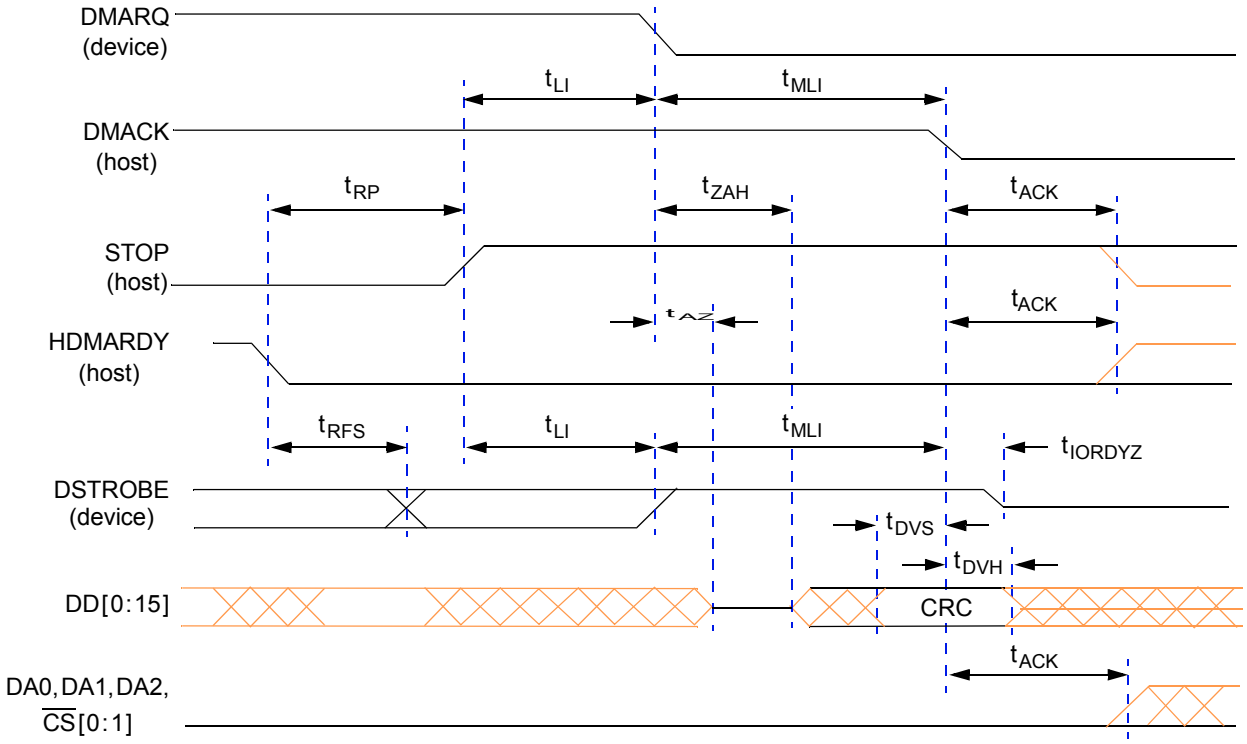


Figure 21. Timing Diagram—Host Terminating Ultra DMA Data In Burst

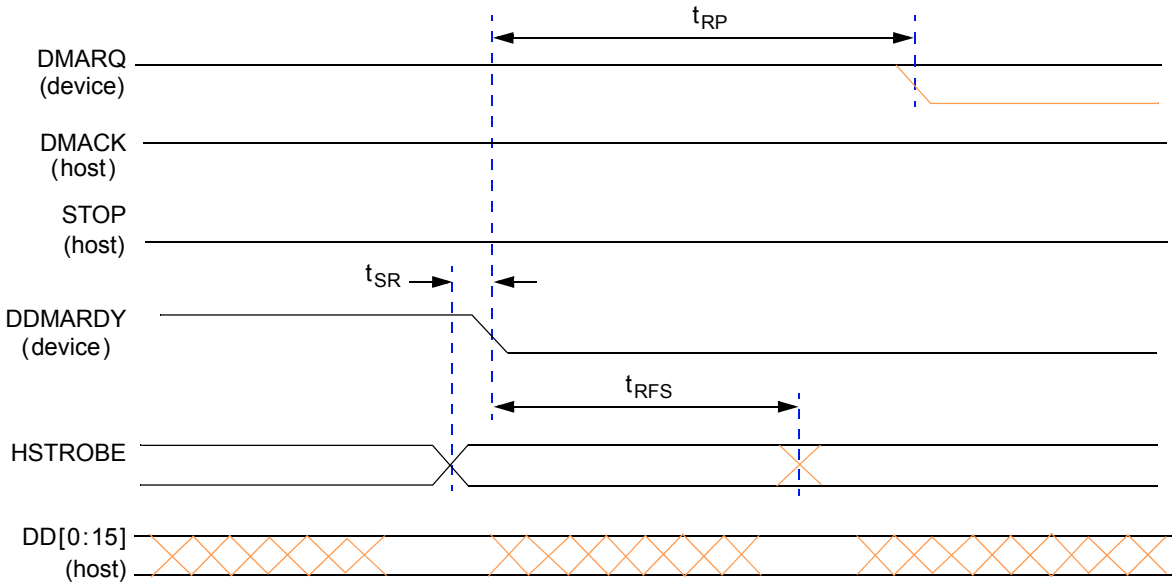


Figure 24. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

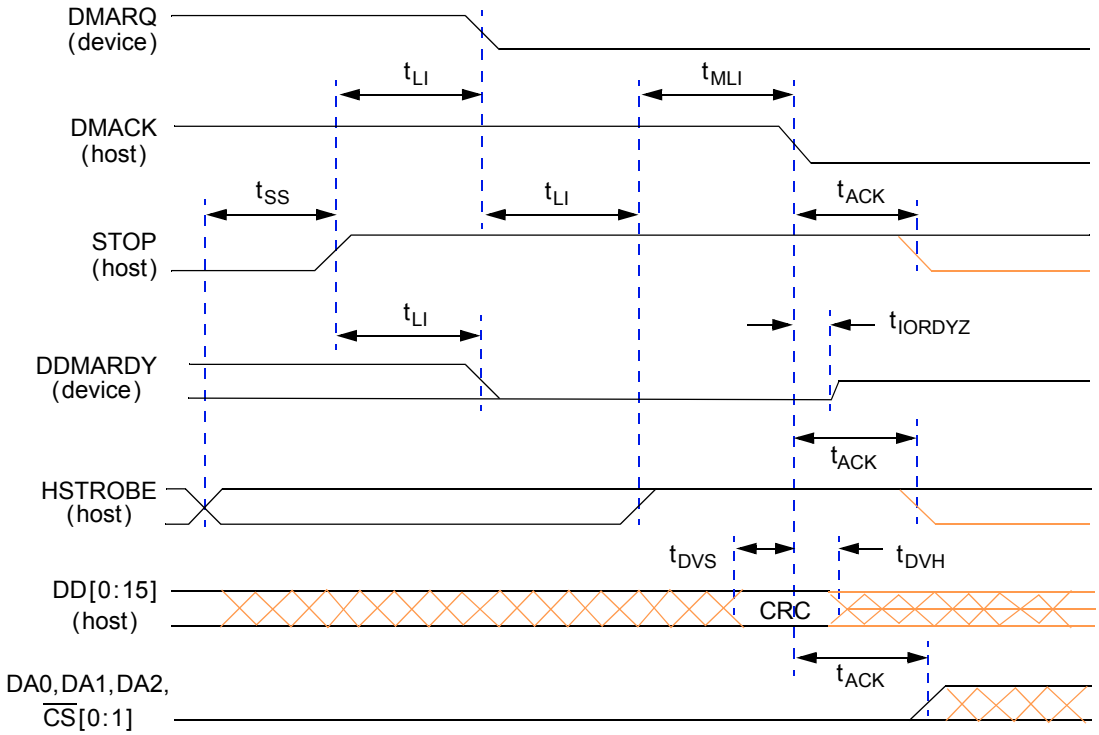


Figure 25. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

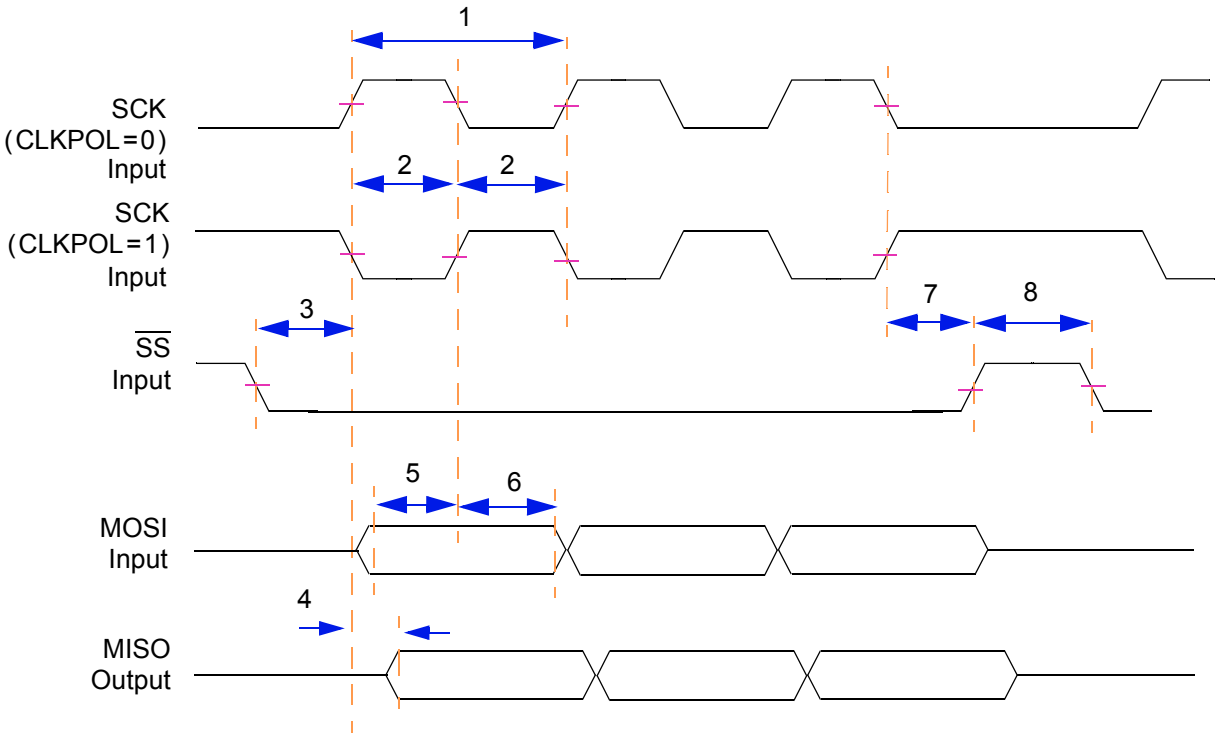


Figure 36. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

3.3.12 MSCAN

The CAN functions are available as RX and TX pins at normal IO pads (I^2C1+GPTimer or PSC2). There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.13 I^2C

Table 40. I^2C Input Timing Specifications—SCL and SDA

Sym	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A13.1
2	Clock low period	8	—	IP-Bus Cycle[1]	A13.2
4	Data hold time	0.0	—	ns	A13.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A13.4
7	Data setup time	0.0	—	ns	A13.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A13.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A13.7

NOTES:
1 Inter Peripheral Clock is defined in the MPC5200 User Manual [1].

3.3.15.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK cycle time	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing was specified at a nominal 50 pF load.

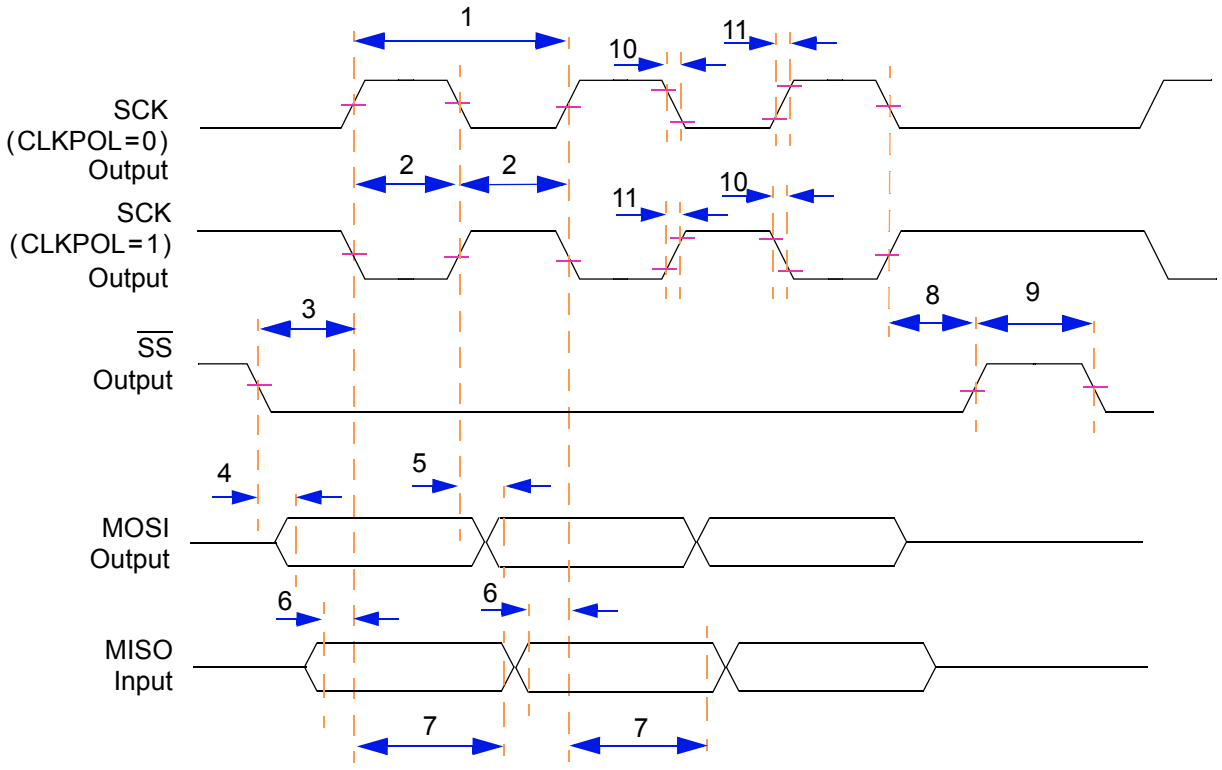


Figure 42. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

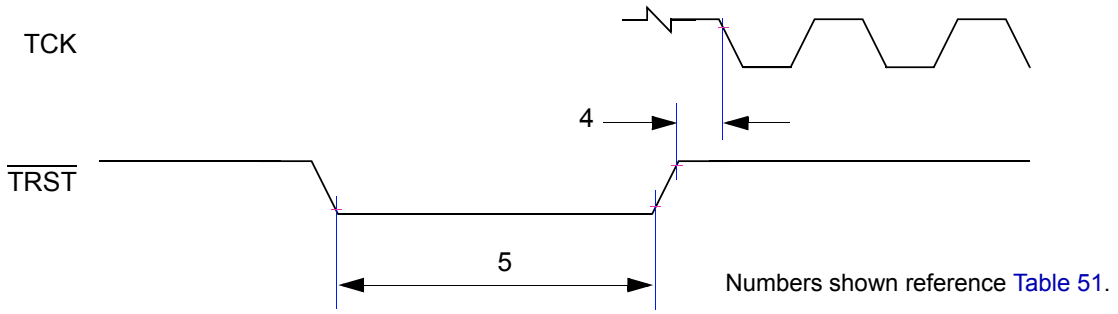


Figure 48. Timing Diagram—JTAG TRST

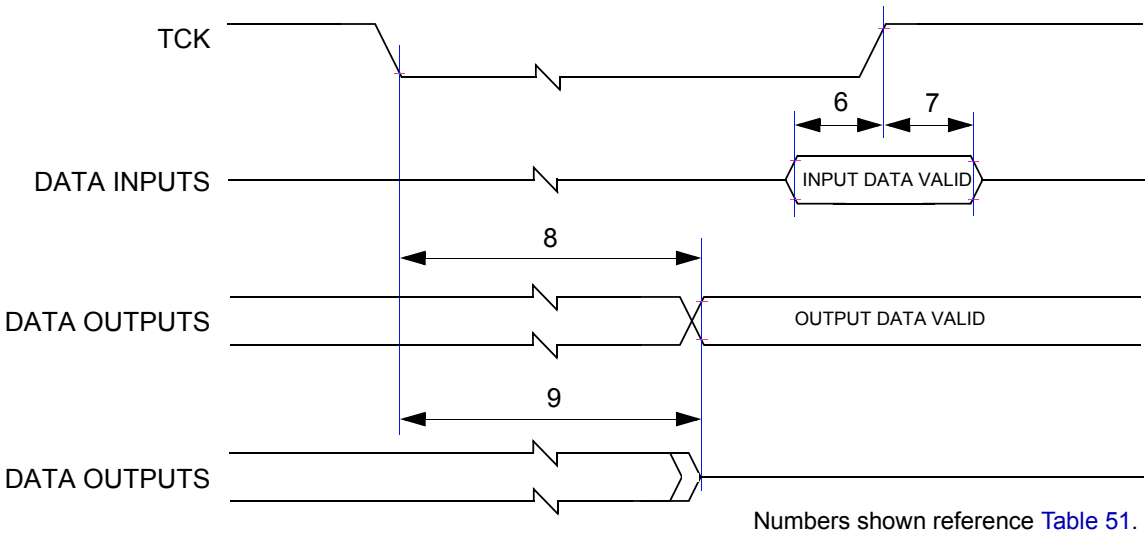


Figure 49. Timing Diagram—JTAG Boundary Scan

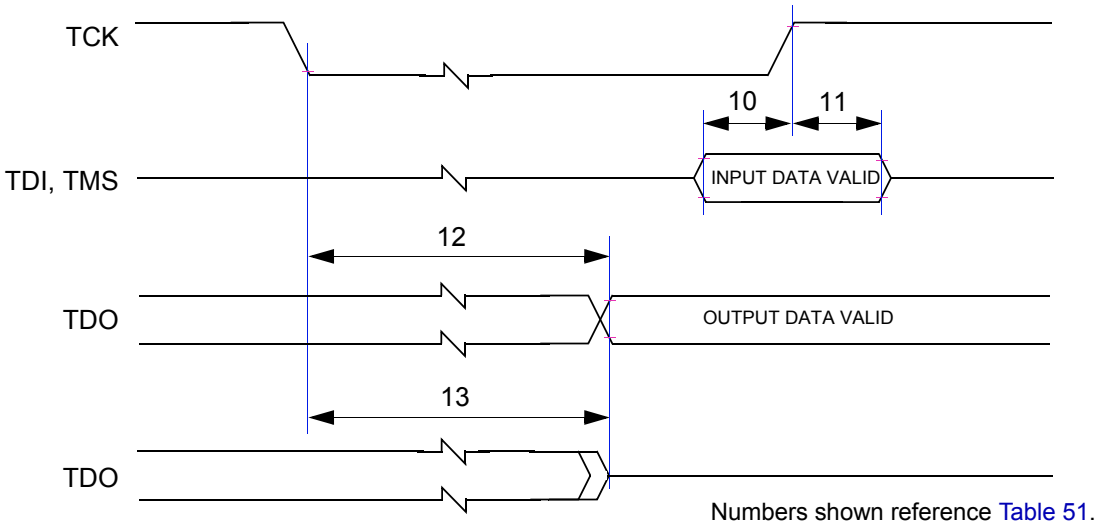


Figure 50. Timing Diagram—Test Access Port

5.3.2 Pull-up Requirements for the PCI Control Lines

If the PCI interface is NOT used (and internally disabled) the PCI control pins must be terminated as indicated by the PCI Local Bus specification [4]. This is also required for MOST/Graphics and Large Flash Mode.

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

5.3.3 Pull-up/Pull-down Requirements for MEM_MDQS pins (SDRAM)

The MEM_MDQS[3:0] signals are not used with SDR memories and require pull-up or pull-down resistors in SDRAM mode.

5.4 JTAG

The MPC5200 provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200's imbedded Freescale (formerly Motorola) MPC603e G2_LE processor. This interface provides a means for executing test routines and for performing software development & debug functions.

5.4.1 JTAG_TRST

Boundary scan testing is enabled through the JTAG interface signals. The JTAG_TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

5.4.1.1 JTAG_TRST and PORRESET

The JTAG interface can control the direction of the MPC5200 I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5200 comes out of power-on reset; do this by asserting JTAG_TRST before PORRESET is released.

For more details refer to the Reset and JTAG Timing Specification.

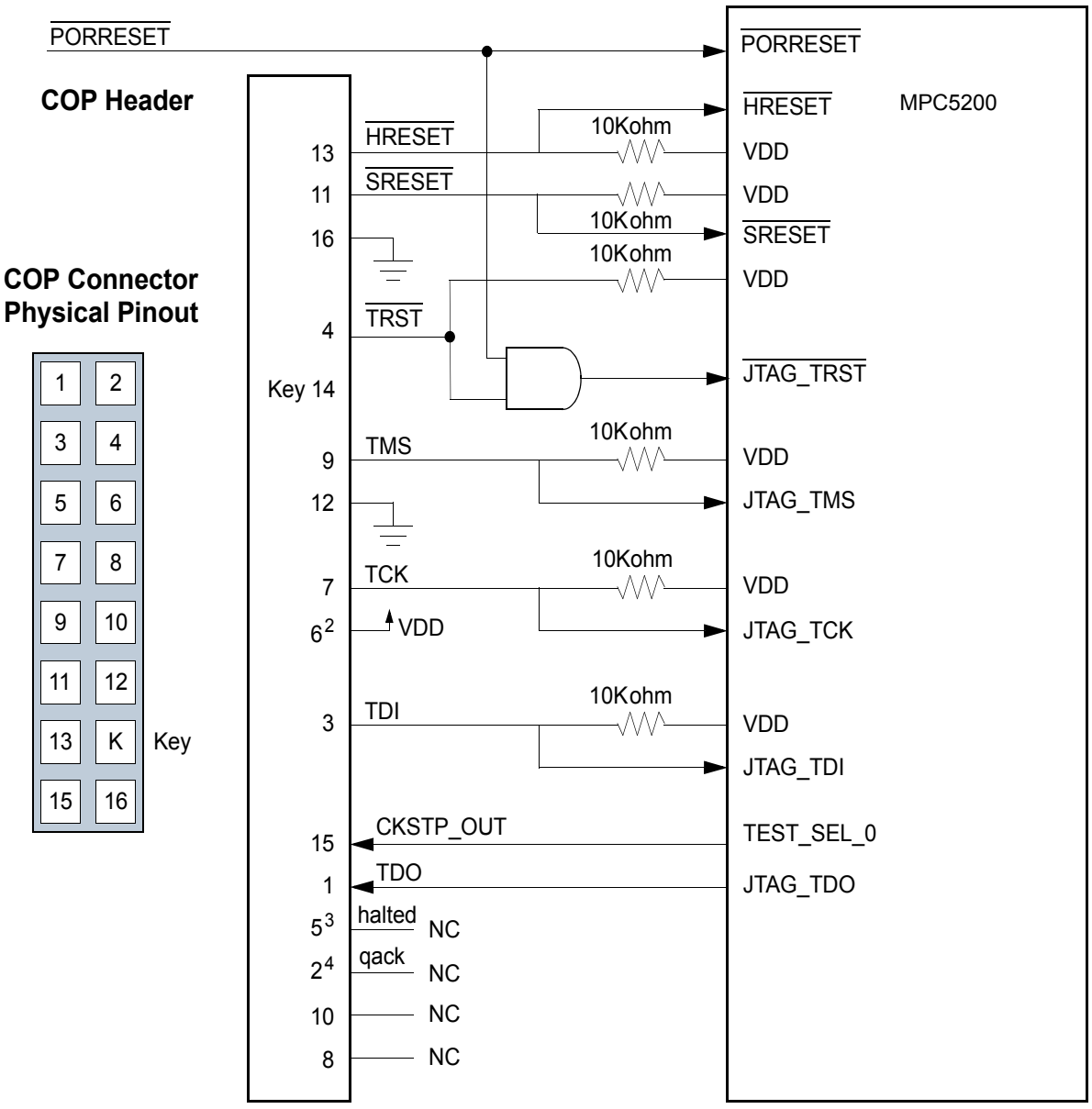


Figure 55. COP Connector Diagram

5.4.2.2 Boards without COP connector

If the JTAG interface is not used, JTAG_TRST should be tied to PORRESET, so that it is asserted when the system reset signal (PORRESET) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 56 shows the connection of the JTAG interface without COP connector.

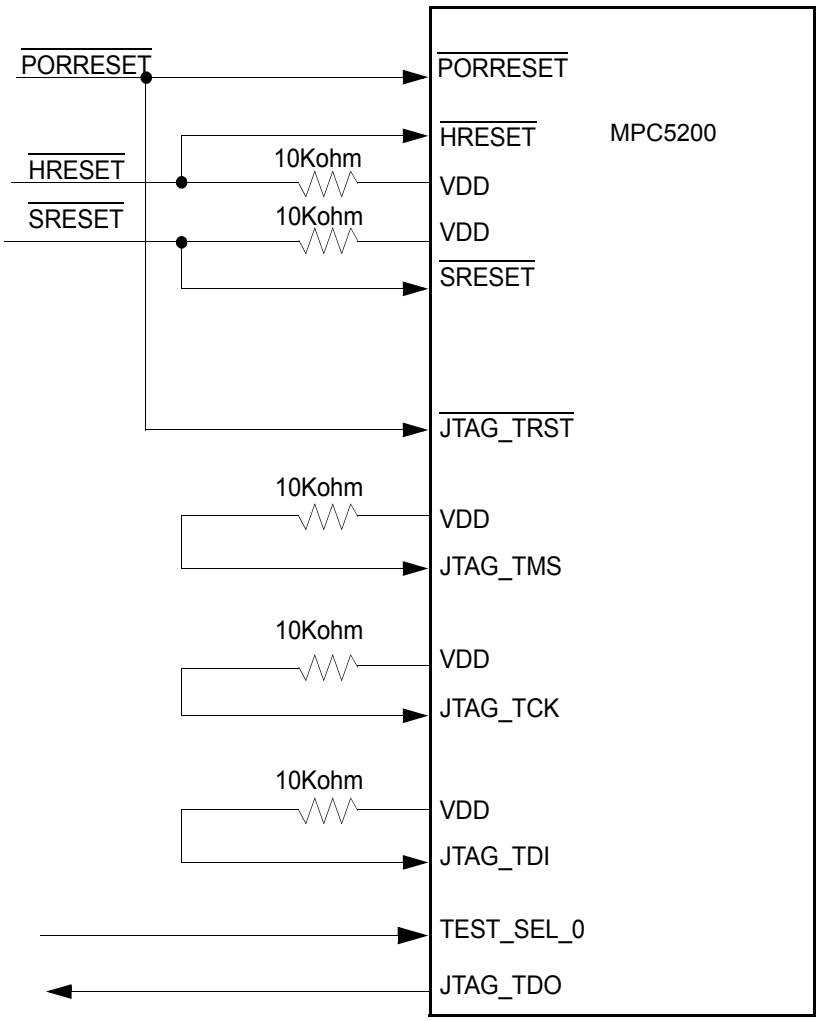


Figure 56. JTAG_TRST wiring for boards without COP connector

6 Ordering Information

Table 54. Ordering Information

Part Number	Speed	Ambient Temp	Qualification
MPC5200BV400	400	0C to 70C	Commercial
MPC5200CBV266	266	-40C to 85C	Industrial
MPC5200CBV400	400	-40C to 85C	Industrial
SPC5200CBV400	400	-40C to 85C	Automotive - AEC

7 Document Revision History

Table 55 provides a revision history for this hardware specification.

Table 55. Document Revision History

Rev. No.	Substantive Change(s)
0.1	First Preliminary release with some TBD's in spec tables (6/2003)
0.2	Added AC specs for missing modules, power-on sequence, misc other updates (7/2003)
0.2.1	Corrected maximum core operating frequency (7/2003)
0.3	Added Memory Interface Timing values, misc other updates (8/2003)
1.0	Added Information about JTAG_TRST (11/2003)
2.0	Added Power Numbers (Section 3.1.5), updated Oscillator and PLL Characteristics (Section 3.2), updated SDRAM AC Characteristics (Section 3.3.5)
3.0	Change to Freescale brand and format (8/2004)
4.0	Updates to LPC timing, DDR SDRAM timing, JTAG section, replaced TBD's (1/2005)
	Rev 4 has been regenerated with the new Freescale appearance guidelines, the title was changed and the reference to www.mobilegt.com in the first paragraph (Note) was changed to www. freescale.com (3/2006).

For more detailed information, refer to the following documentation:

[1] MPC5200 User Manual MPC5200UM

[2] PowerPC Microprocessor Family: The Programming Environments for 32-bit Microprocessors, Rev. 2: MPCFPE32B/AD

[3] G2 Core Reference Manual, Rev. 0: G2CORERM/D

[4] PCI Local Bus Specification, Revision 2.2, December 18, 1998

[5] ANSI ATA-4 Specification

[6] IEEE 802.3 Specification (ETHERNET)

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Rev. 4, 01/2005

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