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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	75
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-1fgg256

RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at $\pm 1\%$ over commercial temperature ranges and $\pm 3\%$ over industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Table 2-9 • Electrical Characteristics of RC Oscillator

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{RC}	Operating Frequency			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V \pm 5%		1		%
		Temperature: -40°C to 125°C Voltage: 3.3 V \pm 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle			50		%
I_{DYNRC}	Operating Current			1		mA

Flash Memory Block Pin Names

Table 2-19 • Flash Memory Block Pin Names

Interface Name	Width	Direction	Description
ADDR[17:0]	18	In	Byte offset into the FB. Byte-based address.
AUXBLOCK	1	In	When asserted, the page addressed is used to access the auxiliary block within that page.
BUSY	1	Out	When asserted, indicates that the FB is performing an operation.
CLK	1	In	User interface clock. All operations and status are synchronous to the rising edge of this clock.
DATAWIDTH[1:0]	2	In	Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0]
DISCARDPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
ERASEPAGE	1	In	When asserted, the address page is to be programmed with all zeros. ERASEPAGE must transition synchronously with the rising edge of CLK.
LOCKREQUEST	1	In	When asserted, indicates to the JTAG controller that the FPGA interface is accessing the FB.
OVERWRITEPAGE	1	In	When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable.
OVERWRITEPROTECT	1	In	When asserted, all program operations will set the overwrite protect bit of the page being programmed.
PAGESTATUS	1	In	When asserted with REN, initiates a read page status operation.
PAGELOSSPROTECT	1	In	When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page.
PIPE	1	In	Adds a pipeline stage to the output for operation above 50 MHz.
PROGRAM	1	In	When asserted, writes the contents of the Page Buffer into the FB page addressed.
RD[31:0]	32	Out	Read data; data will be valid from the first non-busy cycle (BUSY = 0) after REN has been asserted.
READNEXT	1	In	When asserted with REN, initiates a read-next operation.
REN	1	In	When asserted, initiates a read operation.
RESET	1	In	When asserted, resets the state of the FB (active low).
SPAREPAGE	1	In	When asserted, the sector addressed is used to access the spare page within that sector.

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to [Figure 2-47](#) for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in [Table 2-27 on page 2-58](#).

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

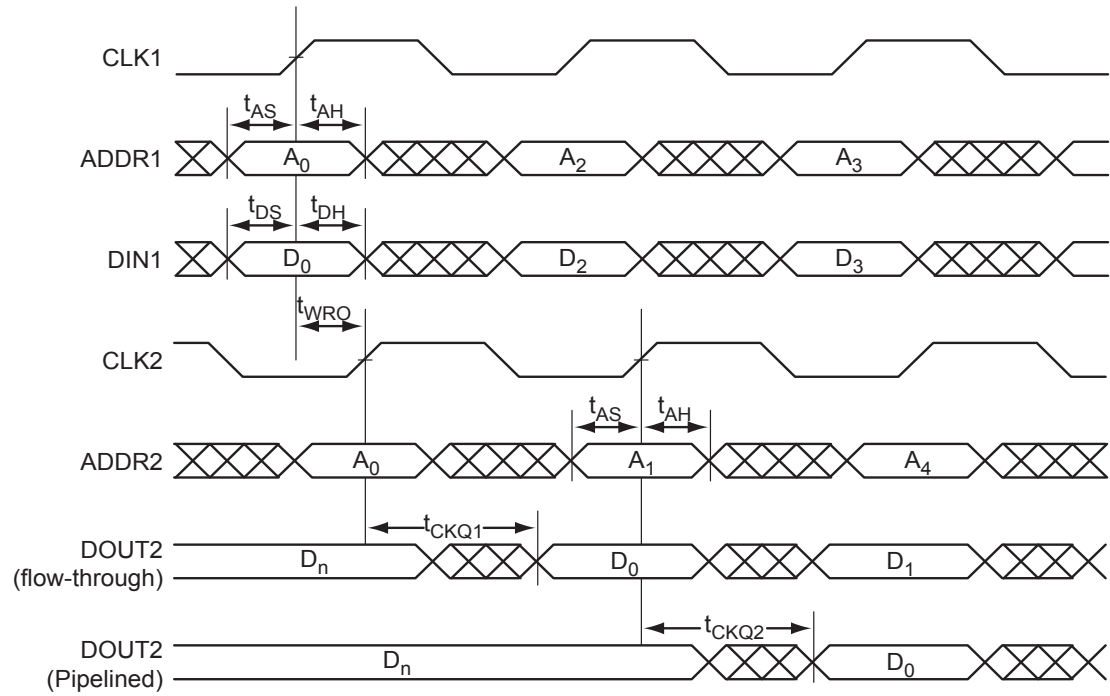


Figure 2-54 • One Port Write / Other Port Read Same

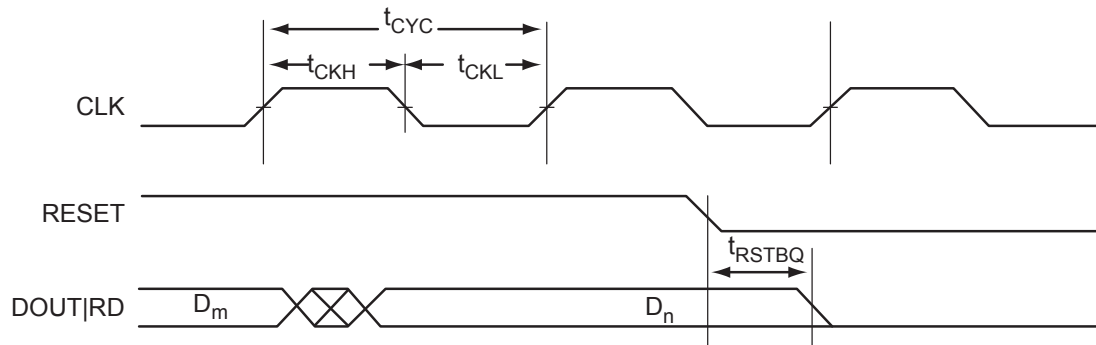


Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18.

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-87).

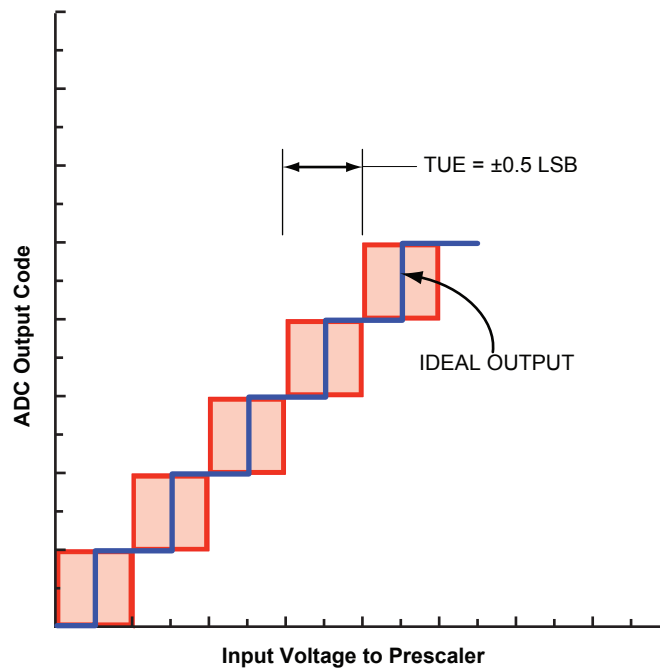


Figure 2-87 • Total Unadjusted Error (TUE)

ADC Operation

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-89 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by post-calibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-91 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADCSTART is issued. The DATAVALID goes low on the rising edge of SYSCLK as shown in Figure 2-90 on page 2-112. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVALID rising edge.

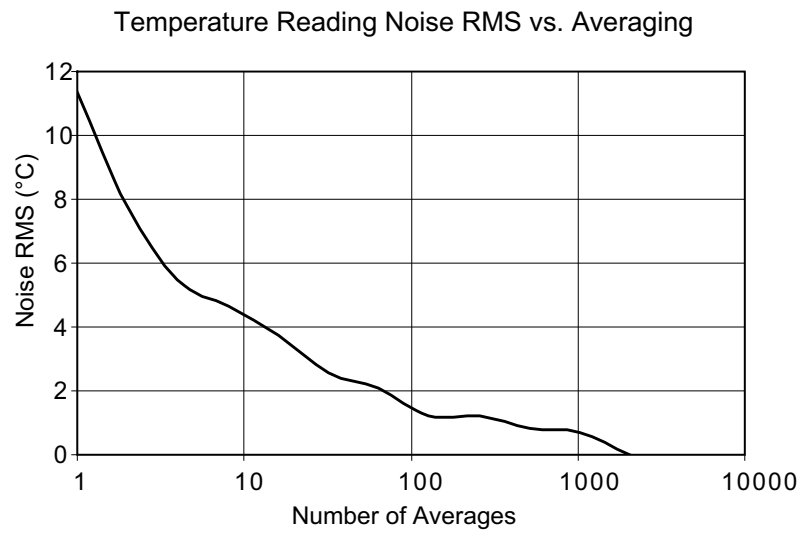


Figure 2-96 • Temperature Reading Noise When Averaging is Used

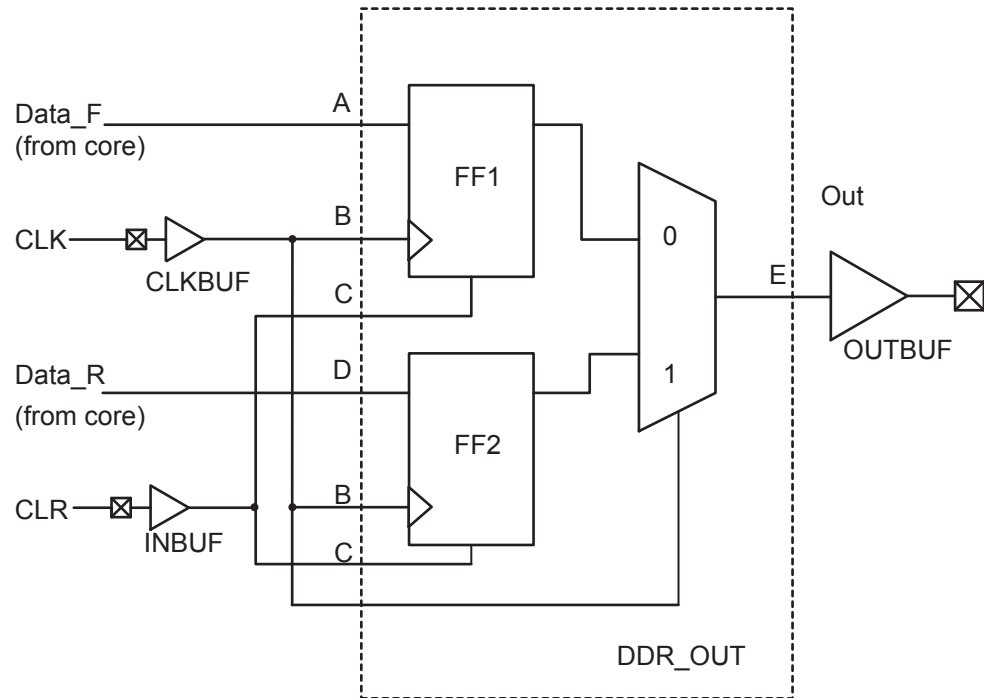


Figure 2-102 • DDR Output Support in Fusion Devices

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in [Table 3-4 on page 3-4](#). This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in [Figure 2-105](#). Relying on the diode clamping would create an excessive pad DC voltage of $3.3\text{ V} + 0.7\text{ V} = 4\text{ V}$.

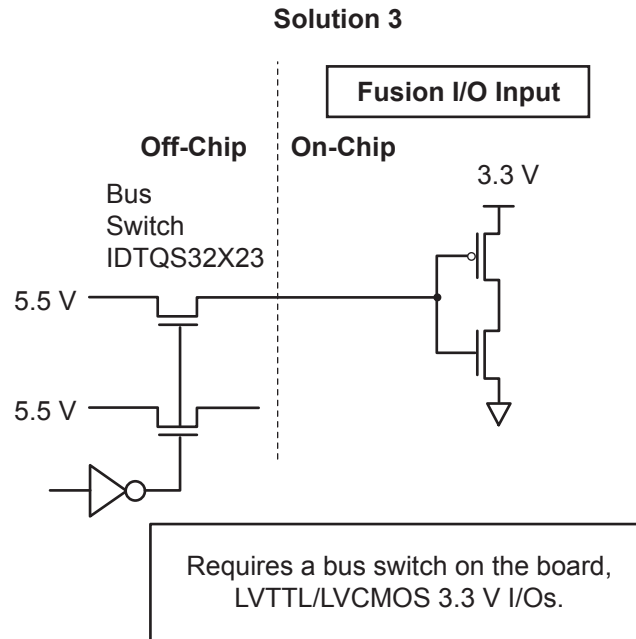


Figure 2-105 • Solution 3

Solution 4

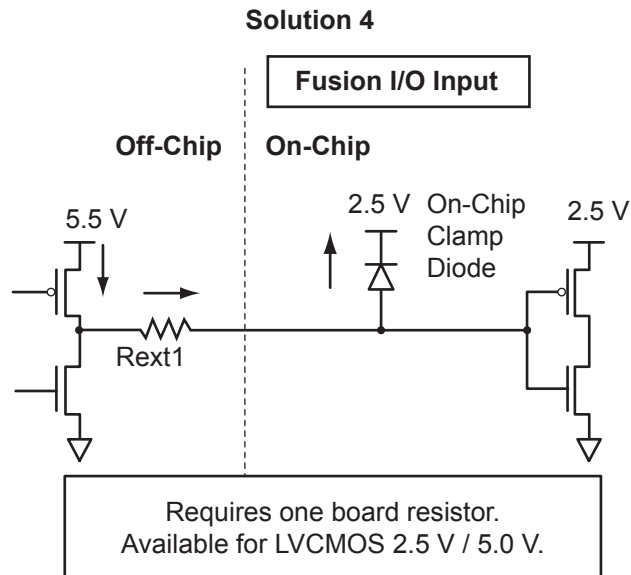


Figure 2-106 • Solution 4

Table 2-83 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages

I/O Standard	Input/Output Supply Voltage (VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V / 5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, BLVDS, M-LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

User I/O Characteristics

Timing Model

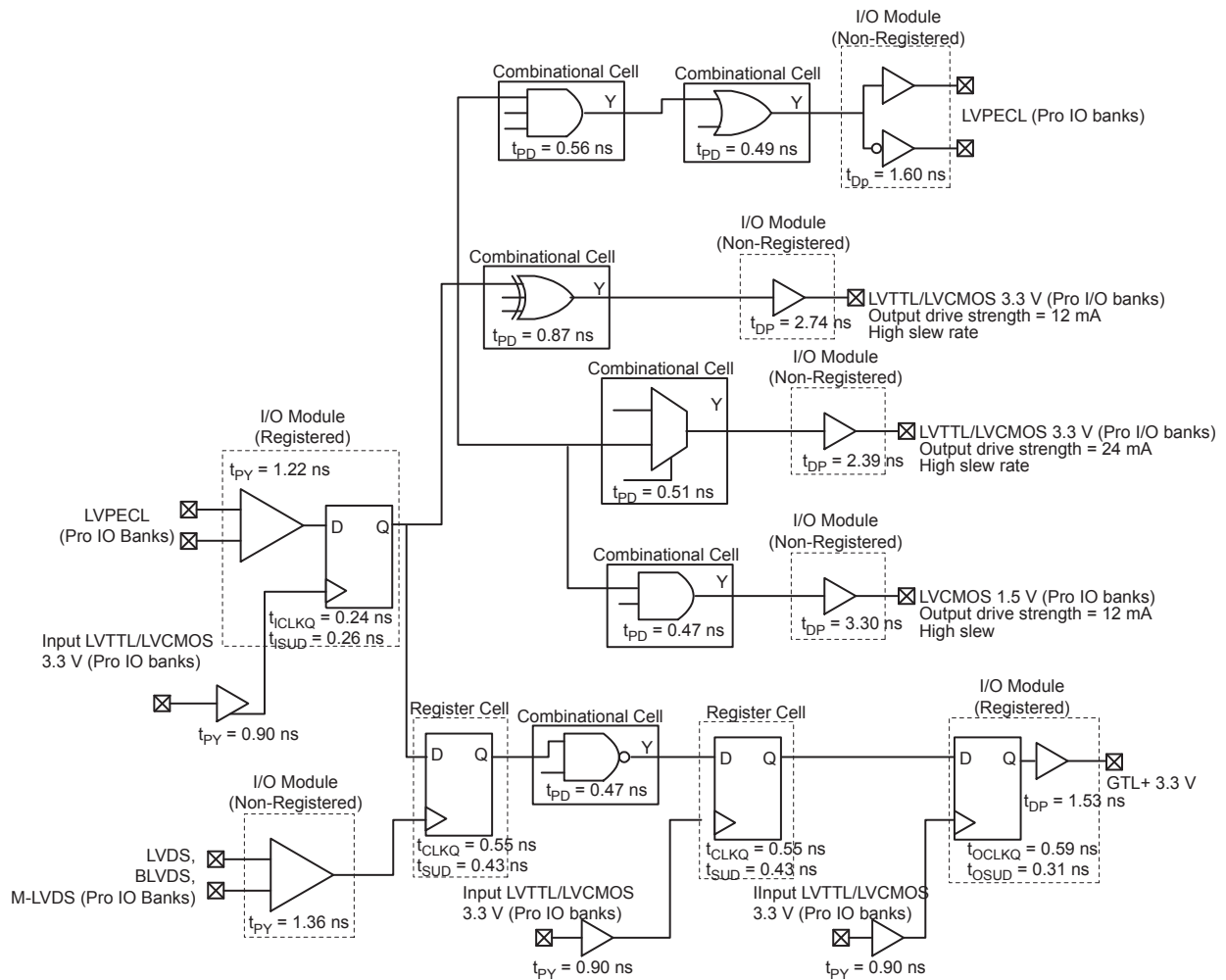


Figure 2-115 • Timing Model

**Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$),
Worst-Case VCC = 1.425 V**

Table 2-117 • 2.5 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-121 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-174 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-137 on page 2-212 for more information.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

where

$\theta_{JA} = 19.00^{\circ}\text{C/W}$ (taken from Table 3-6 on page 3-7).

$T_A = 75.00^{\circ}\text{C}$

$$\text{Maximum Power Allowed} = \frac{100.00^{\circ}\text{C} - 75.00^{\circ}\text{C}}{19.00^{\circ}\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

$T_J = 100.00^{\circ}\text{C}$

$T_A = 70.00^{\circ}\text{C}$

From the datasheet:

$\theta_{JA} = 17.00^{\circ}\text{C/W}$

$\theta_{JC} = 8.28^{\circ}\text{C/W}$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTTL/LVCMOS	35	3.3	—	474.70
2.5 V LVCMOS	35	2.5	—	270.73
1.8 V LVCMOS	35	1.8	—	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	—	104.55
3.3 V PCI	10	3.3	—	204.61
3.3 V PCI-X	10	3.3	—	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	—	24.08
2.5 V GTL	10	2.5	—	13.52
3.3 V GTL+	10	3.3	—	24.10
2.5 V GTL+	10	2.5	—	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS	—	2.5	7.70	89.62
LVPECL	—	3.3	19.42	168.02
Applicable to Advanced I/O Banks				
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	—	468.67
2.5 V LVCMOS	35	2.5	—	267.48
1.8 V LVCMOS	35	1.8	—	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	—	103.12
3.3 V PCI	10	3.3	—	201.02
3.3 V PCI-X	10	3.3	—	201.02

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.
2. PDC8 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CC} and V_{CCI}.

Static Power Consumption of Various Internal Resources

Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices

Parameter	Definition	Power Supply		Device-Specific Static Contributions				Units
				AFS1500	AFS600	AFS250	AFS090	
PDC1	Core static power contribution in operating mode	VCC	1.5 V	18	7.5	4.50	3.00	mW
PDC2	Device static power contribution in standby mode	VCC33A	3.3 V	0.66				mW
PDC3	Device static power contribution in sleep mode	VCC33A	3.3 V	0.03				mW
PDC4	NVM static power contribution	VCC	1.5 V	1.19				mW
PDC5	Analog Block static power contribution of ADC	VCC33A	3.3 V	8.25				mW
PDC6	Analog Block static power contribution per Quad	VCC33A	3.3 V	3.3				mW
PDC7	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-12 on page 3-18					
PDC8	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-13 on page 3-20					
PDC9	Static contribution for PLL	VCC	1.5 V	2.55				mW

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 3-16 on page 3-27](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 3-17 on page 3-27](#).
- Read rate and write rate to the RAM—guidelines are provided for typical applications in [Table 3-17 on page 3-27](#).
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

RC Oscillator Dynamic Contribution— P_{RC-OSC}

Operating Mode

$$P_{RC-OSC} = PAC19$$

Standby Mode and Sleep Mode

$$P_{RC-OSC} = 0 \text{ W}$$

Analog System Dynamic Contribution— P_{AB}

Operating Mode

$$P_{AB} = PAC20$$

Standby Mode and Sleep Mode

$$P_{AB} = 0 \text{ W}$$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 3-16 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-17 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

Power Consumption

Table 3-18 • Power Consumption

Parameter	Description	Condition	Min.	Typical	Max.	Units
Crystal Oscillator						
ISTBXTAL	Standby Current of Crystal Oscillator			10		μA
IDYNXTAL	Operating Current	RC		0.6		mA
		0.032–0.2		0.19		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
RC Oscillator						
IDYNRC	Operating Current			1		mA
ACM						
	Operating Current (fixed clock)			200		μA/MHz
	Operating Current (user clock)			30		μA
NVM System						
	NVM Array Operating Power	Idle		795		μA
		Read operation		See Table 3-15 on page 3-23.		See Table 3-15 on page 3-23.
		Erase		900		μA
		Write		900		μA
PNVMCTRL	NVM Controller Operating Power			20		μW/MHz

FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
H3	XTAL2	XTAL2	XTAL2	XTAL2
H4	XTAL1	XTAL1	XTAL1	XTAL1
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC
H7	VCC	VCC	VCC	VCC
H8	GND	GND	GND	GND
H9	VCC	VCC	VCC	VCC
H10	GND	GND	GND	GND
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
J7	GND	GND	GND	GND
J8	VCC	VCC	VCC	VCC
J9	GND	GND	GND	GND
J10	VCC	VCC	VCC	VCC
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0
K5	GND	GND	GND	GND
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0
K7	VCC	VCC	VCC	VCC
K8	GND	GND	GND	GND

FG484		
Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2
L18	IO46PDB2V0	IO69PDB2V0
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
L20	VCCIB2	VCCIB2
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
M1	NC	IO103PDB4V0
M2	XTAL1	XTAL1
M3	VCCIB4	VCCIB4
M4	GNDOSC	GNDOSC
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
M6	VCCIB4	VCCIB4
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
M8	VCCIB4	VCCIB4
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M15	VCCIB2	VCCIB2
M16	IO48NDB2V0	IO70NDB2V0
M17	VCCIB2	VCCIB2
M18	IO46NDB2V0	IO69NDB2V0
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
M20	VCCIB2	VCCIB2
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
N1	NC	IO103NDB4V0
N2	GND	GND
N3	IO68PDB4V0	IO101PDB4V0
N4	NC	IO100NPB4V0
N5	GND	GND
N6	NC	IO99PDB4V0
N7	NC	IO97PDB4V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
N8	GND	GND
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
N17	NC	IO78PDB2V0
N18	GND	GND
N19	IO47NDB2V0	IO72NDB2V0
N20	IO47PDB2V0	IO72PDB2V0
N21	GND	GND
N22	IO49PDB2V0	IO71PDB2V0
P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
P3	IO68NDB4V0	IO101NDB4V0
P4	IO65PDB4V0	IO96PDB4V0
P5	IO65NDB4V0	IO96NDB4V0
P6	NC	IO99NDB4V0
P7	NC	IO97NDB4V0
P8	VCCIB4	VCCIB4
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P15	VCCIB2	VCCIB2
P16	IO56NDB2V0	IO83NDB2V0
P17	NC	IO78NDB2V0
P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
P20	IO51NDB2V0	IO73NDB2V0