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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	75
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-2fg256i

Email: info@E-XFL.COM

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 2-6 • Sequential Timing Model and Waveforms

Sequential Timing Characteristics

Table 2-2 • Register Delays
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t _{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t _{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t _{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t _{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t _{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t _{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t _{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t _{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t _{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t _{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t _{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t _{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t _{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t _{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

 Table 2-5 • AFS1500 Global Resource Timing

 Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	_	-2		1	S	Unito	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t _{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-6 • AFS600 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2		-	-1	S	Unite	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
t _{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.





Figure 2-21 • Fusion CCC Options: Global Buffers with Programmable Delay

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



GAA[0:2]: GA represents global in the northwest corner of the device. A[0:2]: designates specific A clock source.

Notes:

- 1. Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-158 for more information.
- 2. Instantiate the routed clock source input as follows:
 - a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro. b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
- 3. LVDS-based clock sources are available in the east and west banks on all Fusion devices.

Figure 2-22 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT

CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- · 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • PLL Block



Table 2-16 • RTC Control/Status Register

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset	
		1 – Resets the RTC	
		0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable	0
		1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges.	
		0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	
5	vr_en_mat	Voltage Regulator Enable on Match	0
		1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM.	
		0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	
4:3	xt_mode[1:0]	Crystal Mode	00
		Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	
2	rst_cnt_omat	Reset Counter on Match	0
		1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled.	
		0 – Counter increments indefinitely	
1	rstb_cnt	Counter Reset, active Low	0
		0 - Resets the 40-bit counter value	
0	xtal_en	Crystal Enable	0
		Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC.	
		0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0.	
		1 – Enables XTLOSC, XTL_MODE control by xt_mode	
		Standby mode requires this bit to be set to 1.	
		See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	



Flash Memory Block Addressing

Figure 2-34 shows a graphical representation of the flash memory block.



Figure 2-34 • Flash Memory Block Organization

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data. Addressing for the FB is shown in Table 2-20.

Table 2-20 • FB Address Bit Allocation ADDR[17:0]

17	12	11	7	6	4	3	0
Sec	ctor	Pa	ge	Blo	ock	Ву	/te

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.



Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.



Figure 2-35 • FB Write Waveform

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

- 1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
- 2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.



Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-87).



Figure 2-87 • Total Unadjusted Error (TUE)

ADC Operation

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-89 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by postcalibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-91 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADCSTART is issued. The DATAVALID goes low on the rising edge of SYSCLK as shown in Figure 2-90 on page 2-112. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVLAID rising edge.



Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table	2-56 •	Analog	Quad	Bvte /	Assianme	nt
1 4010	200	Analog	auuu .		Rooiginno	

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0	0	B0[0]	Scaling factor control – prescaler	Highest voltage range
(AV)	1	B0[1]		
	2	B0[2]	-	
	3	B0[3]	Analog MUX select	Prescaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	Prescaler op amp mode	Power-down
Byte 1	0	B1[0]	Scaling factor control – prescaler	Highest voltage range
(AC)	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Prescaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Prescaler op amp mode	Power-down
Byte 2	0	B2[0]	Internal chip temperature monitor *	Off
(AG)	1	B2[1]	Spare	-
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	-
	5	B2[5]	Spare	-
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3	0	B3[0]	Scaling factor control – prescaler	Highest voltage range
(AT)	1	B3[1]	-	
	2	B3[2]	-	
	3	B3[3]	Analog MUX select	Prescaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	_	-
	7	B3[7]	Prescaler op amp mode	Power-down

Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.



Table 2-81 • Fusion Pro I/O Default Attributes

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMO S 3.3 V	Refer to the following tables for more	Refer to the following tables for more	Off	None	35 pF	-	Off	0	Off
LVCMOS 2.5 V	Table 2-78 on page 2-152	Table 2-78 on page 2-152	Off	None	35 pF	-	Off	0	Off
LVCMOS 2.5/5.0 V	Table 2-79 on page 2-152 Table 2-80 on page 2-152	Table 2-79 on page 2-152 Table 2-80 on page 2-152	Off	None	35 pF	-	Off	0	Off
LVCMOS 1.8 V	10010 2 00 011 page 2-102		Off	None	35 pF	-	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	-	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	-	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	-	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	-	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	-	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	-	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	-	Off	0	Off
HSTL Class I			Off	None	20 pF	-	Off	0	Off
HSTL Class II			Off	None	20 pF	-	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	-	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	-	Off	0	Off
LVDS, BLVDS, M-LVDS			Off	None	0 pF	_	Off	0	Off
LVPECL			Off	None	0 pF	_	Off	0	Off

User I/O Characteristics

Timing Model



Figure 2-115	Timing Model
	Operating Conditions: -2 Speed, Commercial Temperature Range (T _J = 70°C),
	Worst-Case VCC = 1.425 V





Figure 2-118 • Tristate Output Buffer Timing Model and Delays (example)

Table 2-96 • I/O Output Buffer Maximum Resistances ¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Ba	nks		•
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

 These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec

Table 2-132 • 1.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	-1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	-2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-133 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	-1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	-2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Symbol	Parameter	Commercial	Industrial	Units	
VCC	DC core supply voltage	-0.3 to 1.65	–0.3 to 1.65	V	
VJTAG	JTAG DC voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VPUMP	Programming voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	-0.3 to 1.65	V	
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VI	I/O input voltage ¹	 -0.3 V to 3.6 V (when I/O hot insertion mode is enabled) -0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) 			
VCC33A	+3.3 V power supply	–0.3 to 3.75 ²	–0.3 to 3.75 ²	V	
VCC33PMP	+3.3 V power supply	-0.3 to 3.75 ²	-0.3 to 3.75 ²	V	
VAREF	Voltage reference for ADC	-0.3 to 3.75	-0.3 to 3.75	V	
VCC15A	Digital power supply for the analog system	-0.3 to 1.65	–0.3 to 1.65	V	
VCCNVM	Embedded flash power supply	-0.3 to 1.65	-0.3 to 1.65	V	
VCCOSC	Oscillator power supply	-0.3 to 3.75	-0.3 to 3.75	V	

Table 3-1 • Absolute Maximum Ratings

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

Maximum Power Allowed =
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

 θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-7).

 $T_A = 75.00^{\circ}C$

Maximum Power Allowed =
$$\frac{100.00^{\circ}C - 75.00^{\circ}C}{19.00^{\circ}C/W} = 1.3 W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

 $T_{J} = 100.00^{\circ}C$

 $T_A = 70.00^{\circ}C$

From the datasheet:

 $\theta_{JA} = 17.00^{\circ}C/W$ $\theta_{JC} = 8.28^{\circ}C/W$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}C - 70^{\circ}C}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6



Package Pin Assignments

QN180					
Pin Number	AFS090 Function	AFS250 Function			
C21	AG2	AG2			
C22	NC	NC			
C23	NC	NC			
C24	NC	NC			
C25	NC	AT5			
C26	GNDAQ	GNDAQ			
C27	NC	NC			
C28	NC	NC			
C29	NC	NC			
C30	NC	NC			
C31	GND	GND			
C32	NC	NC			
C33	NC	NC			
C34	NC	NC			
C35	GND	GND			
C36	GDB0/IO39NPB1V0	GDA0/IO54NPB1V0			
C37	GDA1/IO37NSB1V0	GDC0/IO52NSB1V0			
C38	GCA0/IO36NDB1V0	GCA0/IO49NDB1V0			
C39	GCB1/IO35PPB1V0	GCB1/IO48PPB1V0			
C40	GND	GND			
C41	GCA2/IO32NPB1V0	IO41NPB1V0			
C42	GBB2/IO31NDB1V0	IO40NDB1V0			
C43	NC	NC			
C44	NC	GBA1/IO39RSB0V0			
C45	NC	GBB0/IO36RSB0V0			
C46	GND	GND			
C47	NC	IO30RSB0V0			
C48	IO22RSB0V0	IO27RSB0V0			
C49	GND	GND			
C50	IO13RSB0V0	IO16RSB0V0			
C51	IO09RSB0V0	IO12RSB0V0			
C52	IO06RSB0V0	IO09RSB0V0			
C53	GND	GND			
C54	NC	GAB1/IO03RSB0V0			
C55	NC	GAA0/IO00RSB0V0			
C56	NC	NC			

QN180					
Pin Number	AFS090 Function	AFS250 Function			
D1	NC	NC			
D2	NC	NC			
D3	NC	NC			
D4	NC	NC			



Package Pin Assignments

	FG484		FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND	AA14	AG7	AG7
A2	VCC	NC	AA15	AG8	AG8
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	AA16	GNDA	GNDA
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0	AA17	AG9	AG9
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0	AA18	VAREF	VAREF
A6	IO07NDB0V1	IO07NDB0V1	AA19	VCCIB2	VCCIB2
A7	IO07PDB0V1	IO07PDB0V1	AA20	PTEM	PTEM
A8	IO10PDB0V1	IO09PDB0V1	AA21	GND	GND
A9	IO14NDB0V1	IO13NDB0V2	AA22	VCC	NC
A10	IO14PDB0V1	IO13PDB0V2	AB1	GND	GND
A11	IO17PDB1V0	IO24PDB1V0	AB2	VCC	NC
A12	IO18PDB1V0	IO26PDB1V0	AB3	NC	IO94NSB4V0
A13	IO19NDB1V0	IO27NDB1V1	AB4	GND	GND
A14	IO19PDB1V0	IO27PDB1V1	AB5	VCC33N	VCC33N
A15	IO24NDB1V1	IO35NDB1V2	AB6	AT0	AT0
A16	IO24PDB1V1	IO35PDB1V2	AB7	ATRTN0	ATRTN0
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2	AB8	AT1	AT1
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	AB9	AT2	AT2
A19	IO29NDB1V1	IO43NDB1V2	AB10	ATRTN1	ATRTN1
A20	IO29PDB1V1	IO43PDB1V2	AB11	AT3	AT3
A21	VCC	NC	AB12	AT6	AT6
A22	GND	GND	AB13	ATRTN3	ATRTN3
AA1	VCC	NC	AB14	AT7	AT7
AA2	GND	GND	AB15	AT8	AT8
AA3	VCCIB4	VCCIB4	AB16	ATRTN4	ATRTN4
AA4	VCCIB4	VCCIB4	AB17	AT9	AT9
AA5	PCAP	PCAP	AB18	VCC33A	VCC33A
AA6	AG0	AG0	AB19	GND	GND
AA7	GNDA	GNDA	AB20	NC	IO76NPB2V0
AA8	AG1	AG1	AB21	VCC	NC
AA9	AG2	AG2	AB22	GND	GND
AA10	GNDA	GNDA	B1	VCC	NC
AA11	AG3	AG3	B2	GND	GND
AA12	AG6	AG6	B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
AA13	GNDA	GNDA	B4	GND	GND



Datasheet Information

Revision	Changes	Page
Advance v0.8 (continued)	The voltage range in the "VPUMP Programming Supply Voltage" section was updated. The parenthetical reference to "pulled up" was removed from the statement, "VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V."	2-225
	The "ATRTNx Temperature Monitor Return" section was updated with information about grounding and floating the pin.	2-226
	The following text was deleted from the "VREF I/O Voltage Reference" section: (all digital I/O).	2-225
	The "NCAP Negative Capacitor" section and "PCAP Positive Capacitor" section were updated to include information about the type of capacitor that is required to connect the two.	2-228
	1 µF was changed to 100 pF in the "XTAL1 Crystal Oscillator Circuit Input".	2-228
	The "Programming" section was updated to include information about V_{CCOSC} .	2-229
	The VMV pins have now been tied internally with the V _{CCI} pins.	N/A
	The AFS090"108-Pin QFN" table was updated.	3-2
	The AFS090 and AFS250 devices were updated in the "108-Pin QFN" table.	3-2
	The AFS250 device was updated in the "208-Pin PQFP" table.	3-8
	The AFS600 device was updated in the "208-Pin PQFP" table.	3-8
	The AFS090, AFS250, AFS600, and AFS1500 devices were updated in the "256-Pin FBGA" table.	3-12
	The AFS600 and AFS1500 devices were updated in the "484-Pin FBGA" table.	3-20
Advance v0.7	The AFS600 device was updated in the "676-Pin FBGA" table.	3-28
(January 2007)	The AFS1500 digital I/O count was updated in the "Fusion Family" table.	I
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	II
Advance v0.6 (October 2006)	The second paragraph of the "PLL Macro" section was updated to include information about POWERDOWN.	2-30
	The description for bit 0 was updated in Table 2-17 · RTC Control/Status Register.	2-38
	3.9 was changed to 7.8 in the "Crystal Oscillator (Xtal Osc)" section.	2-40.
	All function descriptions in Table 2-18 · Signals for VRPSM Macro.	2-42
	In Table 2-19 • Flash Memory Block Pin Names, the RD[31:0] description was updated.	2-43
	The "RESET" section was updated.	2-61
	The "RESET" section was updated.	2-64
	Table 2-35 • FIFO was updated.	2-79
	The VAREF function description was updated in Table 2-36 • Analog Block Pin Description.	2-82
	The "Voltage Monitor" section was updated to include information about low power mode and sleep mode.	2-86
	The text in the "Current Monitor" section was changed from 2 mV to 1 mV.	2-90
	The "Gate Driver" section was updated to include information about forcing 1 V on the drain.	2-94