



Welcome to [E-XFL.COM](#)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

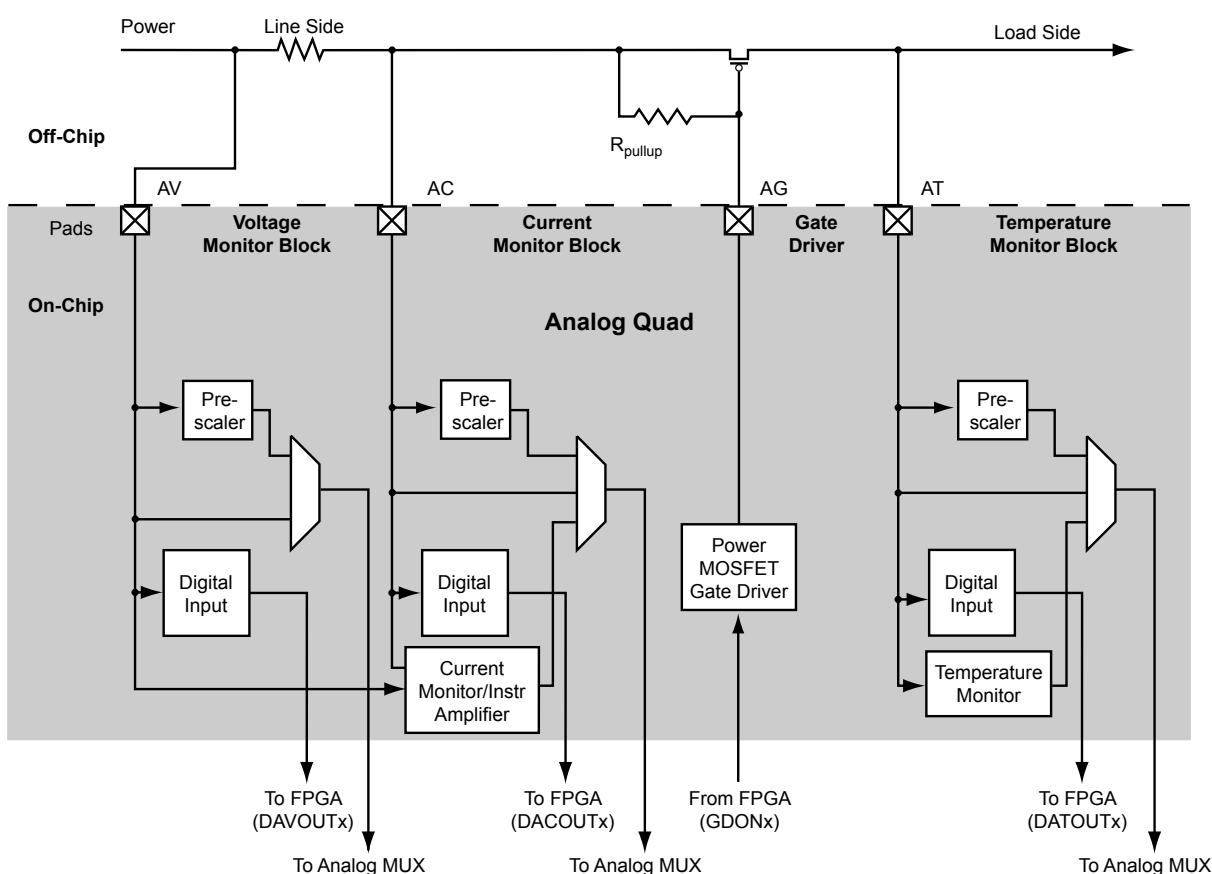
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

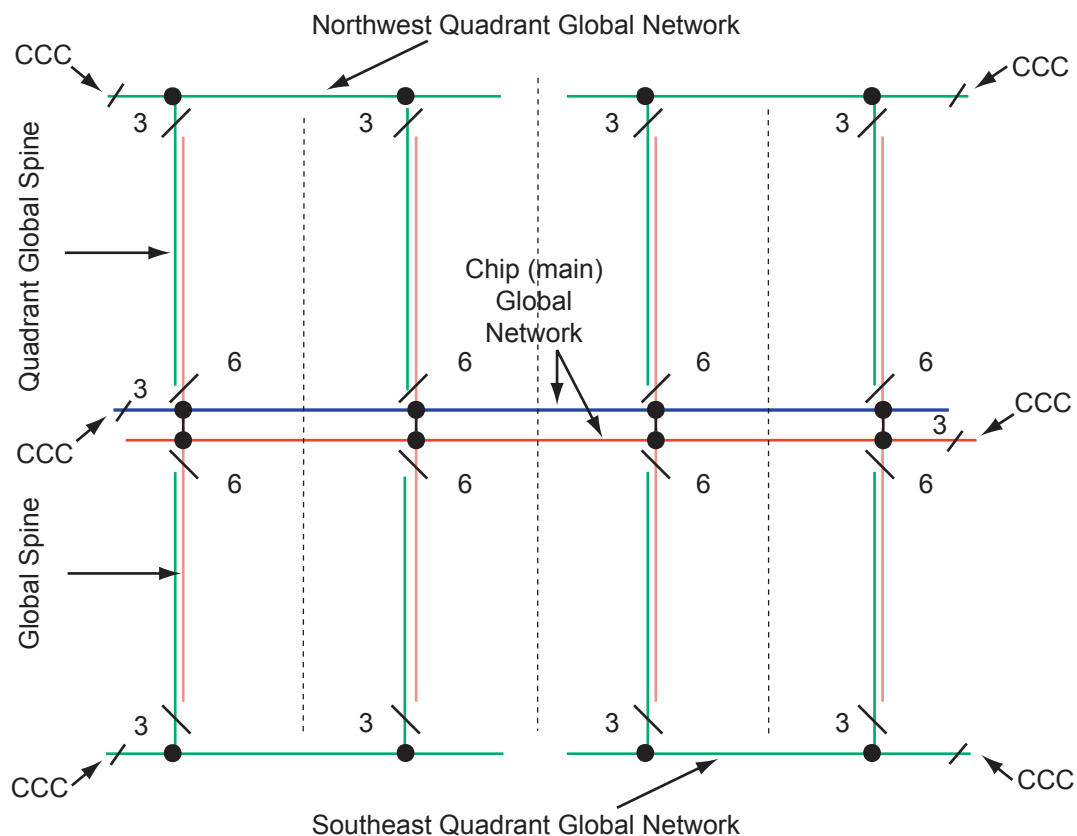
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	75
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/afs090-2fgg256">https://www.e-xfl.com/product-detail/microsemi/afs090-2fgg256</a>

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.



**Figure 1-1 • Analog Quad**



**Figure 2-12 • Global Network Architecture**

**Table 2-4 • Globals/Spines/Rows by Device**

	<b>AFS090</b>	<b>AFS250</b>	<b>AFS600</b>	<b>AFS1500</b>
Global VersaNets (trees)*	9	9	9	9
VersaNet Spines/Tree	4	8	12	20
Total Spines	36	72	108	180
VersaTiles in Each Top or Bottom Spine	384	768	1,152	1,920
Total VersaTiles	2,304	6,144	13,824	38,400

*Note:* \*There are six chip (main) globals and three globals per quadrant.

### VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. [Table 2-5](#), [Table 2-6](#), [Table 2-7](#), and [Table 2-8](#) on [page 2-17](#) present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading, respectively.

#### Timing Characteristics

**Table 2-5 • AFS1500 Global Resource Timing**  
Commercial Temperature Range Conditions:  $T_j = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

**Table 2-6 • AFS600 Global Resource Timing**  
Commercial Temperature Range Conditions:  $T_j = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).



## Real-Time Counter System

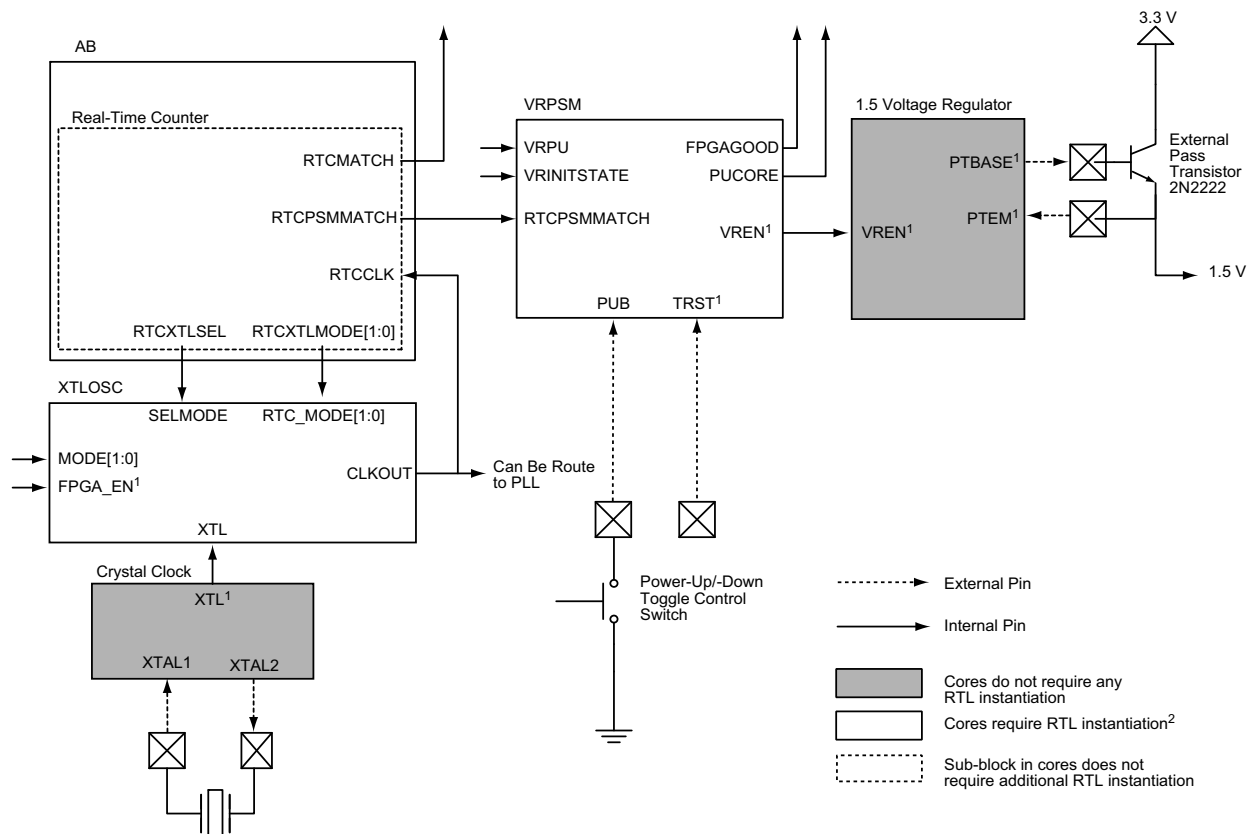
The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10  $\mu$ A
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the [Fusion FPGA Fabric User Guide](#) for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. [Figure 2-27](#) shows their connection.



### Notes:

1. Signals are hardwired internally and do not exist in the macro core.
2. User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.

**Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro)**

### Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

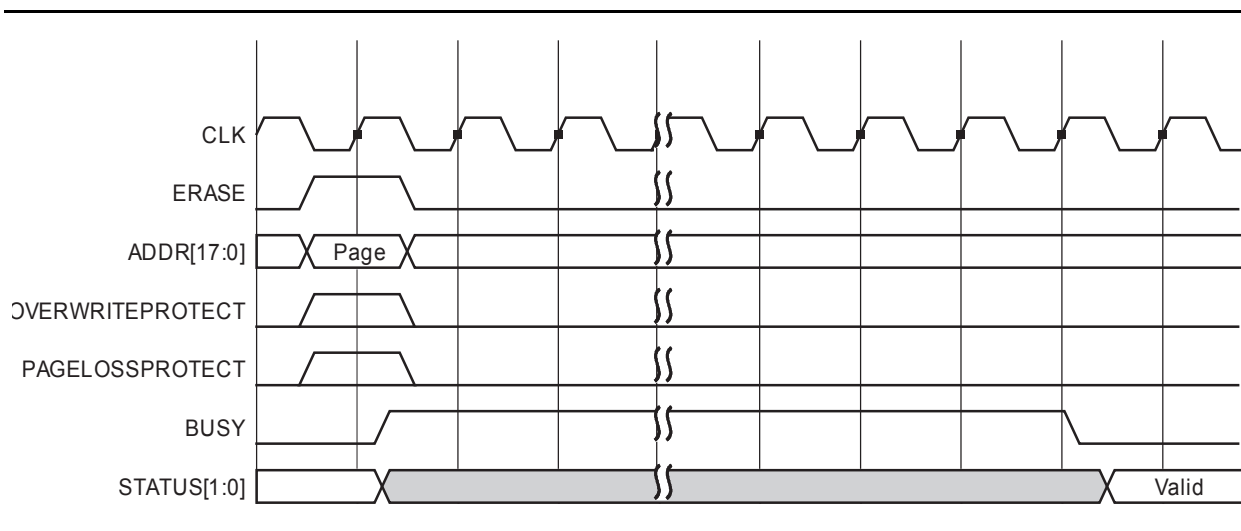
The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in [Figure 2-37](#).

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')



**Figure 2-37 • FB Erase Page Waveform**

### ***DINA and DINB***

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded ([Table 2-29](#)).

### ***DOUTA and DOUTB***

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used ([Table 2-29](#)). The output data on unused pins is undefined.

**Table 2-29 • Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

<b>D×W</b>	<b>DINx/DOUTx</b>	
	<b>Unused</b>	<b>Used</b>
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

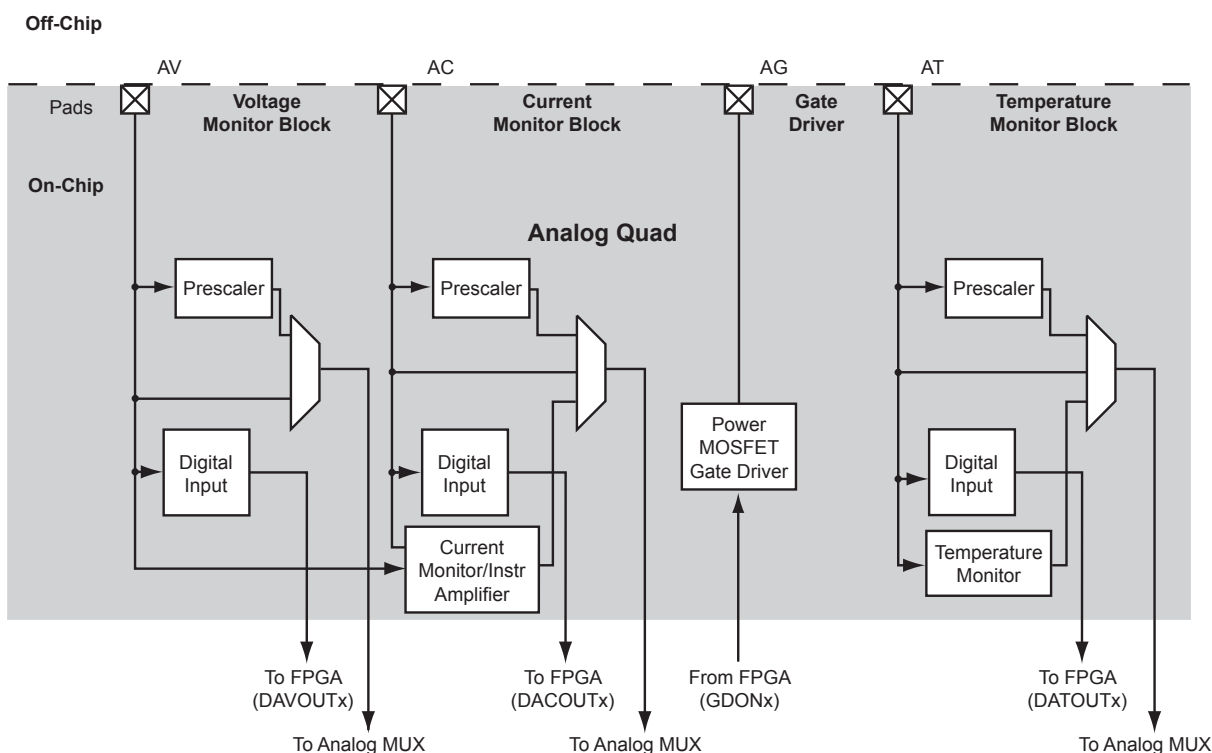
*Note:* The "x" in DINx and DOUTx implies A or B.

The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, ..., AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.



**Figure 2-65 • Analog Quad**

**Table 2-51 • Uncalibrated Analog Channel Accuracy\***  
**Worst-Case Industrial Conditions, T<sub>J</sub> = 85°C**

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	Prescaler Range (V)	Neg. Max.	Med.	Pos. Max.	Neg. Max	Med.	Pos. Max.	Neg. Max.	Med.	Pos. Max.	Min.	Typ.	Max.
<b>Positive Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-22	-2	12	-11	-2	14	-169	-32	224	3	0	-3
	8	-40	-5	17	-11	-5	21	-87	-40	166	2	0	-4
	4	-45	-9	24	-16	-11	36	-63	-43	144	2	0	-4
	2	-70	-19	33	-33	-20	66	-66	-39	131	2	0	-4
	1	-25	-7	5	-11	-3	26	-11	-3	26	3	-1	-3
	0.5	-41	-12	8	-12	-7	38	-6	-4	19	3	-1	-3
	0.25	-53	-14	19	-20	-14	40	-5	-3	10	5	0	-4
	0.125	-89	-29	24	-40	-28	88	-5	-4	11	7	0	-5
AT	16	-3	9	15	-4	0	4	-64	5	64	1	0	-1
	4	-10	2	15	-11	-2	11	-44	-8	44	1	0	-1
<b>Negative Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-35	-10	9	-24	-6	9	-383	-96	148	5	-1	-6
	8	-65	-19	12	-34	-12	9	-268	-99	75	5	-1	-5
	4	-86	-28	21	-64	-24	19	-254	-96	76	5	-1	-6
	2	-136	-53	37	-115	-42	39	-230	-83	78	6	-2	-7
	1	-98	-35	8	-39	-8	15	-39	-8	15	10	-3	-10
	0.5	-121	-46	7	-54	-14	18	-27	-7	9	10	-4	-11
	0.25	-149	-49	19	-72	-16	40	-18	-4	10	14	-4	-12
	0.125	-188	-67	38	-112	-27	56	-14	-3	7	16	-5	-14

**Note:** \*Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.

## Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

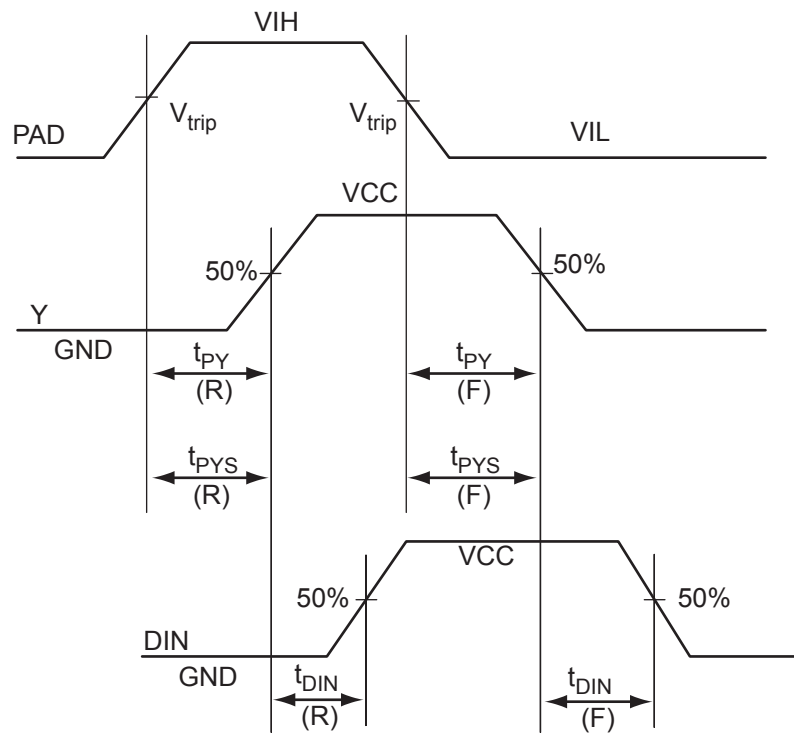
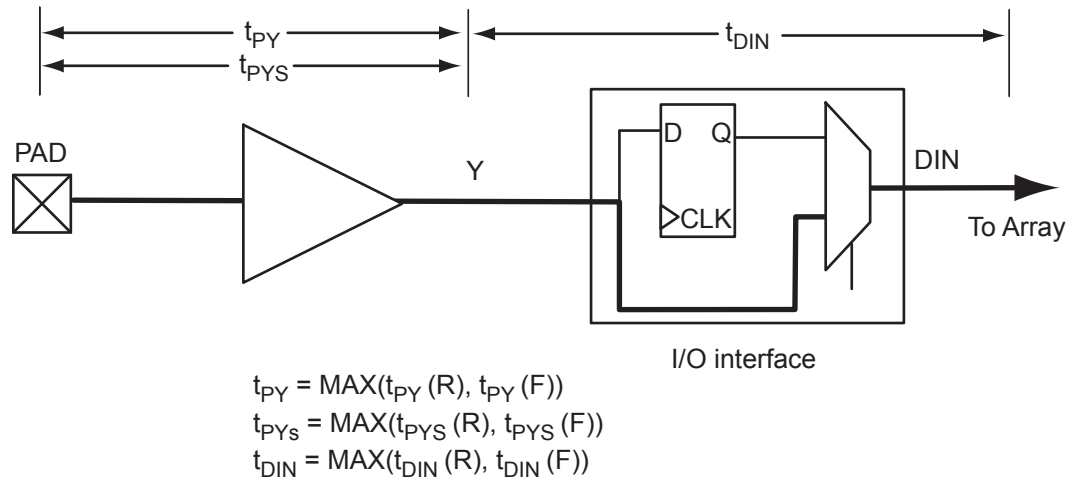
**Table 2-56 • Analog Quad ACM Byte Assignment**

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0 (AV)	0	B0[0]	Scaling factor control – prescaler	Highest voltage range
	1	B0[1]		
	2	B0[2]		
	3	B0[3]	Analog MUX select	Prescaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	Prescaler op amp mode	Power-down
Byte 1 (AC)	0	B1[0]	Scaling factor control – prescaler	Highest voltage range
	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Prescaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Prescaler op amp mode	Power-down
Byte 2 (AG)	0	B2[0]	Internal chip temperature monitor *	Off
	1	B2[1]	Spare	–
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	–
	5	B2[5]	Spare	–
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3 (AT)	0	B3[0]	Scaling factor control – prescaler	Highest voltage range
	1	B3[1]		
	2	B3[2]		
	3	B3[3]	Analog MUX select	Prescaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	–	–
	7	B3[7]	Prescaler op amp mode	Power-down

**Note:** \*For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

**Table 2-85 • Fusion Pro I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, BLVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3



**Figure 2-116 • Input Buffer Timing Model and Delays (example)**



**Table 2-98 • I/O Short Currents IOSH/IOSL (continued)**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109
<b>Applicable to Standard I/O Banks</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

Note: \* $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at  $100^\circ\text{C}$ , the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

## Single-Ended I/O Characteristics

### 3.3 V LVTTL / 3.3 V LVCMOS

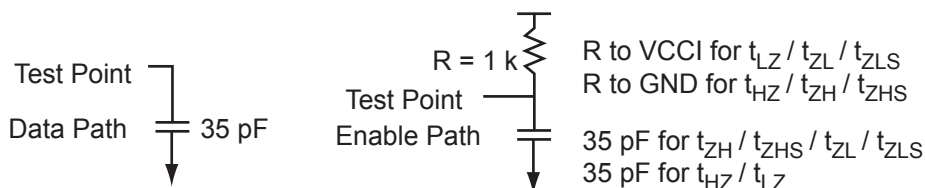
Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

**Table 2-102 • Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
<b>Applicable to Pro I/O Banks</b>												
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
<b>Applicable to Advanced I/O Banks</b>												
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
<b>Applicable to Standard I/O Banks</b>												
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10

**Notes:**

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-119 • AC Loading**

**Table 2-121 • 1.8 V LVCMOS High Slew**  
**Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ ,**  
**Worst-Case  $V_{CCI} = 1.7\text{ V}$**   
**Applicable to Pro I/Os**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

**Table 2-130 • 1.5 V LVCMOS Low Slew**

Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ ,  
Worst-Case  $V_{CCI} = 1.4\text{ V}$   
Applicable to Advanced I/Os

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	12.78	0.04	1.31	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.11	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	0.98	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.31	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.11	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	0.98	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
8 mA	Std.	0.66	9.33	0.04	1.31	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.11	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	0.98	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.31	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.11	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	0.98	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

**Table 2-131 • 1.5 V LVCMOS High Slew**

Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ ,  
Worst-Case  $V_{CCI} = 1.4\text{ V}$   
Applicable to Advanced I/Os

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	–1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	–2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	–1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	–2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
8 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	–1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	–2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	–1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	–2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

### Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

where

$\theta_{JA} = 19.00^{\circ}\text{C/W}$  (taken from Table 3-6 on page 3-7).

$T_A = 75.00^{\circ}\text{C}$

$$\text{Maximum Power Allowed} = \frac{100.00^{\circ}\text{C} - 75.00^{\circ}\text{C}}{19.00^{\circ}\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### Theta-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent  $T_a$  and  $T_j$  are given as follows:

$T_J = 100.00^{\circ}\text{C}$

$T_A = 70.00^{\circ}\text{C}$

From the datasheet:

$\theta_{JA} = 17.00^{\circ}\text{C/W}$

$\theta_{JC} = 8.28^{\circ}\text{C/W}$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

## Methodology

### Total Power Consumption— $P_{TOTAL}$

#### Operating Mode, Standby Mode, and Sleep Mode

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$P_{STAT}$  is the total static power consumption.

$P_{DYN}$  is the total dynamic power consumption.

### Total Static Power Consumption— $P_{STAT}$

#### Operating Mode

$$P_{STAT} = PDC1 + (N_{NVM-BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$$

$N_{NVM-BLOCKS}$  is the number of NVM blocks available in the device.

$N_{QUADS}$  is the number of Analog Quads used in the design.

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$N_{PLLS}$  is the number of PLLs available in the device.

#### Standby Mode

$$P_{STAT} = PDC2$$

#### Sleep Mode

$$P_{STAT} = PDC3$$

### Total Dynamic Power Consumption— $P_{DYN}$

#### Operating Mode

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$$

#### Standby Mode

$$P_{DYN} = P_{XTL-OSC}$$

#### Sleep Mode

$$P_{DYN} = 0 \text{ W}$$

### Global Clock Dynamic Contribution— $P_{CLOCK}$

#### Operating Mode

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

$N_{SPINE}$  is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

$N_{ROW}$  is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

$F_{CLK}$  is the global clock signal frequency.

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

#### Standby Mode and Sleep Mode

$$P_{CLOCK} = 0 \text{ W}$$

### Sequential Cells Dynamic Contribution— $P_{S-CELL}$

#### Operating Mode

FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
K9	VCC	VCC	VCC	VCC
K10	GND	GND	GND	GND
K11	NC	GDC2/IO57PPB1V0	GDC2/IO57PPB2V0	GDC2/IO84PPB2V0
K12	GND	GND	GND	GND
K13	NC	GDA0/IO54NDB1V0	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
K14	NC	GDA2/IO55PPB1V0	GDA2/IO55PPB2V0	GDA2/IO82PPB2V0
K15	VCCIB1	VCCIB1	VCCIB2	VCCIB2
K16	NC	GDB1/IO53PPB1V0	GDB1/IO53PPB2V0	GDB1/IO80PPB2V0
L1	NC	GEC1/IO63PDB3V0	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
L2	NC	GEC0/IO63NDB3V0	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
L3	NC	GEB1/IO62PDB3V0	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
L4	NC	GEB0/IO62NDB3V0	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0
L5	NC	IO60NDB3V0	IO60NDB4V0	IO87NDB4V0
L6	NC	GEC2/IO60PDB3V0	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
L7	GNDA	GNDA	GNDA	GNDA
L8	AC0	AC0	AC2	AC2
L9	AV2	AV2	AV4	AV4
L10	AC3	AC3	AC5	AC5
L11	PTEM	PTEM	PTEM	PTEM
L12	TDO	TDO	TDO	TDO
L13	VJTAG	VJTAG	VJTAG	VJTAG
L14	NC	IO57NPB1V0	IO57NPB2V0	IO84NPB2V0
L15	GDB2/IO41PPB1V0	GDB2/IO56PPB1V0	GDB2/IO56PPB2V0	GDB2/IO83PPB2V0
L16	NC	IO55NPB1V0	IO55NPB2V0	IO82NPB2V0
M1	GND	GND	GND	GND
M2	NC	GEA1/IO61PDB3V0	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
M3	NC	GEA0/IO61NDB3V0	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
M4	VCCIB3	VCCIB3	VCCIB4	VCCIB4
M5	NC	IO58NPB3V0	IO58NPB4V0	IO85NPB4V0
M6	NC	NC	AV0	AV0
M7	NC	NC	AC1	AC1
M8	AG1	AG1	AG3	AG3
M9	AC2	AC2	AC4	AC4
M10	AC4	AC4	AC6	AC6
M11	NC	AG5	AG7	AG7
M12	VPUMP	VPUMP	VPUMP	VPUMP
M13	VCCIB1	VCCIB1	VCCIB2	VCCIB2
M14	TMS	TMS	TMS	TMS

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to $V_{CC33A}$ .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 • Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41



## Datasheet Categories

### **Categories**

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "[Fusion Device Status](#)" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### **Advance**

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### **Preliminary**

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### **Production**

This version contains information that is considered to be final.

### **Export Administration Regulations (EAR)**

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

## Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at [http://www.microsemi.com/soc/documents/ORT\\_Report.pdf](http://www.microsemi.com/soc/documents/ORT_Report.pdf). Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.