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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	5
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Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	75
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-2fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Temperature Grade Offerings

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 ³	P1AFS1500 ³
MicroBlade Devices		U1AFS250 ⁴	U1AFS600 ⁴	U1AFS1500 ⁴
QN108 ⁵	C, I	-	-	_
QN180 ⁵	C, I	C, I	-	-
PQ208	-	C, I	C, I	-
FG256	C, I	C, I	C, I	C, I
FG484	-	-	C, I	C, I
FG676	-	-	-	C, I

Notes:

1. C = Commercial Temperature Range: 0°C to 85°C Junction

2. I = Industrial Temperature Range: -40°C to 100°C Junction

3. Pigeon Point devices are only offered in FG484 and FG256.

4. MicroBlade devices are only offered in FG256.

5. Package not available.

Speed Grade and Temperature Grade Matrix

	Std. ¹	-1	-2 ²
C ³	\checkmark	\checkmark	\checkmark
l ⁴	\checkmark	\checkmark	\checkmark

Notes:

1. MicroBlade devices are only offered in standard speed grade.

2. Pigeon Point devices are only offered in –2 speed grade.

3. C = Commercial Temperature Range: 0°C to 85°C Junction

4. I = Industrial Temperature Range: -40°C to 100°C Junction

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flashbased Fusion devices are Instant On and do not need to be loaded from an external boot PROM.

On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote insystem reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the

industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a

built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with

AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with

industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.



Figure 2-16 • Fusion Clocking Options



RAM4K9 Description



Figure 2-48 • RAM4K9



DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-29).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-29). The output data on unused pins is undefined.

Table 2-29 • Unused/Used Input and Output Data Pins for Various Supported Bus Widths

D×W	DINx/DOUTx							
D	Unused	Used						
4k×1	[8:1]	[0]						
2k×2	[8:2]	[1:0]						
1k×4	[8:4]	[3:0]						
512×9	None	[8:0]						

Note: The "x" in DINx and DOUTx implies A or B.



Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.



Figure 2-77 • Block Diagram for Temperature Monitor Circuit

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.





Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion ¹ (mV)	LSB for a 10-Bit Conversion ¹ (mV)	LSB for a 12-Bit Conversion ¹ (mV)	Full-Scale Voltage in 10-Bit Mode ²	Range Name
000 ³	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010 ³	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Notes:

1. LSB voltage equivalences assume VAREF = 2.56 V.

2. Full Scale voltage for n-bit mode: ((2ⁿ) - 1) x (LSB for a n-bit Conversion)

3. These are the only valid ranges for the Temperature Monitor Block Prescaler.

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[4]	Control Lines Bx[3] ADC Connected To					
0	0	Prescaler				
0	1	Direct input				
1	0	Current amplifier temperature monitor				
1	1	Not valid				

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*

Control Lines Bx[6]	Input Signal Polarity
0	Positive
1	Negative

Note: *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.



Table 2-73 • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to $3.3 \vee LVTTL$ or $3.3 \vee LVCMOS$ mode, Fusion I/Os can directly drive signals into $5 \vee TTL$ receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both $3.3 \vee LVTTL$ and $3.3 \vee LVCMOS$ modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of $5 \vee TTL$ receivers. Therefore, level '1' and level '0' will be recognized correctly by $5 \vee TTL$ receivers.

Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage = L(GND) * di/dt
- VCCI dip noise voltage = L(VCCI) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Table 2-117 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{zL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	-1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	-1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-134 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		V	IH	VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Per PCI specification	Per PCI curves								10	10		

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

- 2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
- 3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-123.



Figure 2-123 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the data path; Microsemi loading for tristate is described in Table 2-135.

Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	0.285 * VCCI for t _{DP(R)}	-	10
		0.615 * VCCI for t _{DP(F)}		

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t _{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t _{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t _{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t _{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t _{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F _{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t _{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t _{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t _{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV, AC	Analog Input (direct input to ADC)	-	2 kΩ (typical)
		-	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	-	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-3 • Input Resistance of Analog Pads

Table 3-4 • Overshoot and Undershoot Limits ¹

vccı	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/ Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at a junction temperature of 85°C.

2. The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

Maximum Power Allowed =
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

 θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-7).

 $T_A = 75.00^{\circ}C$

Maximum Power Allowed =
$$\frac{100.00^{\circ}C - 75.00^{\circ}C}{19.00^{\circ}C/W} = 1.3 W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

 $T_{J} = 100.00^{\circ}C$

 $T_A = 70.00^{\circ}C$

From the datasheet:

 $\theta_{JA} = 17.00^{\circ}C/W$ $\theta_{JC} = 8.28^{\circ}C/W$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}C - 70^{\circ}C}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

Power per I/O Pin

Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings

	VCCI (V)	Static Power PDC7 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Applicable to Pro I/O Banks	<u> </u>		
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3		17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	_	25.51
2.5 V LVCMOS	2.5	_	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	_	7.16
1.8 V LVCMOS	1.8	_	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	_	2.80
1.5 V LVCMOS (JESD8-11)	1.5	_	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	_	2.00
3.3 V PCI	3.3	_	18.82
3.3 V PCI – Schmitt trigger	3.3	_	20.12
3.3 V PCI-X	3.3	_	18.82
3.3 V PCI-X – Schmitt trigger	3.3	_	20.12
Voltage-Referenced	<u></u>		
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential	<u>.</u>		•
LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.

2. PAC9 is the total dynamic power measured on VCC and VCCI.



Package Pin Assignments

	QN180		QN180		
Pin Number	AFS090 Function	AFS250 Function	Pin Number	AFS090 Function	AFS250 Function
A1	GNDQ	GNDQ	A37	VPUMP	VPUMP
A2	VCCIB3	VCCIB3	A38	TDI	TDI
A3	GAB2/IO52NDB3V0	IO74NDB3V0	A39	TDO	TDO
A4	GFA2/IO51NDB3V0	IO71NDB3V0	A40	VJTAG	VJTAG
A5	GFC2/IO50NDB3V0	IO69NPB3V0	A41	GDB1/IO39PPB1V0	GDA1/IO54PPB1V0
A6	VCCIB3	VCCIB3	A42	GDC1/IO38PDB1V0	GDB1/IO53PDB1V0
A7	GFA1/IO47PPB3V0	GFB1/IO67PPB3V0	A43	VCC	VCC
A8	GEB0/IO45NDB3V0	NC	A44	GCB0/IO35NPB1V0	GCB0/IO48NPB1V0
A9	XTAL1	XTAL1	A45	GCC1/IO34PDB1V0	GCC1/IO47PDB1V0
A10	GNDOSC	GNDOSC	A46	VCCIB1	VCCIB1
A11	GEC2/IO43PPB3V0	GEA1/IO61PPB3V0	A47	GBC2/IO32PPB1V0	GBB2/IO41PPB1V0
A12	IO43NPB3V0	GEA0/IO61NPB3V0	A48	VCCIB1	VCCIB1
A13	NC	VCCIB3	A49	NC	NC
A14	GNDNVM	GNDNVM	A50	GBA0/IO29RSB0V0	GBB1/IO37RSB0V0
A15	PCAP	PCAP	A51	VCCIB0	VCCIB0
A16	VCC33PMP	VCC33PMP	A52	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0
A17	NC	NC	A53	GBC1/IO26RSB0V0	IO33RSB0V0
A18	AV0	AV0	A54	IO24RSB0V0	IO29RSB0V0
A19	AG0	AG0	A55	IO21RSB0V0	IO26RSB0V0
A20	ATRTN0	ATRTN0	A56	VCCIB0	VCCIB0
A21	AG1	AG1	A57	IO15RSB0V0	IO21RSB0V0
A22	AC1	AC1	A58	IO10RSB0V0	IO13RSB0V0
A23	AV2	AV2	A59	IO07RSB0V0	IO10RSB0V0
A24	AT2	AT2	A60	GAC0/IO04RSB0V0	IO06RSB0V0
A25	AT3	AT3	A61	GAB1/IO03RSB0V0	GAC1/IO05RSB0V0
A26	AC3	AC3	A62	VCC	VCC
A27	AV4	AV4	A63	GAA1/IO01RSB0V0	GAB0/IO02RSB0V0
A28	AC4	AC4	A64	NC	NC
A29	AT4	AT4	B1	VCOMPLA	VCOMPLA
A30	NC	AG5	B2	GAA2/IO52PDB3V0	GAC2/IO74PDB3V0
A31	NC	AV5	B3	GAC2/IO51PDB3V0	GFA2/IO71PDB3V0
A32	ADCGNDREF	ADCGNDREF	B4	GFB2/IO50PDB3V0	GFB2/IO70PSB3V0
A33	VCC33A	VCC33A	B5	VCC	VCC
A34	GNDA	GNDA	B6	GFC0/IO49NDB3V0	GFC0/IO68NDB3V0
A35	PTBASE	PTBASE	B7	GEB1/IO45PDB3V0	NC
A36	VCCNVM	VCCNVM	B8	VCCOSC	VCCOSC

	QN180		QN180		
Pin Number	AFS090 Function	AFS250 Function	Pin Number	AFS090 Function	AFS250 Function
B9	XTAL2	XTAL2	B45	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0
B10	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	B46	GNDQ	GNDQ
B11	GEB2/IO42PDB3V0	IO60NDB3V0	B47	GBA1/IO30RSB0V0	GBA0/IO38RSB0V0
B12	VCC	VCC	B48	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0
B13	VCCNVM	VCCNVM	B49	VCC	VCC
B14	VCC15A	VCC15A	B50	GBC0/IO25RSB0V0	IO31RSB0V0
B15	NCAP	NCAP	B51	IO23RSB0V0	IO28RSB0V0
B16	VCC33N	VCC33N	B52	IO20RSB0V0	IO25RSB0V0
B17	GNDAQ	GNDAQ	B53	VCC	VCC
B18	AC0	AC0	B54	IO11RSB0V0	IO14RSB0V0
B19	AT0	AT0	B55	IO08RSB0V0	IO11RSB0V0
B20	AT1	AT1	B56	GAC1/IO05RSB0V0	IO08RSB0V0
B21	AV1	AV1	B57	VCCIB0	VCCIB0
B22	AC2	AC2	B58	GAB0/IO02RSB0V0	GAC0/IO04RSB0V0
B23	ATRTN1	ATRTN1	B59	GAA0/IO00RSB0V0	GAA1/IO01RSB0V0
B24	AG3	AG3	B60	VCCPLA	VCCPLA
B25	AV3	AV3	C1	NC	NC
B26	AG4	AG4	C2	NC	VCCIB3
B27	ATRTN2	ATRTN2	C3	GND	GND
B28	NC	AC5	C4	NC	GFC2/IO69PPB3V0
B29	VCC33A	VCC33A	C5	GFC1/IO49PDB3V0	GFC1/IO68PDB3V0
B30	VAREF	VAREF	C6	GFA0/IO47NPB3V0	GFB0/IO67NPB3V0
B31	PUB	PUB	C7	VCCIB3	NC
B32	PTEM	PTEM	C8	GND	GND
B33	GNDNVM	GNDNVM	C9	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0
B34	VCC	VCC	C10	GEA2/IO42NDB3V0	GEC2/IO60PDB3V0
B35	ТСК	ТСК	C11	NC	GEA2/IO58PSB3V0
B36	TMS	TMS	C12	NC	NC
B37	TRST	TRST	C13	GND	GND
B38	GDB2/IO41PSB1V0	GDA2/IO55PSB1V0	C14	NC	NC
B39	GDC0/IO38NDB1V0	GDB0/IO53NDB1V0	C15	NC	NC
B40	VCCIB1	VCCIB1	C16	GNDA	GNDA
B41	GCA1/IO36PDB1V0	GCA1/IO49PDB1V0	C17	NC	NC
B42	GCC0/IO34NDB1V0	GCC0/IO47NDB1V0	C18	NC	NC
B43	GCB2/IO33PSB1V0	GBC2/IO42PSB1V0	C19	NC	NC
B44	VCC	VCC	C20	NC	NC

FG256					
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function	
E13	VCCIB1	VCCIB1	VCCIB2	VCCIB2	
E14	GCC2/IO33NDB1V0	IO42NDB1V0	IO32NDB2V0	IO46NDB2V0	
E15	GCB2/IO33PDB1V0	GBC2/IO42PDB1V0	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0	
E16	GND	GND	GND	GND	
F1	NC	NC	IO79NDB4V0	IO111NDB4V0	
F2	NC	NC	IO79PDB4V0	IO111PDB4V0	
F3	GFB1/IO48PPB3V0	IO72NDB3V0	IO76NDB4V0	IO112NDB4V0	
F4	GFC0/IO49NDB3V0	IO72PDB3V0	IO76PDB4V0	IO112PDB4V0	
F5	NC	NC	IO82PSB4V0	IO120PSB4V0	
F6	GFC1/IO49PDB3V0	GAC2/IO74PPB3V0	GAC2/IO83PPB4V0	GAC2/IO123PPB4V0	
F7	NC	IO09RSB0V0	IO04PPB0V0	IO05PPB0V1	
F8	NC	IO19RSB0V0	IO08NDB0V1	IO11NDB0V1	
F9	NC	NC	IO20PDB1V0	IO27PDB1V1	
F10	NC	IO29RSB0V0	IO23NDB1V1	IO37NDB1V2	
F11	NC	IO43NDB1V0	IO36NDB2V0	IO50NDB2V0	
F12	NC	IO43PDB1V0	IO36PDB2V0	IO50PDB2V0	
F13	NC	IO44NDB1V0	IO39NDB2V0	IO59NDB2V0	
F14	NC	GCA2/IO44PDB1V0	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0	
F15	GCC1/IO34PDB1V0	GCB2/IO45PDB1V0	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0	
F16	GCC0/IO34NDB1V0	IO45NDB1V0	IO40NDB2V0	IO60NDB2V0	
G1	GEC0/IO46NPB3V0	IO70NPB3V0	IO74NPB4V0	IO109NPB4V0	
G2	VCCIB3	VCCIB3	VCCIB4	VCCIB4	
G3	GEC1/IO46PPB3V0	GFB2/IO70PPB3V0	GFB2/IO74PPB4V0	GFB2/IO109PPB4V0	
G4	GFA1/IO47PDB3V0	GFA2/IO71PDB3V0	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0	
G5	GND	GND	GND	GND	
G6	GFA0/IO47NDB3V0	IO71NDB3V0	IO75NDB4V0	IO110NDB4V0	
G7	GND	GND	GND	GND	
G8	VCC	VCC	VCC	VCC	
G9	GND	GND	GND	GND	
G10	VCC	VCC	VCC	VCC	
G11	GDA1/IO37NDB1V0	GCC0/IO47NDB1V0	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0	
G12	GND	GND	GND	GND	
G13	IO37PDB1V0	GCC1/IO47PDB1V0	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0	
G14	GCB0/IO35NPB1V0	IO46NPB1V0	IO41NPB2V0	IO61NPB2V0	
G15	VCCIB1	VCCIB1	VCCIB2	VCCIB2	
G16	GCB1/IO35PPB1V0	GCC2/IO46PPB1V0	GCC2/IO41PPB2V0	GCC2/IO61PPB2V0	
H1	GEB1/IO45PDB3V0	GFC2/IO69PDB3V0	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0	
H2	GEB0/IO45NDB3V0	IO69NDB3V0	IO73NDB4V0	IO108NDB4V0	



Package Pin Assignments

FG484			FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function	
L17	VCCIB2	VCCIB2	N8	GND	GND	
L18	IO46PDB2V0	IO69PDB2V0	N9	GND	GND	
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0	N10	VCC	VCC	
L20	VCCIB2	VCCIB2	N11	GND	GND	
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0	N12	VCC	VCC	
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0	N13	GND	GND	
M1	NC	IO103PDB4V0	N14	VCC	VCC	
M2	XTAL1	XTAL1	N15	GND	GND	
M3	VCCIB4	VCCIB4	N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0	
M4	GNDOSC	GNDOSC	N17	NC	IO78PDB2V0	
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0	N18	GND	GND	
M6	VCCIB4	VCCIB4	N19	IO47NDB2V0	IO72NDB2V0	
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0	N20	IO47PDB2V0	IO72PDB2V0	
M8	VCCIB4	VCCIB4	N21	GND	GND	
M9	VCC	VCC	N22	IO49PDB2V0	IO71PDB2V0	
M10	GND	GND	P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0	
M11	VCC	VCC	P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0	
M12	GND	GND	P3	IO68NDB4V0	IO101NDB4V0	
M13	VCC	VCC	P4	IO65PDB4V0	IO96PDB4V0	
M14	GND	GND	P5	IO65NDB4V0	IO96NDB4V0	
M15	VCCIB2	VCCIB2	P6	NC	IO99NDB4V0	
M16	IO48NDB2V0	IO70NDB2V0	P7	NC	IO97NDB4V0	
M17	VCCIB2	VCCIB2	P8	VCCIB4	VCCIB4	
M18	IO46NDB2V0	IO69NDB2V0	P9	VCC	VCC	
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0	P10	GND	GND	
M20	VCCIB2	VCCIB2	P11	VCC	VCC	
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0	P12	GND	GND	
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0	P13	VCC	VCC	
N1	NC	IO103NDB4V0	P14	GND	GND	
N2	GND	GND	P15	VCCIB2	VCCIB2	
N3	IO68PDB4V0	IO101PDB4V0	P16	IO56NDB2V0	IO83NDB2V0	
N4	NC	IO100NPB4V0	P17	NC	IO78NDB2V0	
N5	GND	GND	P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0	
N6	NC	IO99PDB4V0	P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0	
N7	NC	IO97PDB4V0	P20	IO51NDB2V0	IO73NDB2V0	